

EE3220: Assignment 2 – Answer (Total of 64 marks)

Q1

(i)

No. of ROM chips required: $24\text{M}/4\text{M} = 6$

No. of RAM chips required: $32\text{M}/8\text{M} = 4$

(ii)

		Address lines											
Device	nGCS	24	23	22	21	20	19	18 - 05	04	03	02	01	00
ROM0	0(000)	0	0	X	X	X	X	X	X	X	X	X	-
ROM1	0(000)	0	1	X	X	X	X	X	X	X	X	X	-
ROM2	0(000)	0	0	X	X	X	X	X	X	X	X	X	-
RAM0	6(110)	0	X	X	X	X	X	X	X	X	X	-	-
RAM1	6(110)	1	X	X	X	X	X	X	X	X	X	-	-

(iii)

$$\text{ROM0_CS} = \text{nGCS0} \overline{A_{24}} \overline{A_{23}}$$

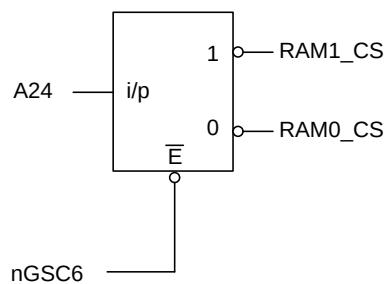
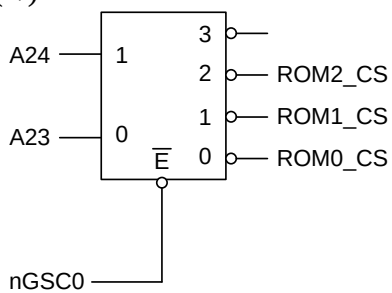
$$\text{ROM1_CS} = \text{nGCS0} \overline{A_{24}} A_{23}$$

$$\text{ROM2_CS} = \text{nGCS0} A_{24} \overline{A_{23}}$$

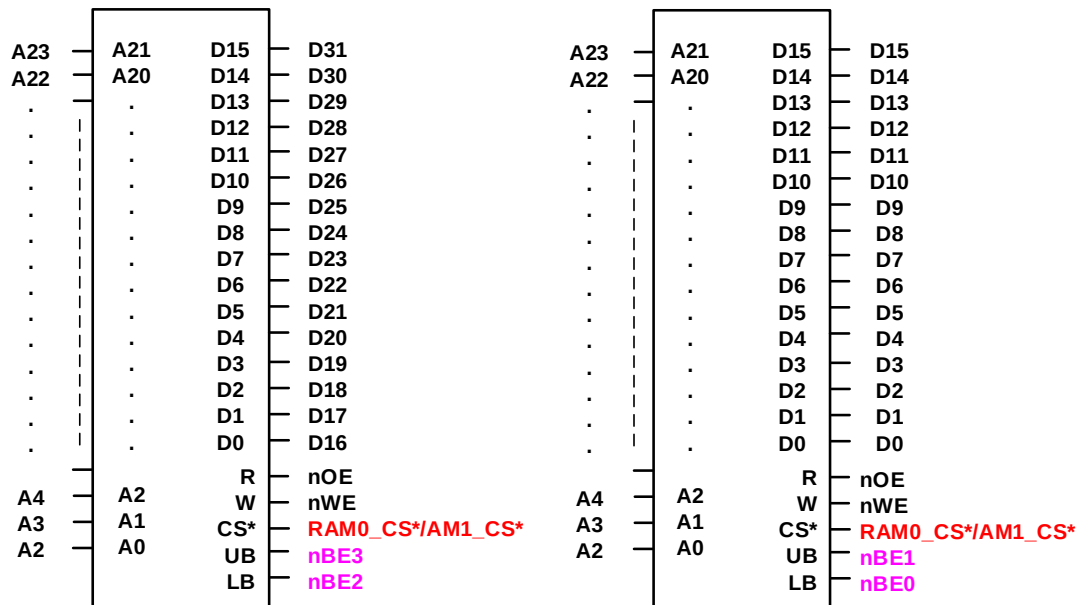
$$\text{RAM0_CS} = \text{nGCS6} \overline{A_{24}}$$

$$\text{RAM1_CS} = \text{nGCS6} A_{24}$$

(iv)



(v)



Q2. (i) For 70 ns SRAM and CPU running at 50 MHz ($t_{cyc} = 20$ ns):

Read cycle:

$$t_{RAD} + t_{AA} + \text{margin} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$\text{i.e., } T_{acc} \geq (t_{RAD} + t_{AA} + t_{RDS}) / t_{cyc} \quad (\text{Margin}_{\min} = 0)$$

$$T_{acc_{\min}} \geq (12 + 70 + 1) / 20 \geq 4.15 = 5$$

Condition checking (a):

$$(a) \quad t_{RCD} + t_{DEC} + t_{ACE} + \text{margin} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$11 + 12 + 70 + 1 = 94 \Rightarrow 94 / 20 = 4.7$$

$$\Rightarrow T_{acc} = 5$$

Condition checking (b):

$$(b) \quad t_{ROD} + t_{OE} + \text{margin} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$11 + 40 + 1 = 52 \Rightarrow 52 / 20 = 2.6$$

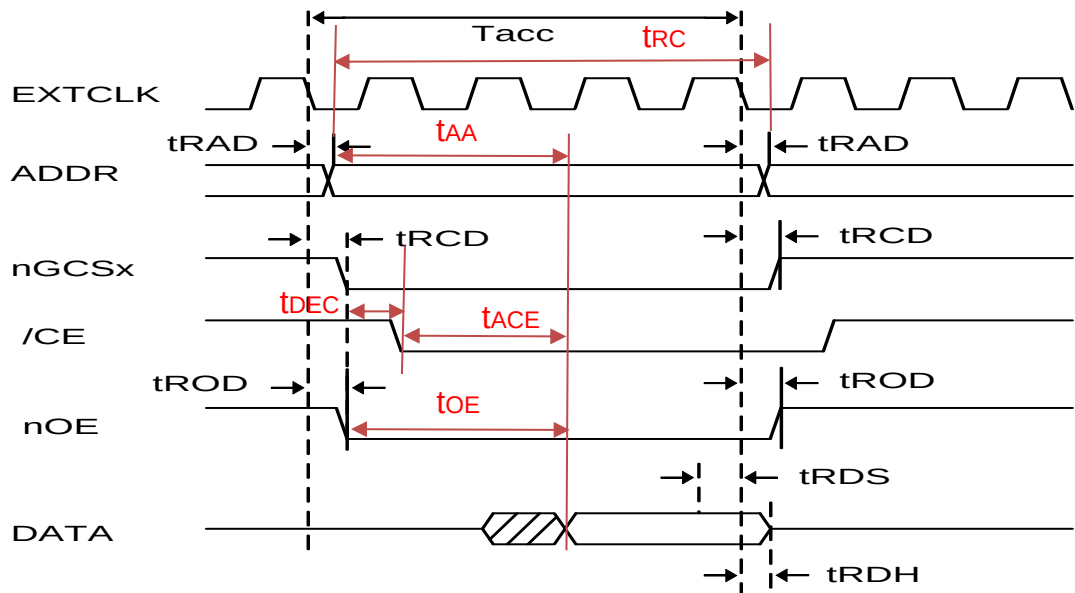
$$\Rightarrow T_{acc} = 3$$

Write cycle:

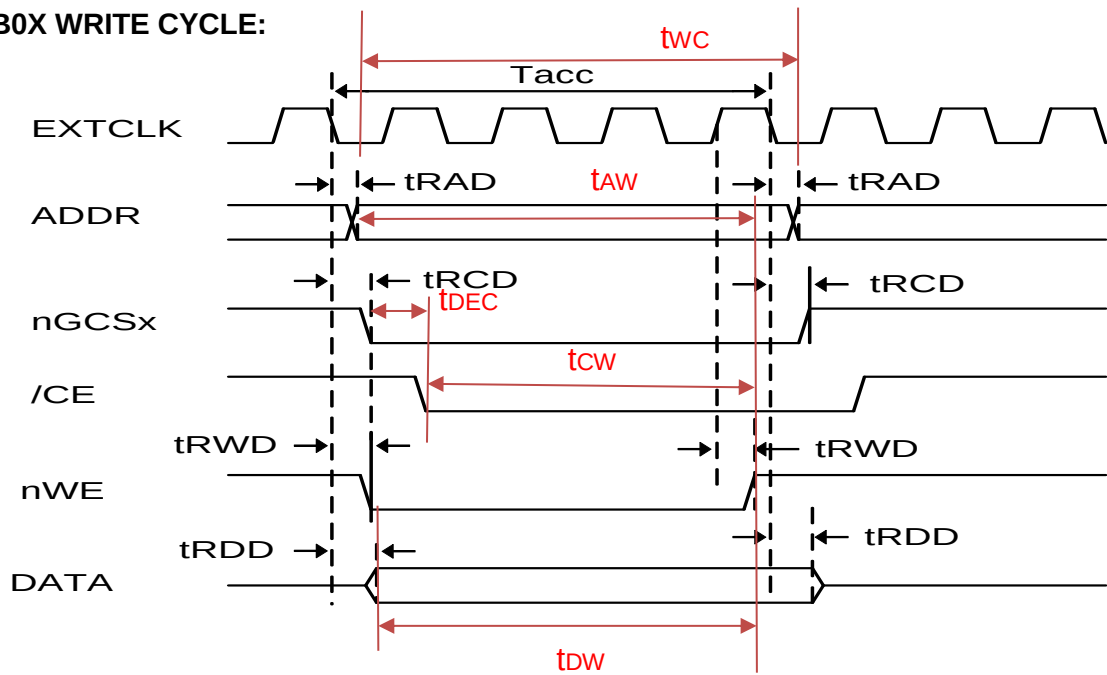
			Req'd
tWC	$N \times T_{cyc}$	$N \times 20$	70
tCW	$(N-0.5) \times T_{cyc} + t_{RWD} - t_{RCD} - t_{DEC}$	$(N-0.5) \times 25 + 14 - 11 - t_{DEC} = (N-0.5) \times 20 + 3 - 12 = (N-0.5) \times 20 - 12$	60
tAW	$(N-0.5) \times T_{cyc} + t_{RWD} - t_{RAD}$	$(N-0.5) \times 25 + 14 - 12 = (N-0.5) \times 20 + 2$	60
tWP	$(N-0.5) \times T_{cyc}$	$(N-0.5) \times 20$	50
tDW	$(N-0.5) \times T_{cyc} + t_{RWD} - t_{RDD}$	$(N-0.5) \times 25 + 14 - 14 = (N-0.5) \times 20$	30

$N = 5$ satisfy all requirement

S3C44B0X READ CYCLE:



S3C44B0X WRITE CYCLE:



Q3.

66 MHz → (tCYC = 15.15 ns):

tRCD = 20ns (2 clock) → tRCD = 00

Column address: A0 ~ A8 (=9 bits) → SCAN = 01

Thus, rBANKCON6(7) = 1 1xxx xxxx xxxx 0001

Enable refresh : REFEN = 1

CBR/Auto Refresh: TREFMD = 0

Precharge time = 20ns (~2 clock) → tRP = 00

Minimum RC = 70ns (~5 clocks) → tRC = 01

Refresh period = 64ms/4096 = 15.625μs

Refresh counter = $2^{11} + 1 - 66 \times 15.625 = 1018 = 0x3FA$

Since Tchr can be 00, 01, 10 or 11, we have

rREFRESH = 0x8□03FA (□ can be 4,5,6 or 7)

