

Devices II Outline

- High-level description of MOSFET function
- MOSFET structure (NMOS)
 - > Based on the N-channel MOSFET (NMOS)
- Gate control and the concept of **transconductance**
- MOSFET operating modes
 - > Based on the N-channel MOSFET (NMOS)
- P-channel MOSFET (PMOS)
- Some examples on analyzing the operating modes of MOSFETs

MOSFET in the off state

A MOSFET has three terminals:

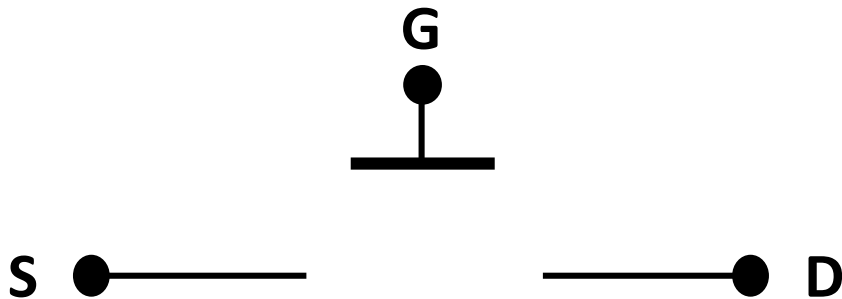
G terminal is called the GATE

S terminal is called the SOURCE

D terminal is called the DRAIN

The voltage applied at the Gate (V_G) controls the resistance between S and D

In the example below, the connection between S and D terminals is an open circuit as the device has been not switched on or activated



In the off state, no current flow can flow between S and D for any voltage difference applied across terminals S-D

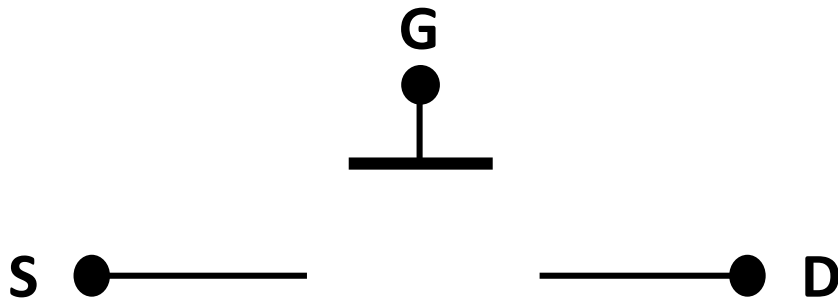
Activating the MOSFET

To activate the MOSFET, V_G must be equal or larger than a minimum value

This minimum voltage to switch-on the MOSFET is called the **Threshold Voltage** (symbolized by V_T). The value of V_T is fixed for given MOSFET model.

In the example below, $V_G > V_T$ to create an electrical connection between S and D terminals.

This electrical connection will have some value of resistance (which we here symbolize using R_o).



The value of R_o depends on the value of V_G relative to V_T . Generally, increasing V_G will cause R_o to fall.

Now that S-D are connected, current can follow between S-D when we apply a voltage across S-D.

MOSFET structure

M: Metal (Forms the Gate)

O: Oxide (Insulator between Gate and Semiconductor substrate)

S: Semiconductor (Source and Drain regions, substrate)

F: Field

E: Effect

T: Transistor

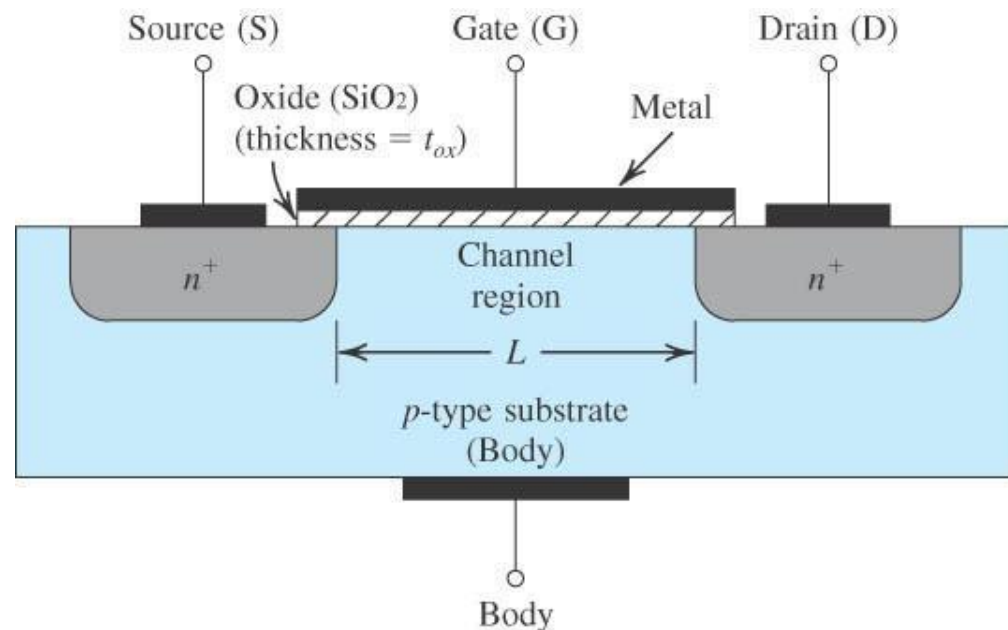
3 materials: MOS

2 semiconductor regions:

N-type and P-type

*Note: In normal operation, ALL
pn junctions are reverse biased*

Oxide resistivity: $10^{16} \Omega\text{cm}$

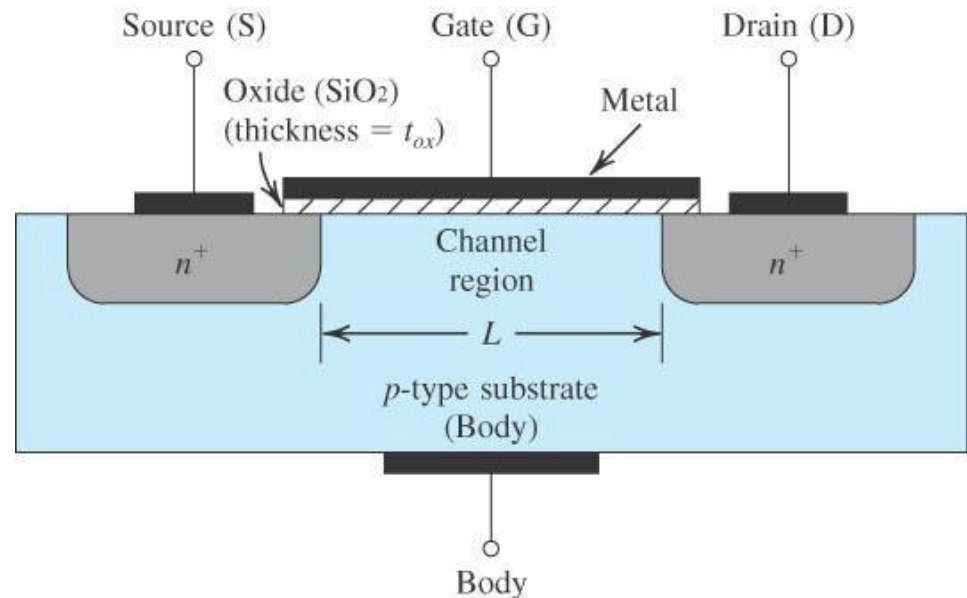


E-type MOSFET structure

Notice that the figure contains a label “Channel region”. But there is no channel region shown in the figure. The channel not been formed yet because the device is still in the off state. It needs to be activated by forming the channel.

When $V_G > V_T$, an n-type channel will form below the surface of the oxide to connect the S and D regions. The device is thereby activated.

V_G is applied relative to the body of the MOSFET. The body of the MOSFET is the reference node.



E-type MOSFET structure

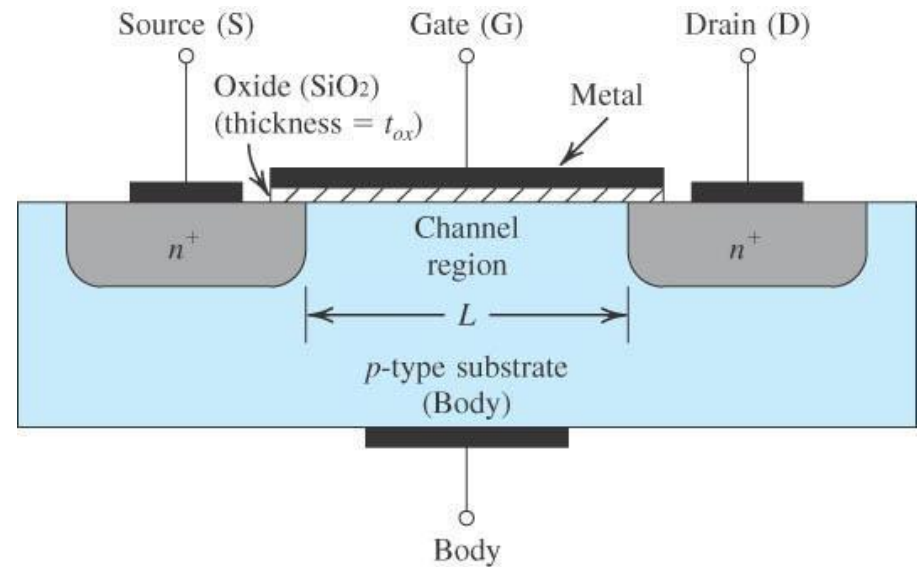
This type of MOSFET that requires us to actively switch-on the device is called Enhancement-type (E-type) MOSFET

We will focus on E-type MOSFETs for this course

E-type MOSFETs are normally off (until they are activated by V_G)

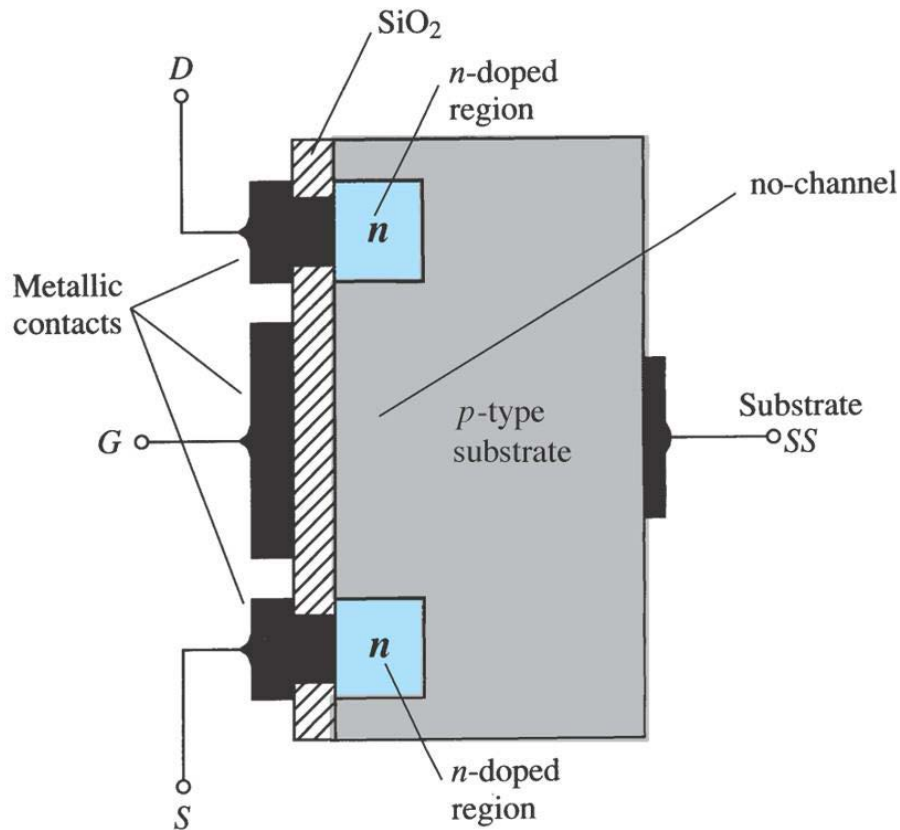
Other type: Depletion (D-type) MOSFET

D-type MOSFETs are normally on and require a Gate voltage to be applied to switch-off the device

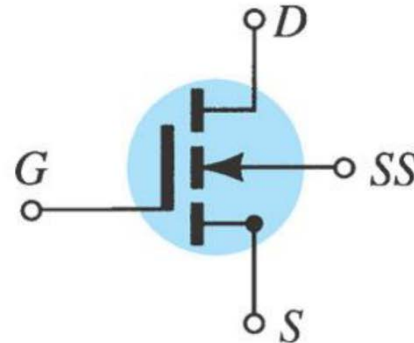


MOSFET symbol

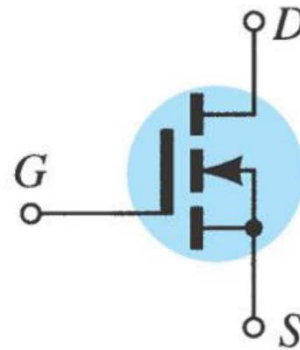
As the channel of this MOSFET is n-type, it is called an n-channel MOSFET (NMOS)



n-channel

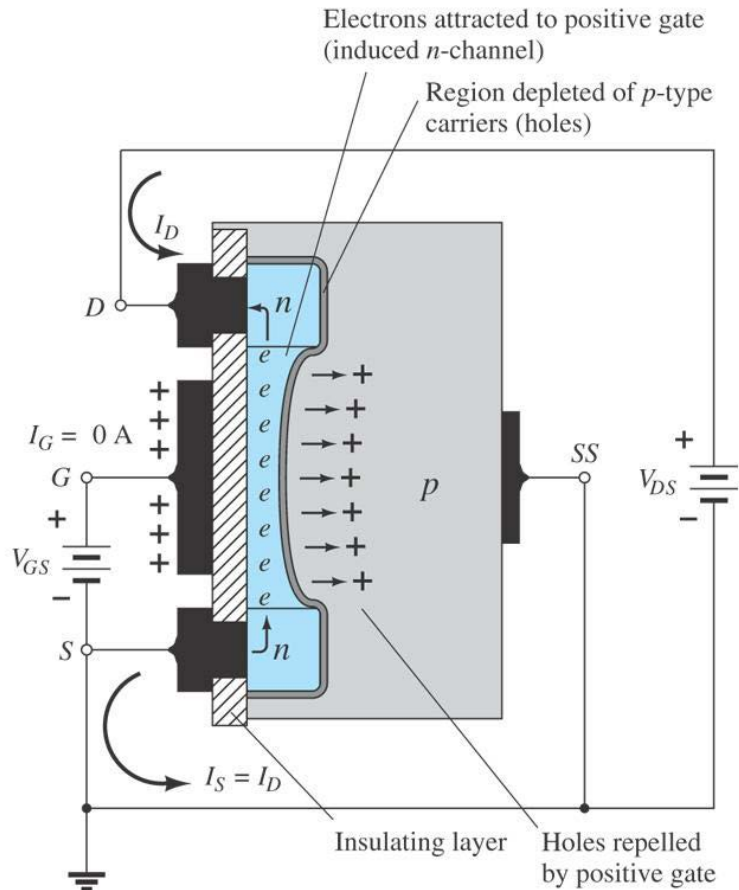


Recall from diodes



When the body/substrate is connected to the source

MOSFET current



The MOSFET is designed such that the free carriers flow from S $\rightarrow$ D.

S: Source – Where it starts

D: Drain – Where it ends

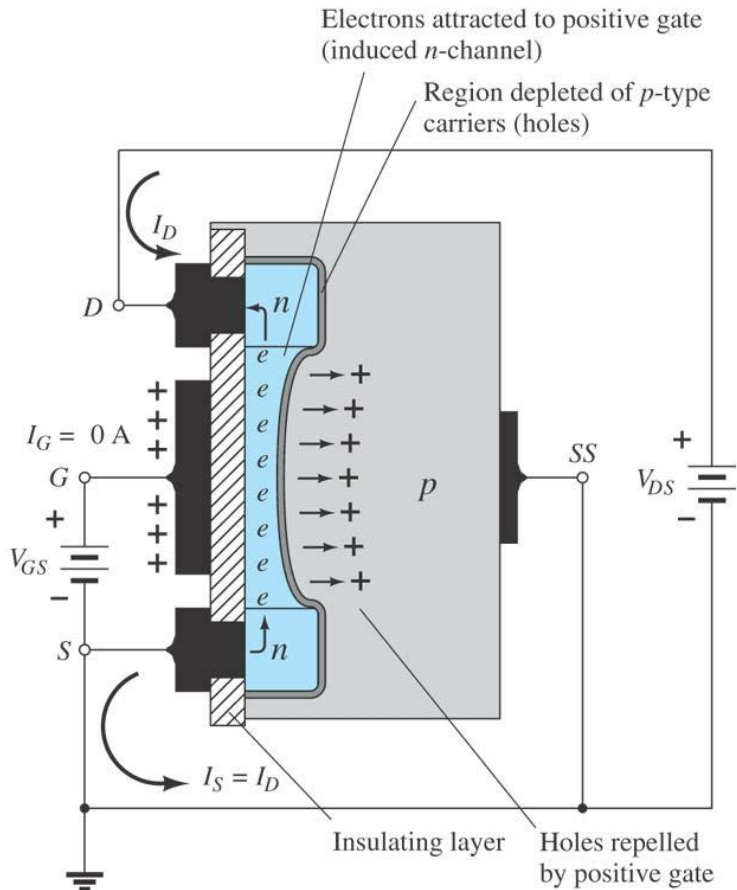
In an n-channel MOSFET, S and D regions are n-type:

Majority carriers for n-type:

Channel current runs from:

_____ $\rightarrow$ _____

MOSFET Current



I_D : Current flowing into D

I_S : Current flowing out of S

Why is $I_D = I_S$?

Why is $I_G = 0\text{ A}$?

If there was voltage across G and SS, would what be the current?

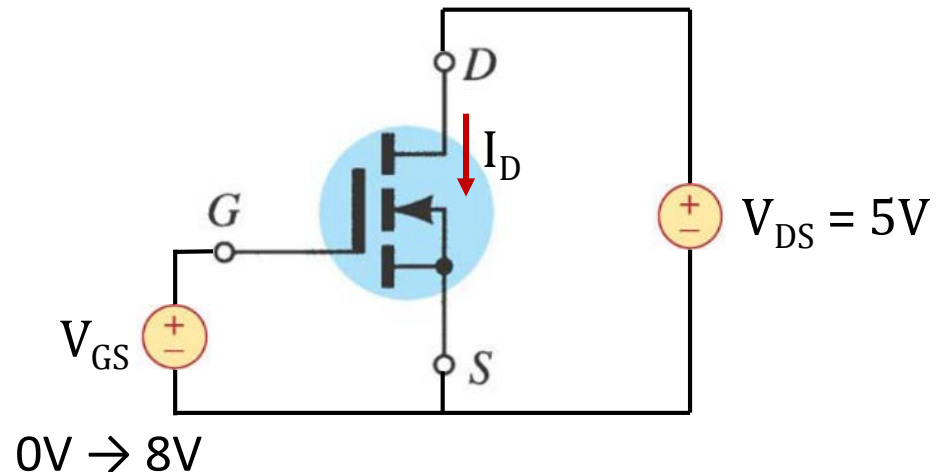
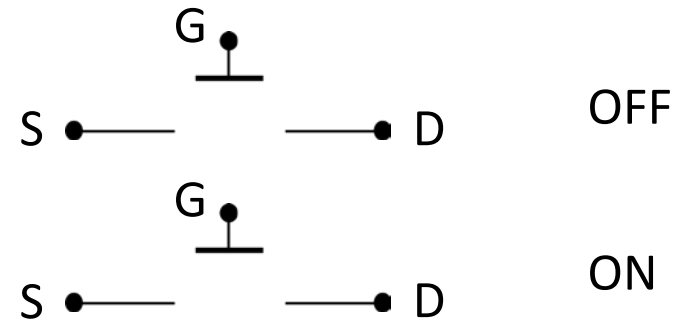
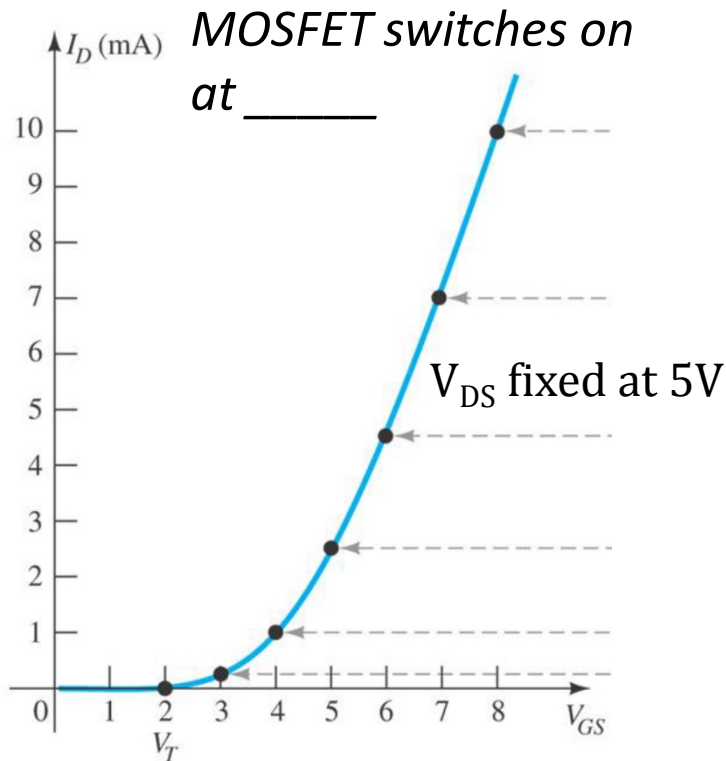
NMOS: I_D flows from D $\rightarrow$ S: Voltage can only be dropped from D to S (V_{DS} must be positive)

Transconductance Characteristic

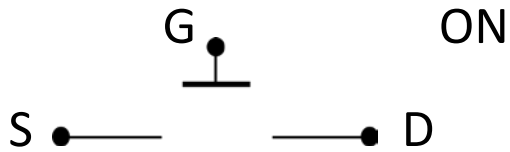
Trans: Across

Conductance: Inverse of Resistance ($G = I/V$)

Transconductance Characteristic: Describes how I_D changes with V_{GS} (while V_{DS} is kept constant)



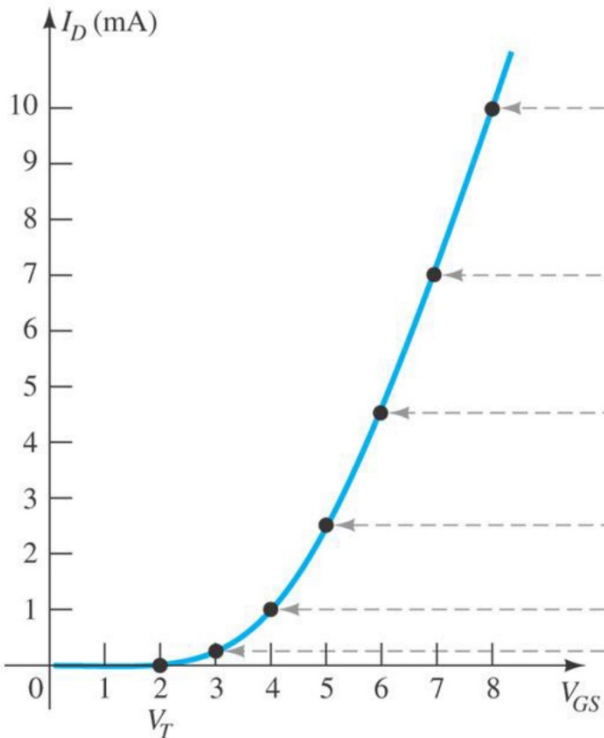
Transconductance Characteristic



Notice that when the MOSFET is switched on, increasing V_{GS} increases I_D even though V_{DS} is constant.

If R_o was constant, then Ohm's law says that for constant V_{DS} , I_D must be constant.

So why does this happen?



For I_D to increase while V_{DS} remains fixed means that R_o must be decreasing when V_{GS} is being increased.

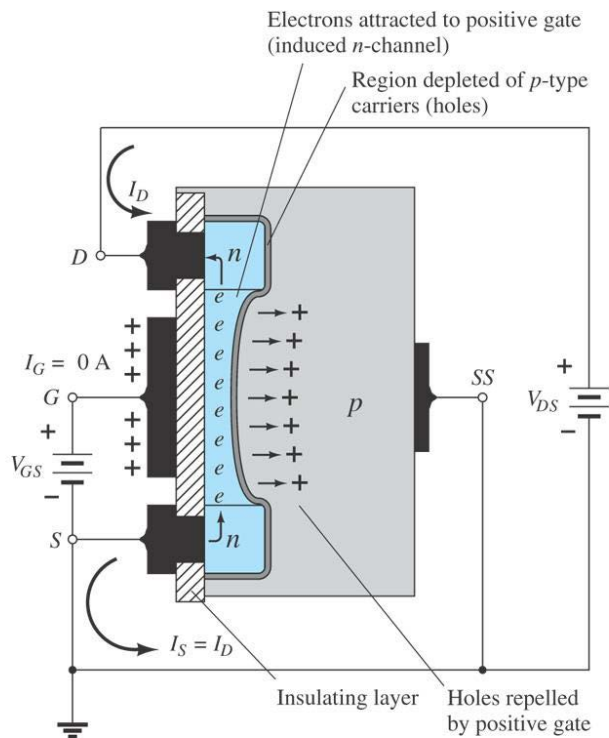
How does this happen?

Transconductance: Gate voltage effect

Before we answer question of why the channel resistance (R_o) decreases as V_{GS} increases relative to V_T , we should first answer the question:

How does the n-channel form in the first place?

How do you get a n-channel from a P-type substrate?



P-type substrate

Majority carriers: _____

Minority carriers: _____

N-type channel

Majority carriers: _____

Minority carriers: _____

Where do the electrons in the n-channel come from?
_____ carriers in the substrate

Transconductance: Gate voltage effect

Forming of the n-channel:

When V_{GS} reaches V_T : Thin layer of electrons form a channel just underneath the oxide to connect the source and drain regions

This can be called an Inversion Layer (n-channel from a p-type substrate)

Increasing V_{GS} beyond V_T :

Electron concentration in n-channel increases

Resistivity of the n-channel falls as a result

Therefore I_D will increase as we increase V_{GS} without increasing V_{DS}

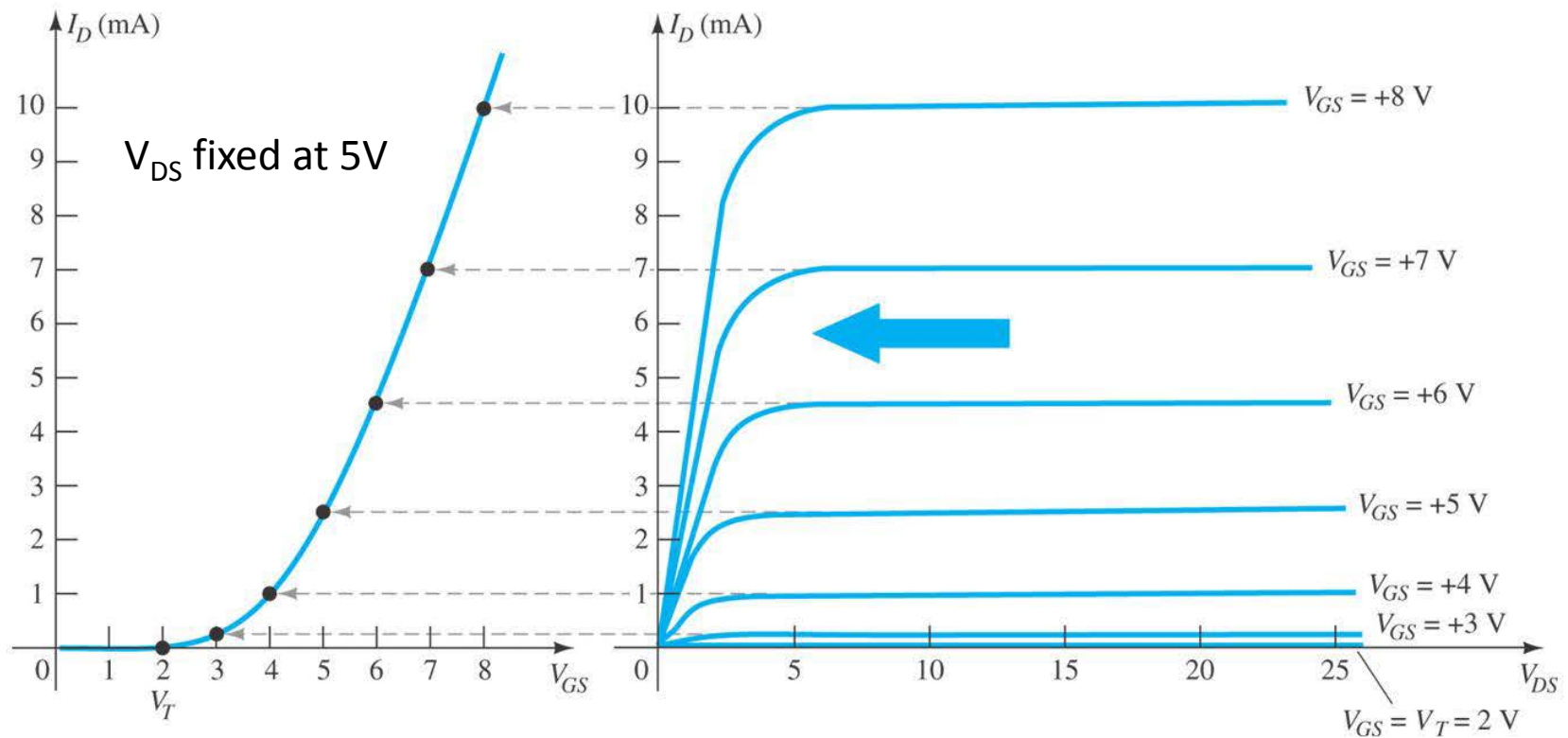
Go back to the transconductance curve:

How many sections in the curve can you identify other than just ON/OFF?

Within the ON state, can you see that there are two sections of the curve?

Initially quadratic then linear. What do these sections mean?

E-type MOSFET Characteristic



Quadratic:

Linear:

Plot of I_D vs V_{DS} when V_{GS} is constant

Triode region: When I_D is linear with V_{DS}

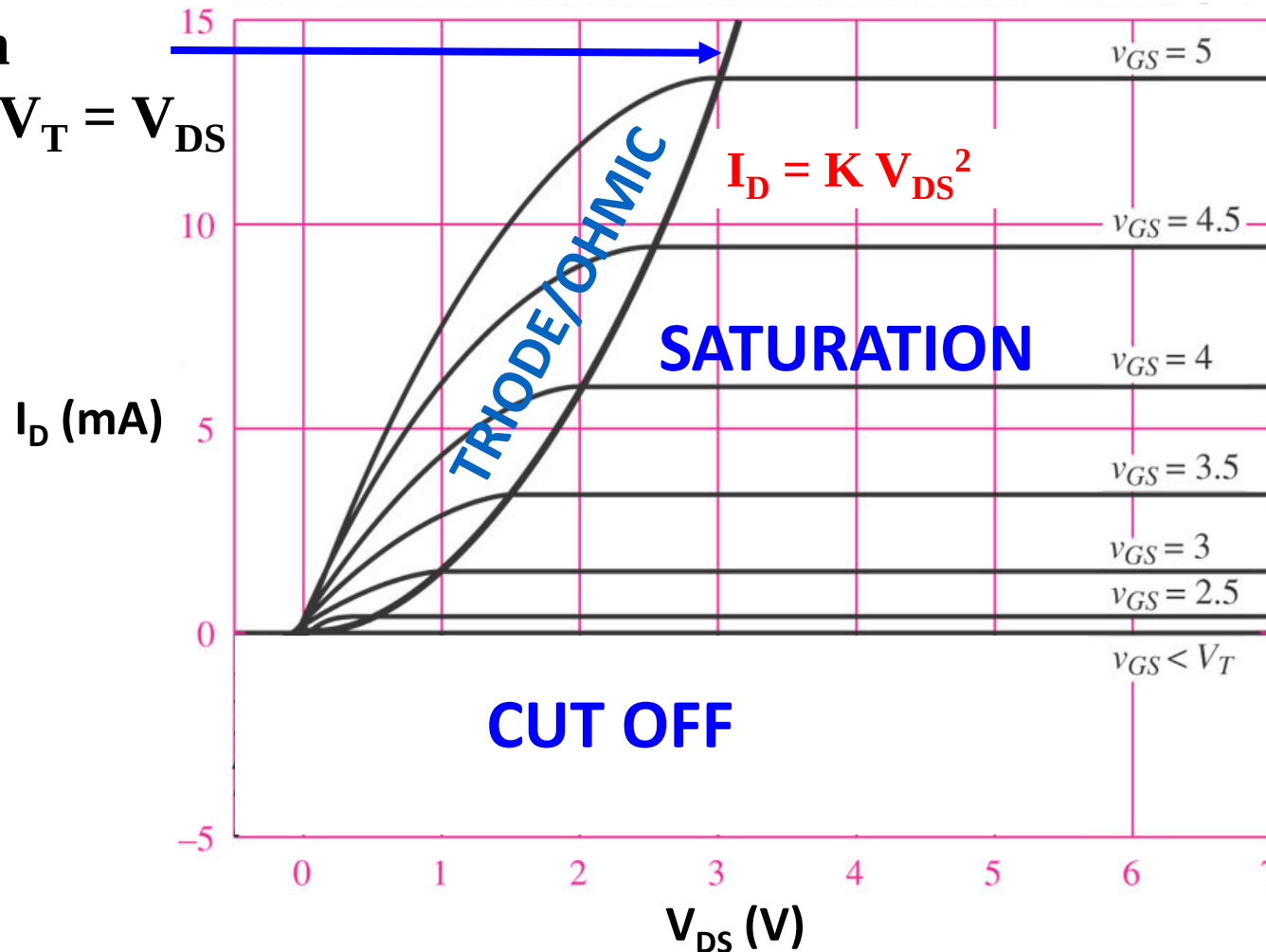
Saturation region: When I_D is constant with V_{DS}

Operating regions

K is a constant with the units: mA/V²

When

$$V_{GS} - V_T = V_{DS}$$



Cut-off mode

Applied voltage conditions:

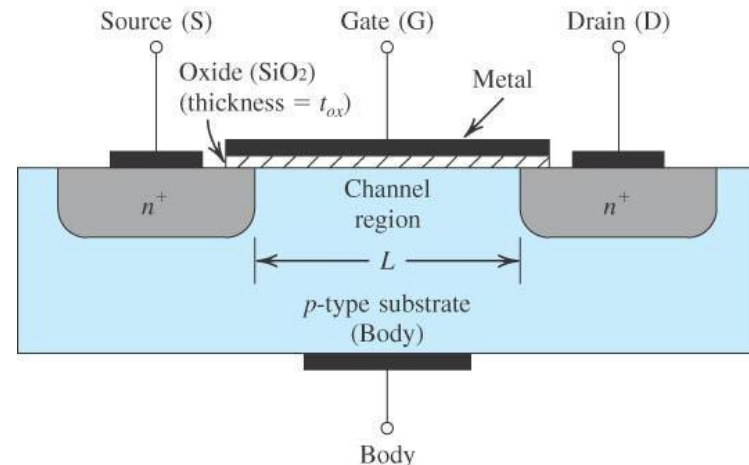
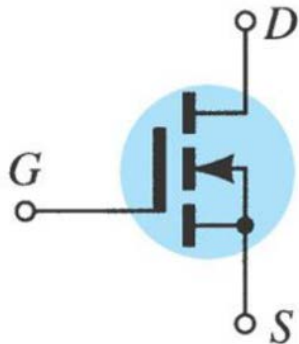
$$V_{GS} < V_T \text{ and } V_{GD} < V_T$$

Insufficient gate voltage anywhere along the length of the channel region to form a channel as V_T has not been reached.

No channel is formed under the gate to connect source and drain

No channel current (I_D) for any voltage applied across drain and source

This is what we previously referred to as the OFF state of the MOSFET

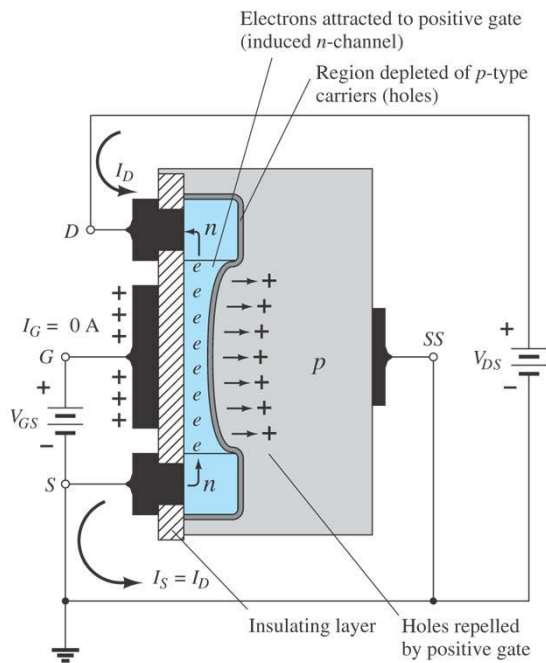


Triode mode

Applied voltage conditions:

$$V_{GS} > V_T \text{ and } V_{GD} > V_T$$

Sufficient gate voltage everywhere along the length of the channel region to form a channel as V_T has been reached or exceeded.



Increase V_{GS} :

Channel resistance falls and I_D increases

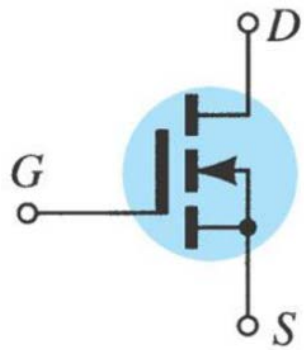
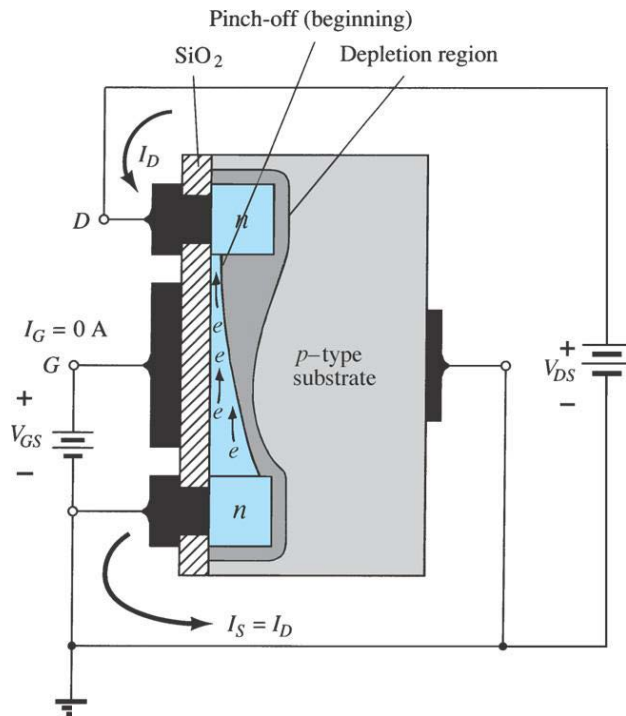
Increase V_{DS} :

Channel resistance follows Ohm's law so I_D increases

I_D is dependent on V_{DS} and V_{GS} in the triode region

Tri: Three (Voltage between the 3 terminals have an effect on I_D)

Increasing V_{DS} (fixed V_{GS}) in Triode Mode



$$V_{GS} - V_{GD} = V_{DS}$$

When $V_{DS} > 0V$: $V_{GD} < V_{GS}$

$(V_{GD} - V_T)$ will be less than $(V_{GS} - V_T)$

Channel close to the drain will be _____ compared to close to S

As V_{DS} is increased further, channel close to the drain will _____ further

When V_{GD} finally drops and equals V_T , the channel close to the drain will pinch off

When $V_{GS} > V_T$ but $V_{GD} = V_T$:

The NMOS reaches **Pinch-off**

Increasing V_{DS} further: V_{GD} _____ V_T

NMOS enters into _____ mode

Saturation mode

Applied voltage conditions:

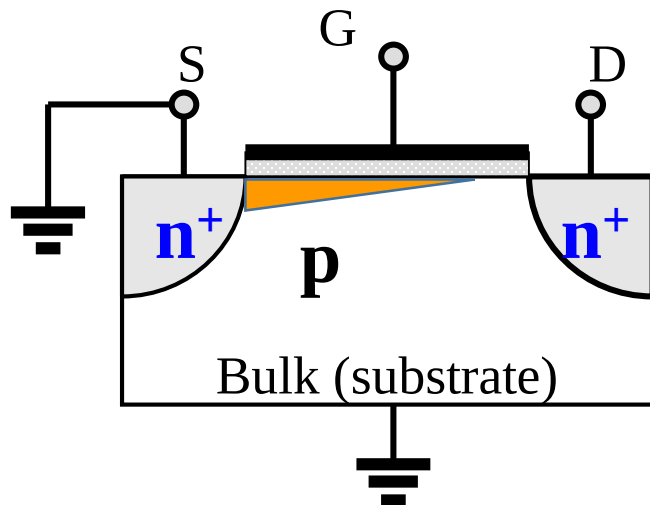
$$V_{GS} > V_T \text{ and } V_{GD} < V_T$$

Channel near the drain disappears (but I_D does not drop to zero)

Depleted section of the channel will have much higher resistance than the wider sections of the channel

Most of V_{DS} appears across the depleted section of the channel region

Electrons are swept across the depleted portion of the channel region



I_D is almost independent of V_{DS}

Channel current equations

Triode/Ohmic mode:

$$I_D = K [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

Dependent on V_{DS} and V_{GS}

Values of V_T and K depend on the MOSFET model but are fixed for a given model

Saturation mode:

$$I_D = K (V_{GS} - V_T)^2$$

Independent of V_{DS} (recall: I_D does not change with V_{DS} in saturation mode)

Pinch-off: $V_{DS} = V_{GS} - V_T$

$$K = \frac{\mu C_{ox}}{2} \left(\frac{W}{L} \right)$$

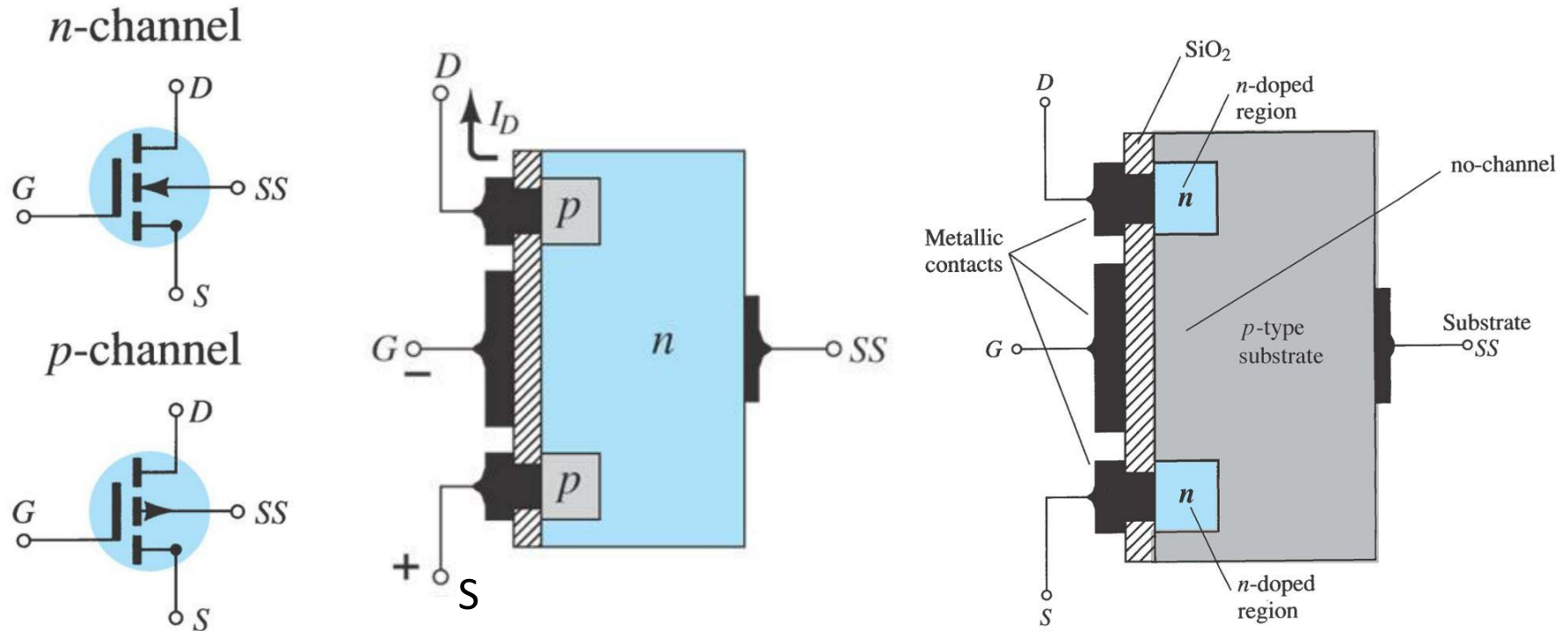
Mobility of carriers: μ

C_{ox} : Next set of slides

$$I_D = K V_{DS}^2$$

K is known as the conductance parameter (constant)

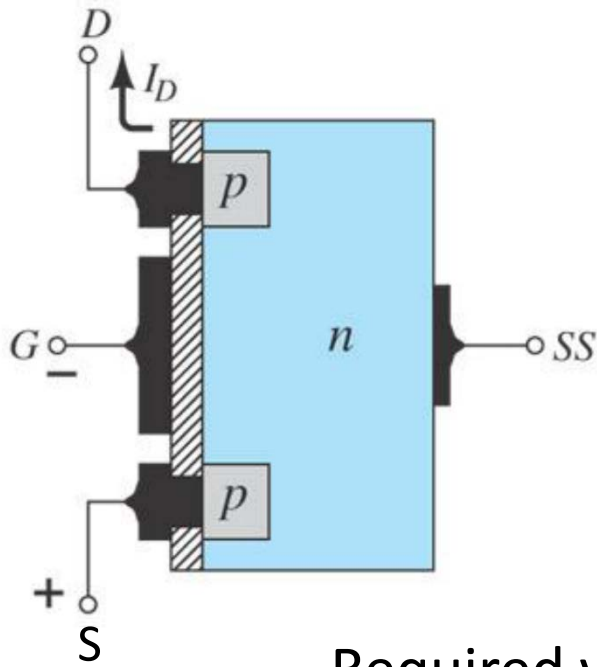
P-channel E-type MOSFET (PMOS)



Compared to the NMOS, the semiconductor regions are reversed/opposite

	PMOS	NMOS
Source/Drain region	-type	-type
Substrate	-type	-type

PMOS



Channel current:

Majority carriers in source-channel-drain:

Free carriers flow from source → drain

Current flows from _____ → _____

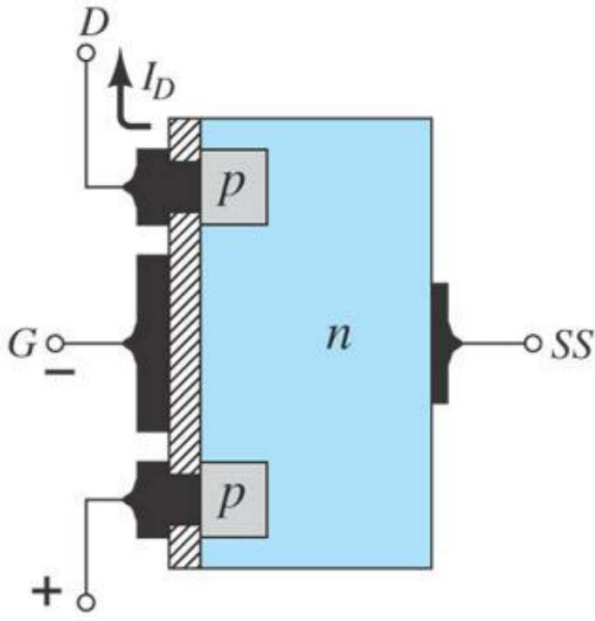
Required voltage applied across source and drain

Voltage must be dropped from _____ to _____

$V_{DS} < 0V$ (more common to use $V_{SD} > 0V$)

Typically connect source and substrate as well (same as NMOS)

PMOS activation



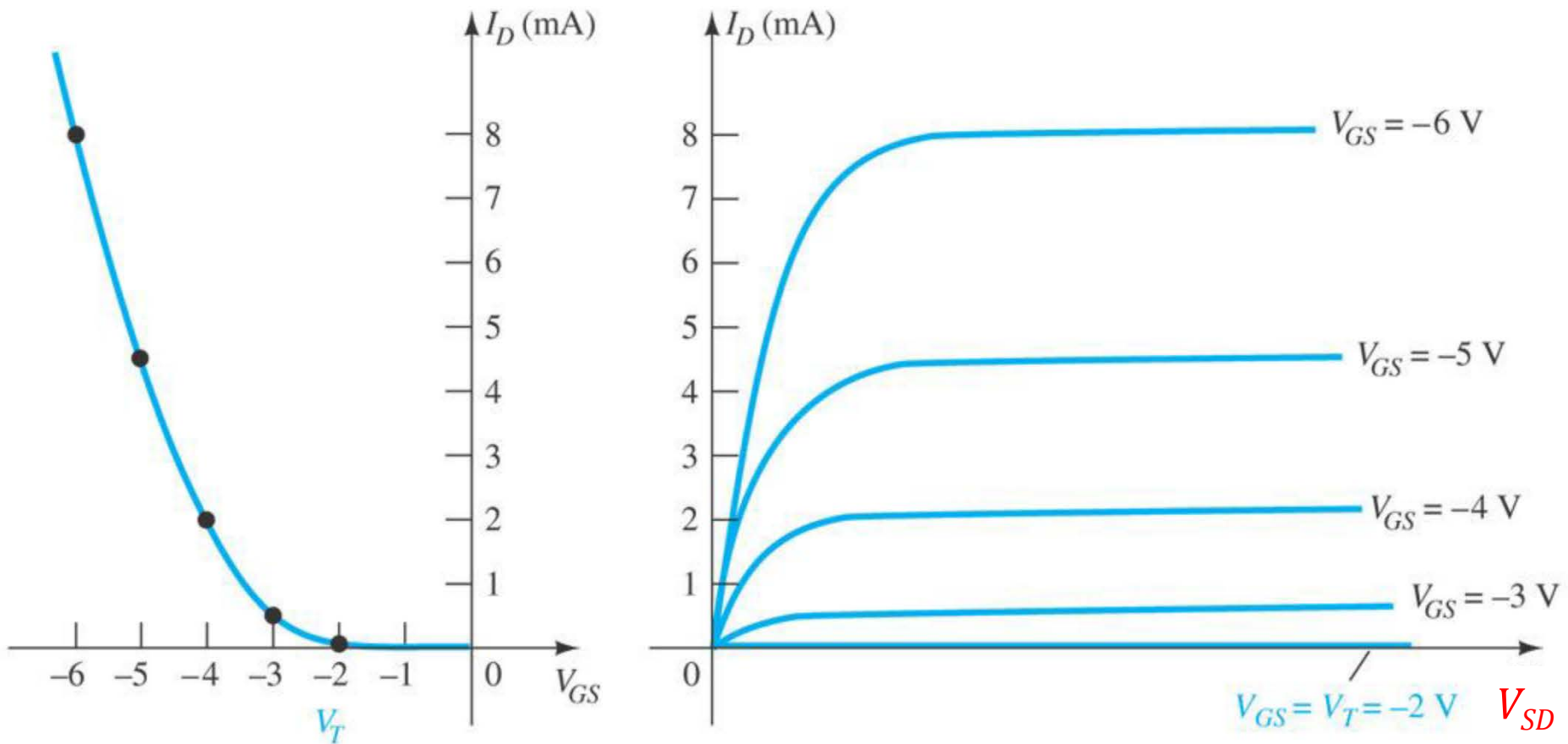
To switch-on a PMOS, we must form a p-channel to connect between source and drain.

To attract holes to the surface of the oxide layer, V_{GS} must be _____
(common to use V_{SG} instead)

Relative to the substrate (SS), the threshold voltage (V_T) for a PMOS will be _____

To form a p-channel in PMOS: $V_{GS} < V_T$ or $V_{SG} > |V_T|$

PMOS characteristic

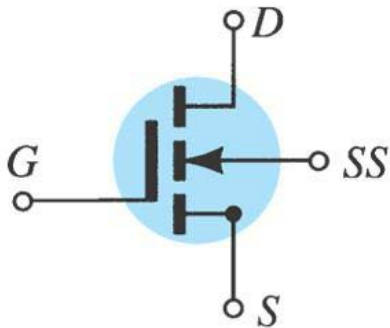


PMOS switches on when $V_{GS} < V_T$

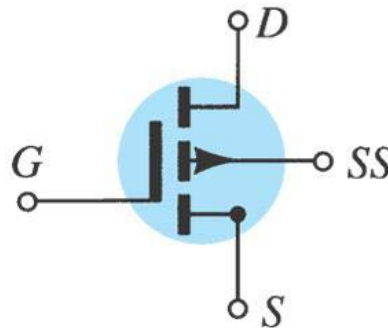
I_D increases as V_{GS} becomes more negative

E-type NMOS and PMOS

n-channel



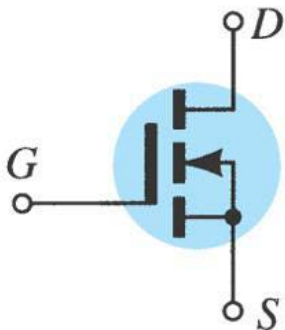
p-channel



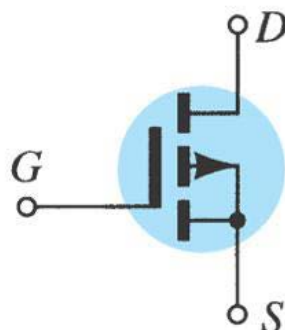
Recall from before



Notice how in the PMOS, the arrow points away from the channel and towards the substrate



(a)



(b)

Bottom figures: SS (body) connected to Source

How to check the operating mode

Does V_{GS} reach or exceed V_T to switch on the MOSFET?

NO

Cut-off mode

YES

ON-state: Either saturation / triode

Does V_{GD} exceed V_T ?

NO

Saturation mode

YES

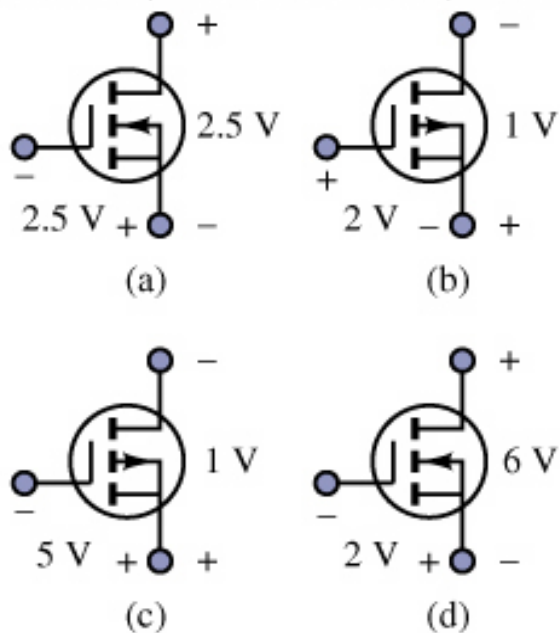
Triode mode

Example 1

The transistors have $|V_T| = 3\text{V}$. Determine the operating region for each MOSFET.

For NMOS: $V_T = 3\text{V}$; V_{GS} needs to exceed this voltage for the NMOS to turn on.

For PMOS: $V_T = \text{_____}$; V_{GS} needs to be more negative than this voltage for the PMOS to turn on.



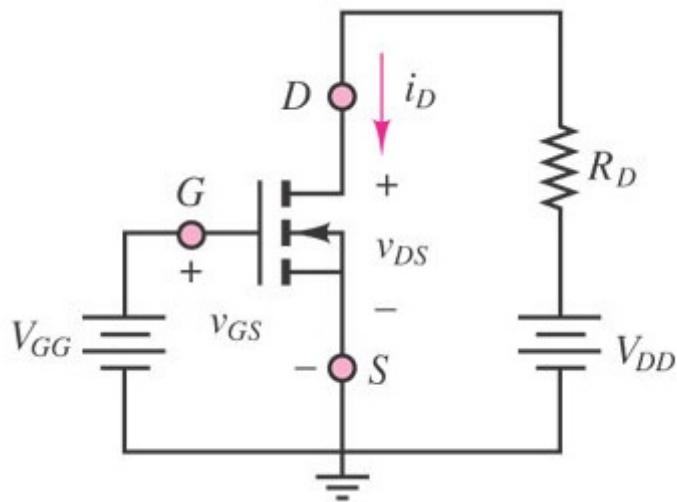
Example 2

Given: $V_T = 2\text{V}$, $K = 20\text{mA/V}^2$; V_{DS} fixed at 1V .

Determine the operating mode and drain current (I_D) when:

a) $V_{GG} = 1.5\text{V}$, b) $V_{GG} = 2.5\text{V}$, c) $V_{GG} = 3.5\text{V}$

How would the answers change if a resistor $R_G = 1\text{k}\Omega$ was added between terminal G and V_{GG} ?



First thing to check: Is _____ ?

When $V_{GG} = 1.5\text{V}$:

$V_{GS} = \underline{\hspace{1cm}} (\underline{\hspace{1cm}} V_T)$

Conclusion: _____

$\Rightarrow I_D = \underline{\hspace{1cm}}$

Example 2 (next)

When $V_{GG} = 2.5V$:

$$V_{GS} = \underline{\hspace{2cm}} (\underline{\hspace{1cm}} V_T)$$

Next thing to check: Is _____?

$$V_{GS} = \underline{\hspace{2cm}} (\underline{\hspace{1cm}} V_T)$$

Conclusion: _____

$$I_D = K (V_{GS} - V_T)^2$$

$$I_D = 20(2.5 - 2)^2$$
$$\Rightarrow I_D = 5\text{mA}$$

When $V_{GG} = 2.5V$:

$$V_{GS} = \underline{\hspace{2cm}} (\underline{\hspace{1cm}} V_T)$$

_____?

$$V_{GS} = \underline{\hspace{2cm}} (\underline{\hspace{1cm}} V_T)$$

Conclusion: _____

$$I_D = K [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

$$I_D = 20[2(3.5 - 2)(1) - (1)^2]$$

$$\Rightarrow I_D = 40\text{mA}$$

If a resistor $R_G = 1k\Omega$ was added between terminal G and V_{GG} :

Example 3

Given: $V_T = 2V$, $K = 20\text{mA/V}^2$, $V_{DS} = 1V$, $V_{GG} = 5V$, and $R_1 + R_2 = 10\text{k}\Omega$

Determine the operating mode and drain current (I_D) when:

a) $R_1 = 4R_2$, b) $R_1 = R_2$, c) $4R_1 = R_2$

Recall that: Gate current is always _____

$$V_{GS} = \frac{R_2}{R_1 + R_2} V_{GG}$$

a) $V_{GS} = 1V$: Operating mode: _____
($I_D = \text{_____}$)

b) $V_{GS} = 2.5V$: Operating mode: _____
($I_D = 5\text{mA}$)

c) $V_{GS} = 4V$: Operating mode: _____
 $I_D = 20[2(4 - 2)(1) - (1)^2] \Rightarrow I_D = 60\text{mA}$

