

EE2000 Logic Circuit Design

Logic Families

Outline

10.1 Timing Parameters of Flip-flips

- Propagation delay, output transition time, minimum pulse width, setup time, hold time

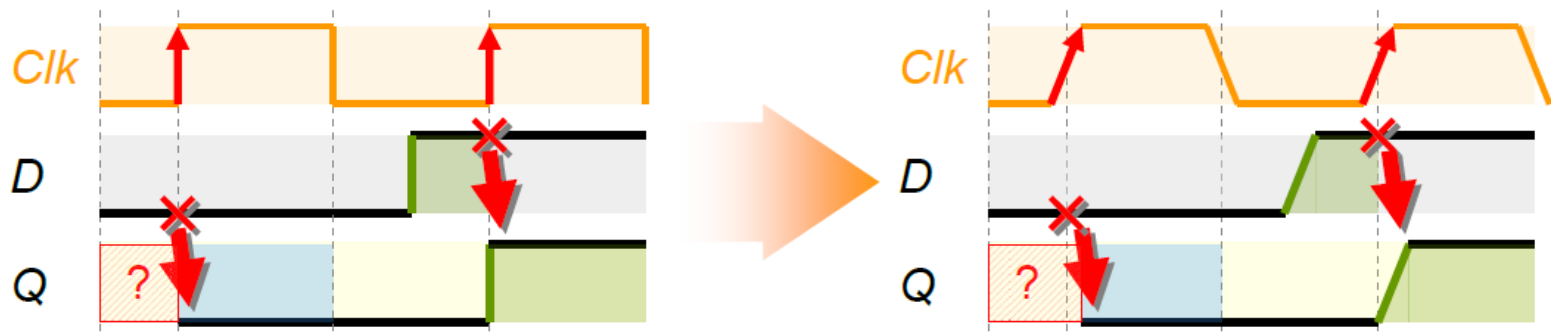
10.2 Electrical Characteristics of Logic Gates

- Logic levels, noise margins, speed of operation, power dissipation, operation temperature, fan-in, fan-out, comparison of logic families

Five Timing Parameters

- 1. Propagation delay
- 2. Output transition time
- 3. Minimum pulse width
- 4. Setup time
- 5. Hold time

Timing diagram of a positive edge-triggered D FF

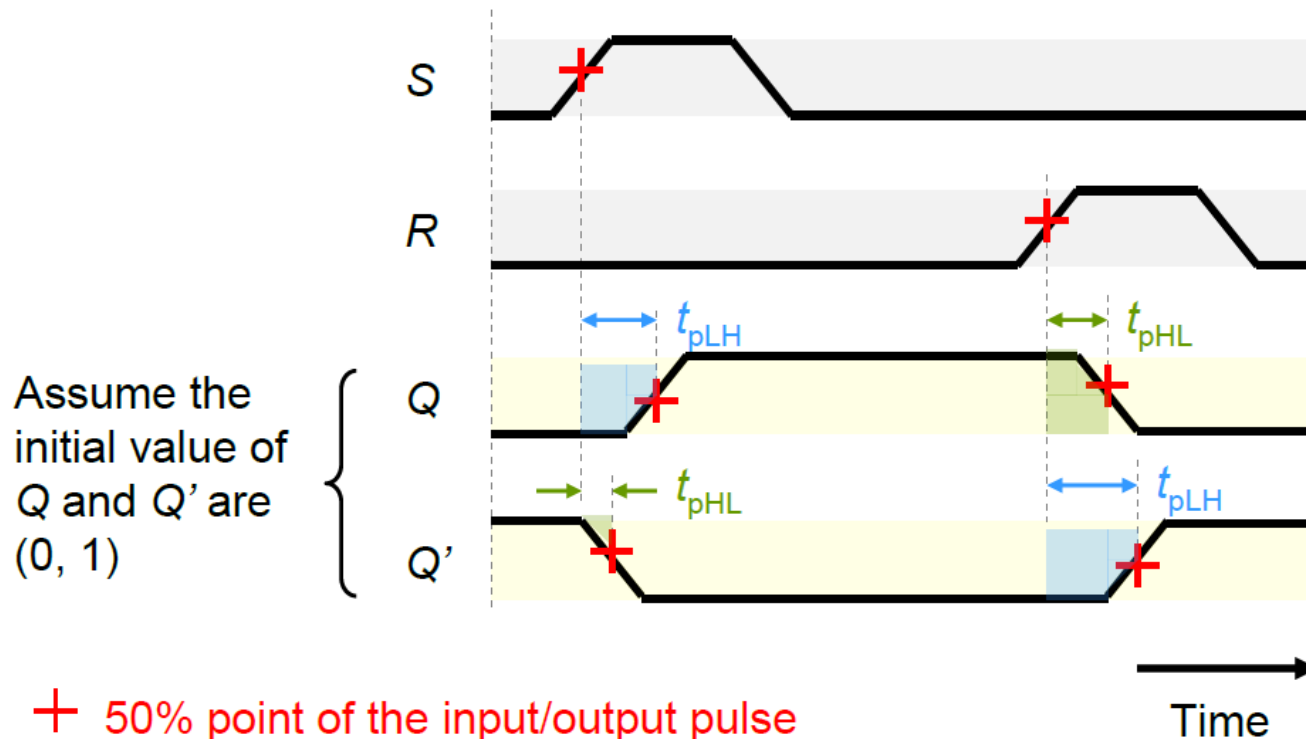


Propagation time and delay

- The amount of time it takes for the output of FF to change its state from a clock trigger (or asynchronous preset or clear)
- Denoted by t_{pHL} and t_{pLH}
 - t_{pHL} : Propagation time from a HIGH to a LOW
 - t_{pLH} : Propagation time from a LOW to a HIGH
- Defined from the 50% point of the input pulse to the 50% point of the output pulse

Example: t_{pHL} and t_{pLH}

- Illustrate the propagation delays in an *SR* latch using timing diagram

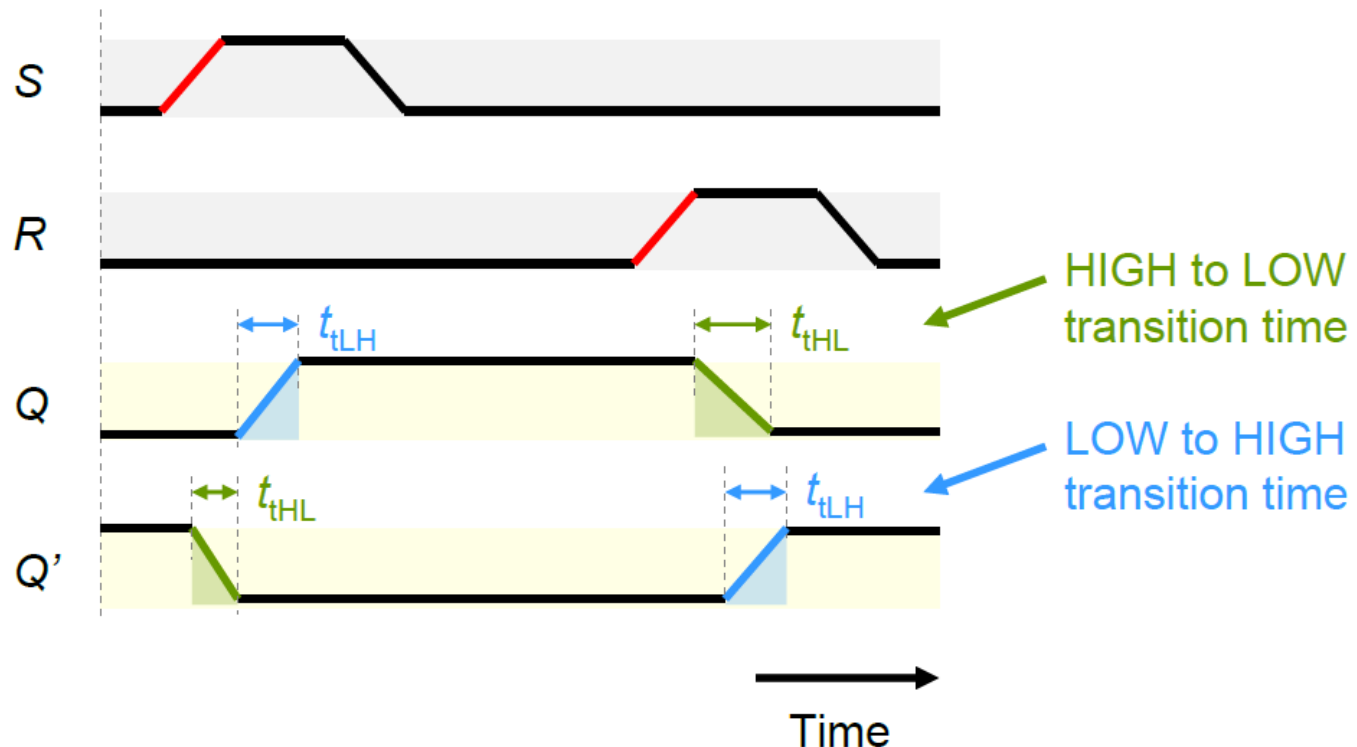


Output Transition Time

- The **rise time** or **fall time** of the output
- Denoted by t_{tHL} and t_{tLH}
 - t_{tLH} : 10% to 90% time, or LOW to HIGH transition time
 - t_{tHL} : 90% to 10% time, or HIGH to LOW transition time

Example: t_{tHL} and t_{tLH}

- Illustrate the output transition time in an *SR* latch using timing diagram

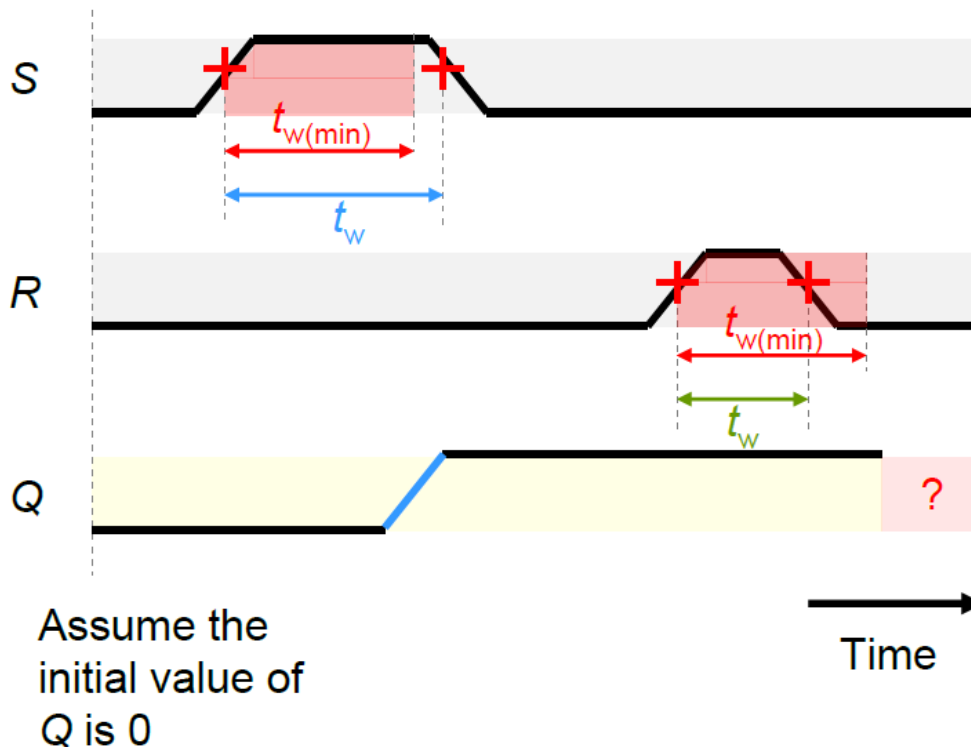


Minimum Pulse Width

- The minimum amount of time that the input signal must be applied in order to produce a correct result
- To insure the device has enough time to capture and response to the input values correctly
- Pulse width is denoted by t_w
- Minimum pulse width is denoted by $t_{w(\min)}$

Example: t_w and $t_{w(\min)}$

- Illustrate the minimum pulse width in an *SR* latch using timing diagram



The pulse width is greater than the min. pulse width. The output is guaranteed.

The pulse width is too short that the output state becomes unpredictable (why?)

Setup Time and Hold Time

■ Setup Time

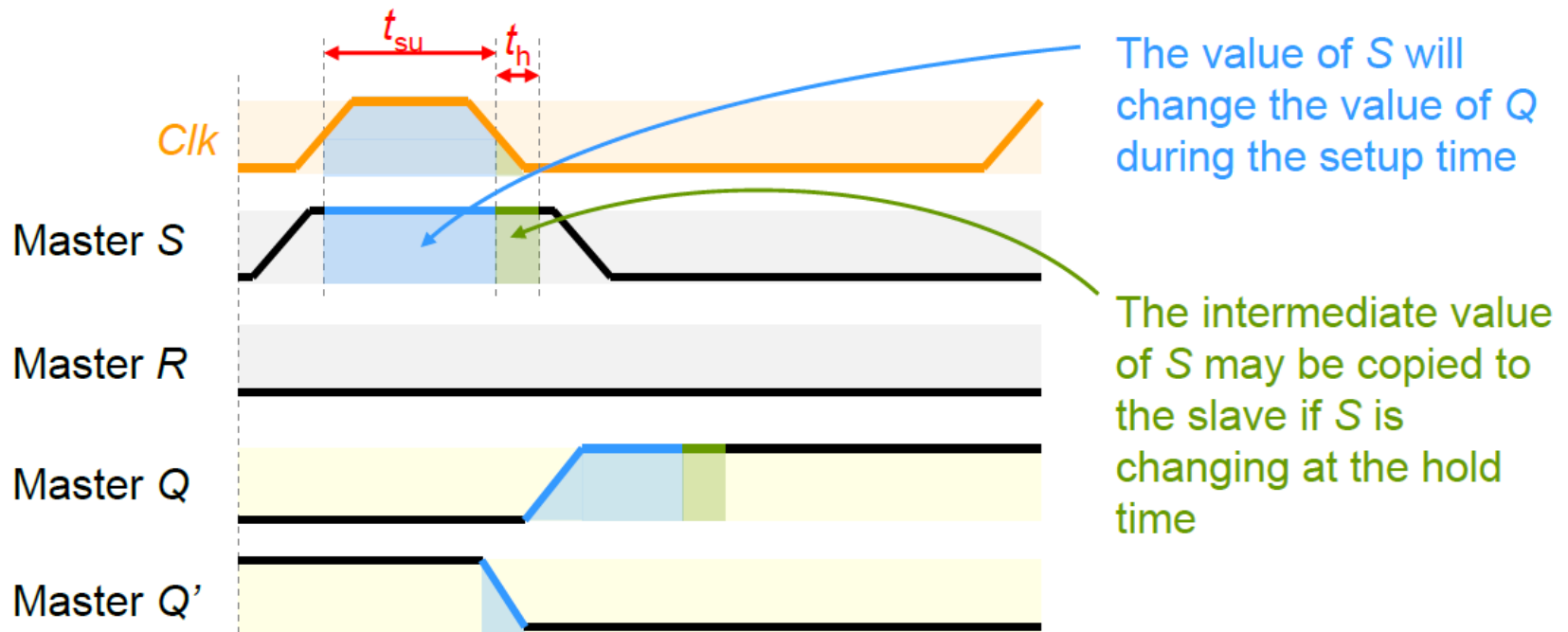
- Denoted by t_{su}
- The minimum time that the input(s) must be maintained at a constant value prior to the occurrence of the clock transition that causes the output to change

■ Hold Time

- Denoted by t_h
- The minimum time that the input(s) must not change after the application of the clock transition that causes the output to change

Example: t_{su} and t_h

- Illustrate the setup and hold time in an positive pulse-triggered (master-slave) *SR* flip-flop



Logic Gate Characteristics

- For practical gates, the following features have to be considered during selection of appropriate gate type to ensure a specified performance
 - Range of voltages correspond to the logic 0 and 1 levels
 - Uncertainty region for these logic levels, i.e. noise margin
 - Switching speed
 - Static and dynamic power dissipation
 - Input and output loading effects
 - Operating temperature
 - Supply voltage limits

Logic Levels

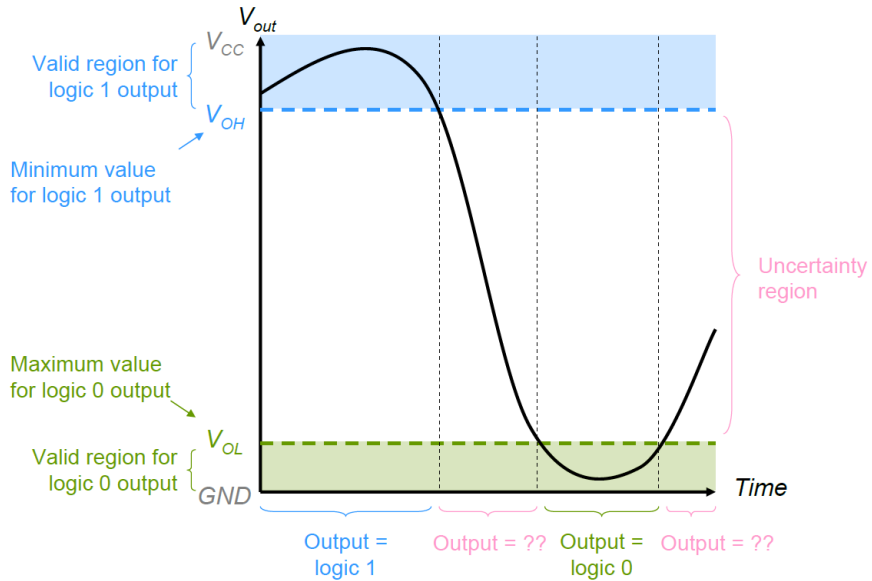
- Ideal logic levels
 - Logic 0: Ground
 - Logic 1: V_{CC}
- For practical gates, the **outputs** voltage have to be defined
 - V_{OH} : the minimum value of output logic 1
 - V_{OL} : the maximum value of output logic 0
 - Uncertainty region: region between V_{OH} and V_{OL}

Logic Levels

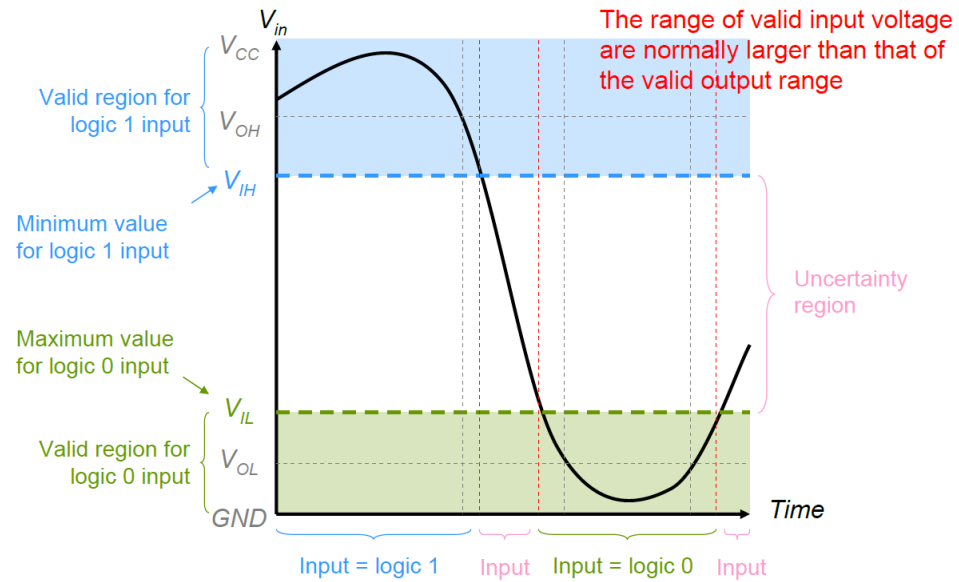
- Similarly for the **inputs**,
 - V_{IH} : the minimum value for input logic 1
 - V_{IL} : the maximum value for input logic 0
 - Uncertainty region: region between V_{IH} and V_{IL}
 - *Input level within this region to a logic gate will not provide a clear output level*
 - *i.e. can either be HIGH (logic 1) or LOW (logic 0)*

Logic Levels

Output Logic Levels: V_{OH} , V_{OL}



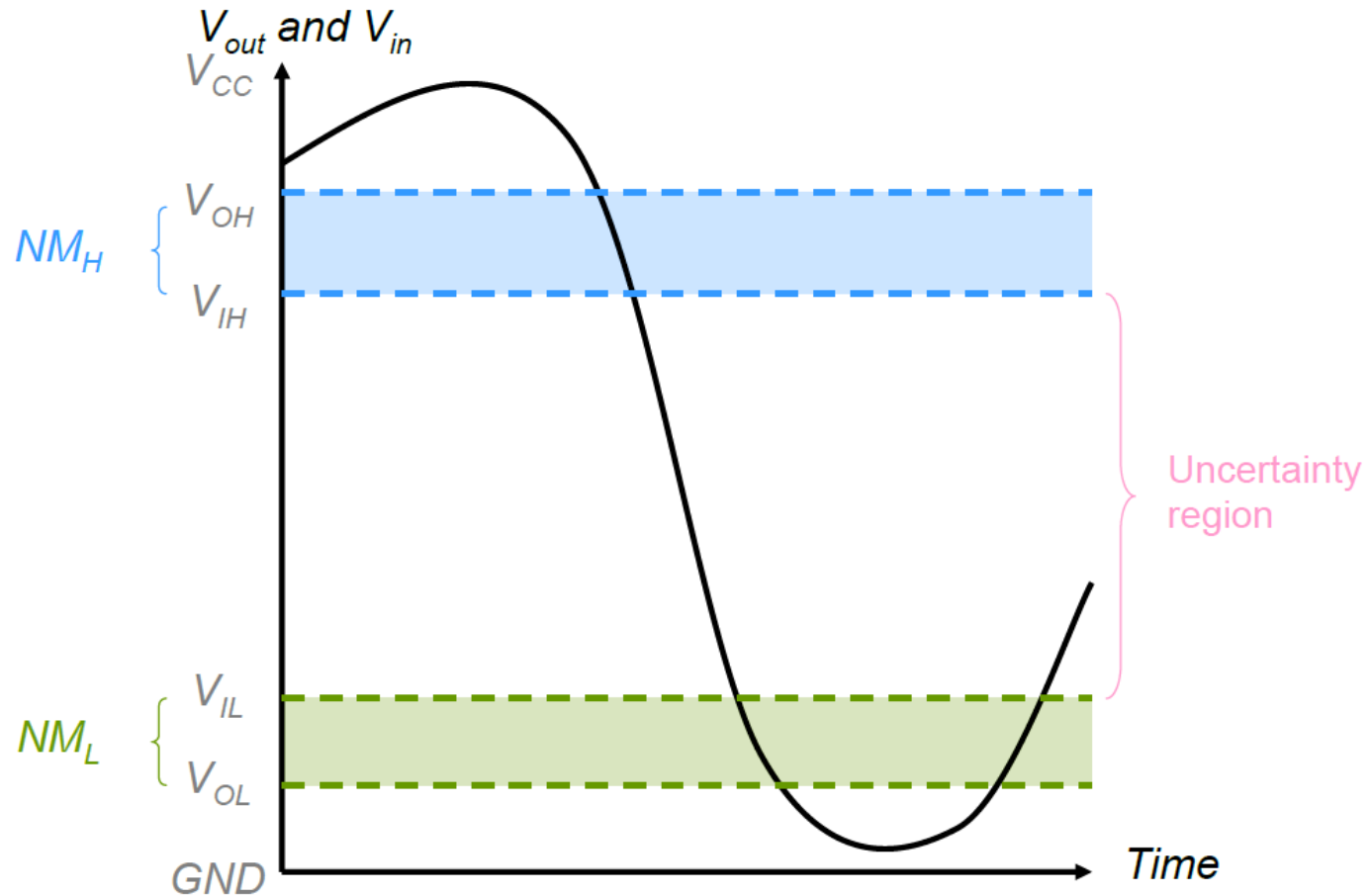
Input Logic Levels: V_{IH} , V_{IL}



Noise Margin

- Noise is **unwanted signal** present in the electric circuit
- Ideally, noise should not alter the logic states
- If the noise level exceeds the margin in the **uncertainty region**, it can trigger the transition
- The margin is known as noise margin
 - $NM_H = V_{OH} - V_{IH}$ (Noise Margin for logic 1)
 - $NM_L = V_{IL} - V_{OL}$ (Noise Margin for logic 0)

Noise Margin: NM_H , NM_L



Speed of Operation

- Speed of operation is determined by
 - 1) Time for a signal to propagate from input to output
 - Denoted by t_{pHL} and t_{pLH} (Defined earlier on)
 - 2) The transition time between states
 - Denoted by t_{tHL} and t_{tLH} (Defined earlier on)
- Cycle time
 - Denoted by t_{cyc}
 - The time required to make two successive cycles of transition
 - Often the reciprocal of the clock frequency
- Delay power product
 - The product of the **propagation delay** and the **power dissipation**
 - Used to measure the gate performance

Power Dissipation

- Static (D.C.) power dissipation
 - The true logic states in a practical gate is not 0V and V_{CC}
 - The difference in these levels contributes to the static power dissipation
- Dynamic power dissipation
 - During the change of state, the transition time is not instantaneously
 - Hence, it contributes the dynamic power dissipation
- The total static and dynamic consumption
 - A measurement of the efficiency
 - A key factor during the design to avoid overheating

Operating Temperature

- Most commercial logic gates operate between 0° and 70°C
- For some special gates, temperature range can be extended to operate between -40° and 100°C
 - e.g. military products
- Most data supply by manufacturer are produced at room temperature (i.e. 25°C)

Fan-in and Fan-out

■ Fan-in

- The no. of inputs that a gate can accept without affecting its normal performance
- Constrained by the no. of inputs provided by the gate

■ Fan-out

- The no. of gates that a gate can **drive** without degrading its performance
- Directly related to the input and output resistance of the gates
- Different logic gate types will provide different fan-out values

Comparison of logic families

Most commonly used logic families are: TTL, CMOS and ECL.

Generally speaking,

- 1) ECL has the lowest propagation delay and thus comprises the fastest logic circuits available.
- 2) TTL has the smallest delay power product.
- 3) CMOS has the lowest power dissipation and is used for LOW power consumption circuits, such as calculator and digital watches.

Comparison of logic families

Propagation delay

		Typical (ns)		Worst case (ns)	
Logic	Subfamily	LH	HL	LH	HL
TTL	74	12	7	22	15
TTL	74L	35	31	60	60
TTL	74H	5.9	6.2	10	10
TTL	74S	4	5	7	8
TTL	74LS	8	8	15	15
TTL	74AS	1	1	4	4
TTL	74ALS	3	2	11	8
CMOS	4000B	75	75	150	150
CMOS	74HC	10	10	18	18
ECL	10K/100K	0.2	0.2	0.6	0.6

Comparison of logic families

Power dissipation

			Power dissipation (1 NAND)	
Logic	Subfamily		Typical	Worst case
TTL	74		10 mW	29 mW
TTL	74L		1 mW	3 mW
TTL	74H		21 mW	50 mW
TTL	74S		19 mW	47 mW
TTL	74LS		4 mW	6 mW
TTL	74AS		16 mW	23 mW
TTL	74ALS		2 mW	4 mW
CMOS	4000B		2 mW	Freq. Dependent
CMOS	74HC	static	1 mW	12 mW
		active	550 mW	Freq. Dependent
CMOS	74HCT	static	2 mW	20 mW
		active	1 mW	Freq. Dependent
ECL	10K		30 mW	35 mW
ECL	100K		45 mW	50 mW

Family	Description	Propagation delay (ns)	Toggle speed (MHz)	Power per gate @1 MHz (mW)	Typical supply voltage V (range)	Introduction year	Remarks
RTL	Resistor–transistor logic	500	4	10	3.3	1963	the first CPU built from integrated circuits (the Apollo Guidance Computer) used RTL.
DTL	Diode–transistor logic	25		10	5	1962	Introduced by Signetics, Fairchild 930 line became industry standard in 1964
CMOS	AC/ACT	3	125	0.5	3.3 or 5 (2-6 or 4.5-5.5)	1985	ACT has TTL Compatible levels
CMOS	HC/HCT	9	50	0.5	5 (2-6 or 4.5-5.5)	1982	HCT has TTL compatible levels
CMOS	4000B/74C	30	5	1.2	10V (3-18)	1970	Approximately half speed and power at 5 volts
TTL	Original series	10	25	10	5 (4.75-5.25)	1964	Several manufacturers
TTL	L	33	3	1	5 (4.75-5.25)	1964	Low power
TTL	H	6	43	22	5 (4.75-5.25)	1964	High speed
TTL	S	3	100	19	5 (4.75-5.25)	1969	Schottky high speed
TTL	LS	10	40	2	5 (4.75-5.25)	1976	Low power Schottky high speed
TTL	ALS	4	50	1.3	5 (4.5-5.5)	1976	Advanced Low power Schottky
TTL	F	3.5	100	5.4	5 (4.75-5.25)	1979	Fast
TTL	AS	2	105	8	5 (4.5-5.5)	1980	Advanced Schottky
TTL	G	1.5	1125 (1.125 GHz)		1.65 - 3.6	2004	First GHz 7400 series logic
ECL	ECL III	1	500	60	-5.2(-5.19 - -5.21)	1968	Improved ECL
ECL	MECL I	8		31	-5.2	1962	first integrated logic circuit commercially produced
ECL	ECL 10K	2	125	25	-5.2(-5.19 - -5.21)	1971	Motorola
ECL	ECL 100K	0.75	350	40	-4.5(-4.2 - -5.2)	1981	
ECL	ECL 100KH	1	250	25	-5.2(-4.9 - -5.5)	1981	