

EE2000 Logic Circuit Design

EE2000 – Assignment 2

Q1. Figure Q1 shows the block diagram of a circuit which has four inputs A, B, C, D and one output Y. It operates according to the following rules:

- (i) If the inputs A, B, C and D have more 0s than 1s, the circuit will generate an odd parity bit for the inputs.
- (ii) If the number of 0s and 1s of the inputs are equal, the machine will generate an even parity for the inputs.
- (iii) If there is only one 0, the output is equal to 1.
- (iv) The output of the remaining case(s) is (are) 1.

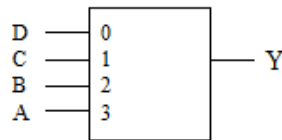


Figure Q1. Block diagram of a 4 inputs to 1 output circuit.

- (a) Tabulate the truth table of the circuit.
- (b) By considering the minimum SOP expression of the truth table, design the circuit using minimum number of logic gates. You can use AND, OR and NOT gates only.

Q1. Answer

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

[20 marks]

	CD			
AB	1			
			1	
		1	1	1
			1	

$$Y = \overline{A} \overline{B} \overline{C} \overline{D} + BCD + ACD + ABD + ABC$$

or

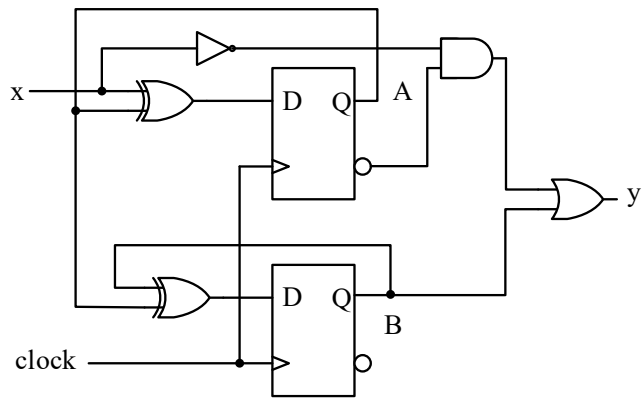
$$Y = \overline{A + B + C + D} + BCD + ACD + ABD + ABC$$

[10 marks]

Circuit (not show) [10 mark]

Q2. The following diagram shows a sequential circuit.

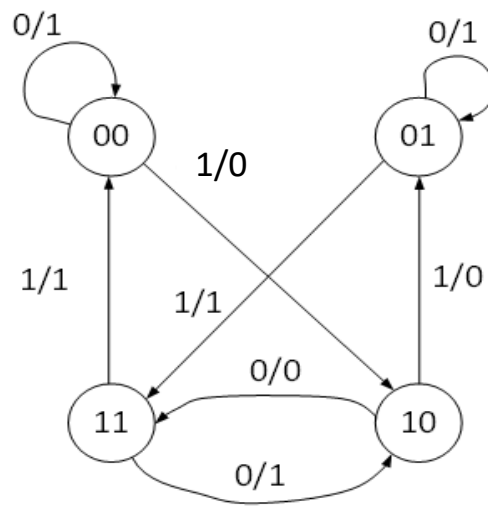
- (i) Derive the state diagram.
- (ii) Find the state transition Boolean functions.



Q2. ANSWER

$$D_A = x \oplus A, D_B = A \oplus B, y = x'A' + B$$

PS	Input	FFs' excitation		NS	O/P
AB	x	D_A	D_B	AB	y
00	0	0	0	00	1
00	1	1	0	10	0
01	0	0	1	01	1
01	1	1	1	11	1
10	0	1	1	11	0
10	1	0	1	01	0
11	0	1	0	10	1
11	1	0	0	00	1



[table 15 marks, state diagram 15 marks]

(ii)

	AB			
x			1	1
	1	1		

$$A_{n+1} = A_n x' + A_n' x = A_n \oplus x$$

	AB			
x		1		1
		1		1

$$B_{n+1} = A_n' B_n + A_n B_n' = A_n \oplus B_n$$

[A 15 marks, B 15 marks]