

EE3220: Assignment 2

Question 1

The memory system requirement for a S3C44B0X based board with *different data bus width* for different memory banks is shown as follows:

ROM: 16M bytes using 2M x 8-bit chips for Bank0 with 16-bit data bus width
SRAM: 16M bytes using 2M x 16-bit chips for Bank6 with 32-bit data bus width
SDRAM: 16M bytes using 4 Banks x 1M x 8-bit chips for Bank7 with 16 bit data bus width

- (i) Find the chip count for all the memory components.
- (ii) Design the address table for the memory system.
- (iii) Determine the Boolean expressions of ALL the chip select signals.
- (iv) Based on standard decoder chips to design the *decoder circuit* for the ROM, SRAM and SDRAM, and draw the circuits.
- (v) Draw the connection diagram of SRAM chip to the CPU control signals (see examples in pages 26 & 27 of Chapter 9).

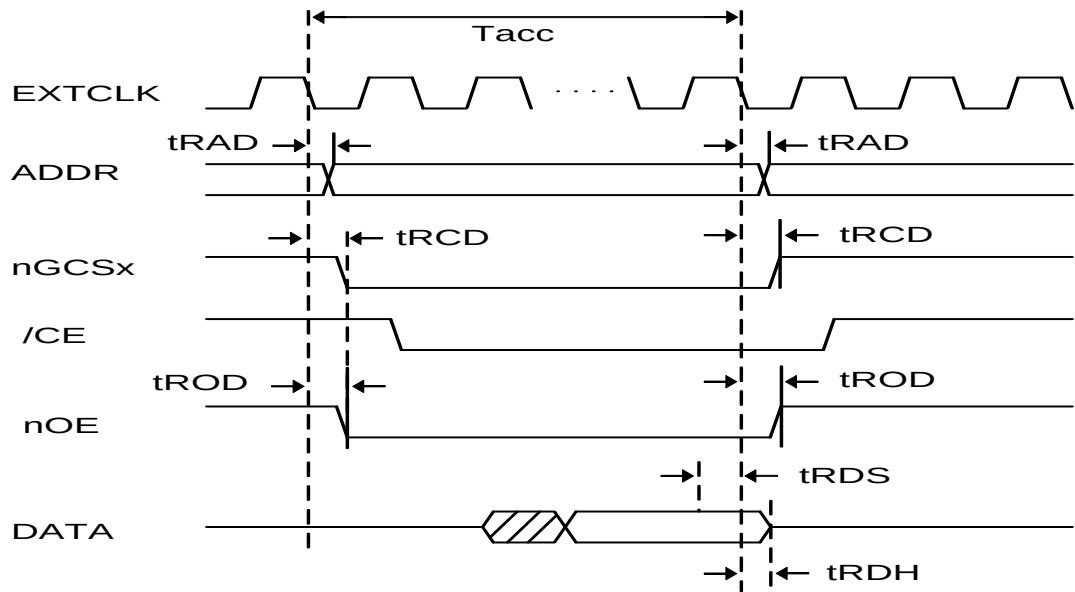
Question 2

Determine for the number of Tacc (with Tacs, Tcos, Toch and Tcah = 0) cycles required for S3C44B0X to carry out valid read/write operations when operated at 50 MHz with SRAM SRAM-CY62167 (70 ns). Complete the timing diagrams for both read and write cycles for submission. Assuming that the address decoder circuit consists of one single chip 74LV138 with delay of 15 ns.

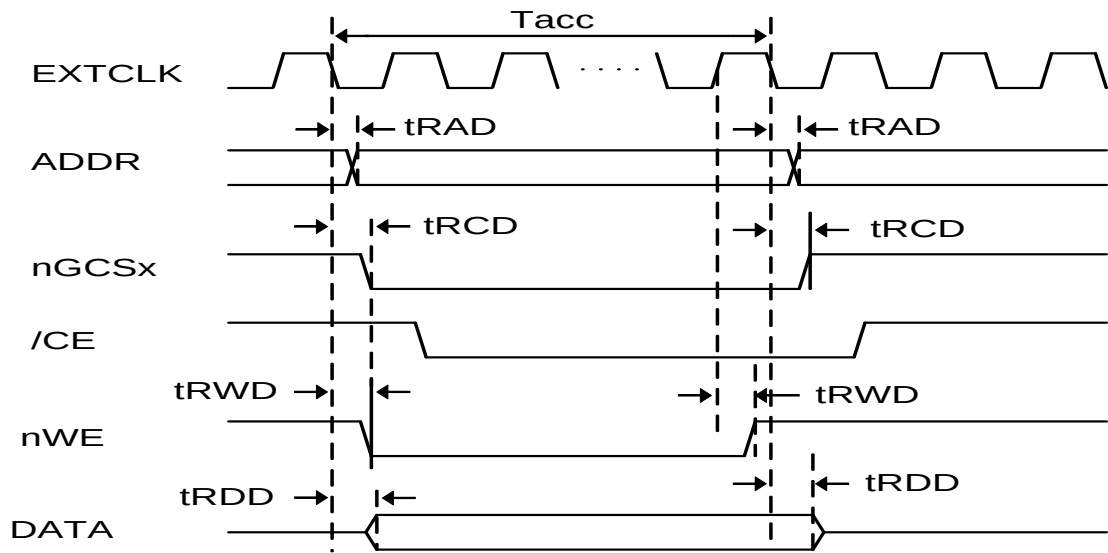
Question 3

Determine the relevant register setting for interfacing SDRAM MT48LC8M8A2 (speed grade – 75) to S3C44B0X with 2 M x 8 x 4 banks configuration. Draw the circuit diagram as well. S3C44B0X is operated at 50 MHz.

S3C44B0X READ CYCLE:



S3C44B0X WRITE CYCLE:



Q1 (i)

No. of ROM chips required: $16M/2M = 8$

No. of SRAM chips required: $16M/4M = 4$

No. of SDRAM chips required: $16M/4M = 4$

(ii)

Device	nGCS	Address lines															
		24	23	22	21	20	19	18	17	...	06	05	04	03	02	01	00
ROM0	0(000)	0	0	0	X	X	X	X	X	...	X	X	X	X	X	X	-
ROM1	0(000)	0	0	1	X	X	X	X	X	...	X	X	X	X	X	X	-
ROM2	0(000)	0	1	0	X	X	X	X	X	...	X	X	X	X	X	X	-
ROM3	0(000)	0	1	1	X	X	X	X	X	...	X	X	X	X	X	X	-
SRAM0	6(110)	0	0	X	X	X	X	X	X	...	X	X	X	X	X	-	-
SRAM1	6(110)	0	1	X	X	X	X	X	X	...	X	X	X	X	X	-	-
SDRAM0	7(111)	0	0	X	X	X	X	X	X	...	X	X	X	X	X	X	-
SDRAM1	7(111)	0	1	X	X	X	X	X	X	...	X	X	X	X	X	X	-

(iii)

$$\text{ROM_0_CS} = \text{nGCS0} \overline{A_{24}} \overline{A_{23}} \overline{A_{22}}$$

$$\text{ROM_1_CS} = \text{nGCS0} \overline{A_{24}} \overline{A_{23}} A_{22}$$

$$\text{ROM_2_CS} = \text{nGCS0} \overline{A_{24}} A_{23} \overline{A_{22}}$$

$$\text{ROM_3_CS} = \text{nGCS0} \overline{A_{24}} A_{23} A_{22}$$

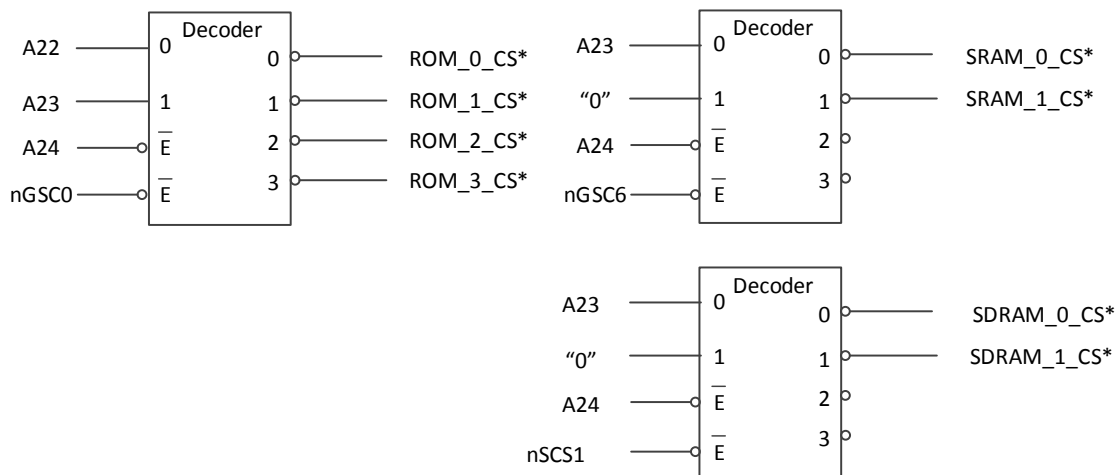
$$\text{SRAM_0_CS} = \text{nGCS6} \overline{A_{24}} \overline{A_{23}}$$

$$\text{SRAM_1_CS} = \text{nGCS6} \overline{A_{24}} A_{23}$$

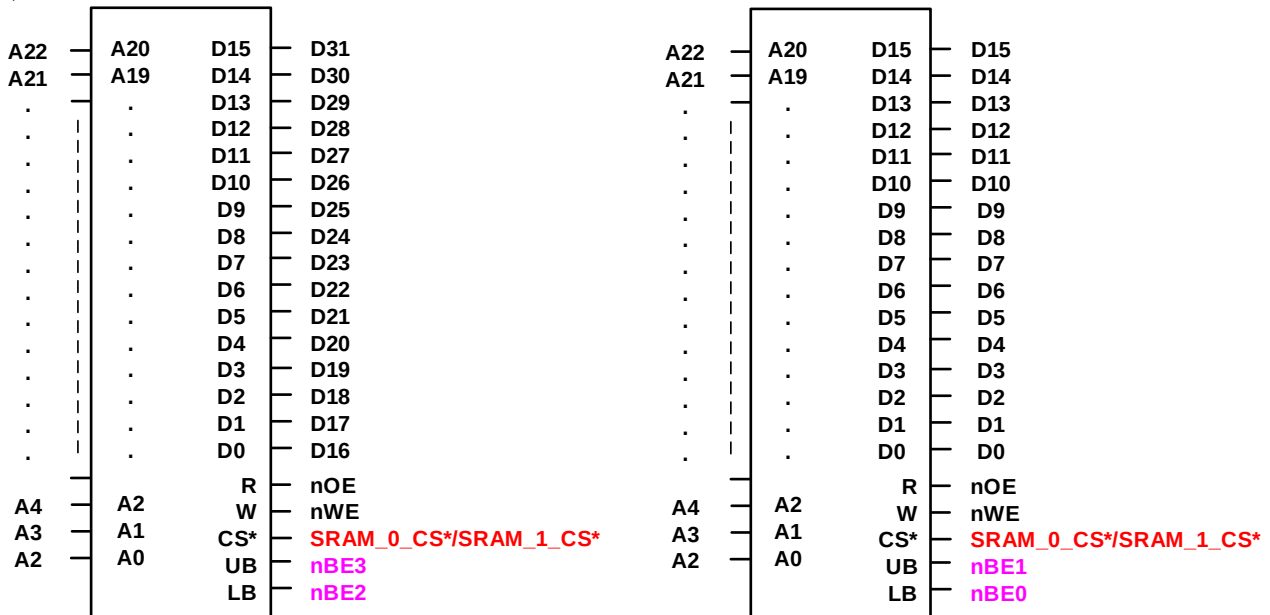
$$\text{SDRAM_2_CS} = \text{nSCS1} \overline{A_{24}} \overline{A_{23}}$$

$$\text{SDRAM_3_CS} = \text{nSCS1} \overline{A_{24}} A_{23}$$

(iv)



(v)



Q2:

READ CYCLE:

$$t_{RAD} + t_{AA} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$\text{i.e., } T_{acc} \geq (t_{RAD} + t_{AA} + t_{RDS}) / t_{cyc}$$

CPU running at 50 MHz ($t_{cyc} = 20 \text{ ns}$):

$$T_{acc_{min}} \geq (12 + 70 + 1) / 20 \geq 4.15 = 5$$

Condition checking (i):

$$(i) \ t_{RCD} + t_{DEC} + t_{ACS} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$11 + 15 + 70 + 1 = 97 \rightarrow T_{acc} \geq 97 / 20 = 5$$

Condition checking (ii):

$$(ii) \ t_{ROD} + t_{DOE} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

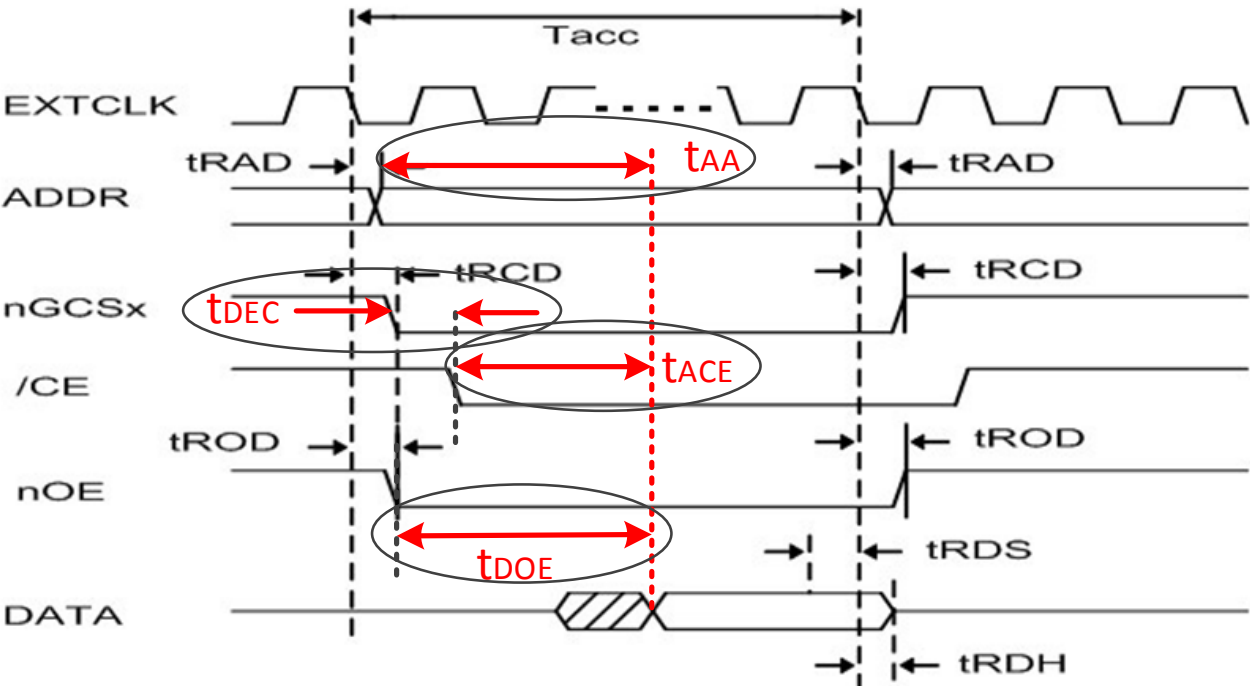
$$11 + 35 + 1 = 47 \rightarrow T_{acc} \geq 47 / 20 = 3$$

$$\text{i.e } T_{acc} = \text{Max}(5, 5, 3) = 5$$

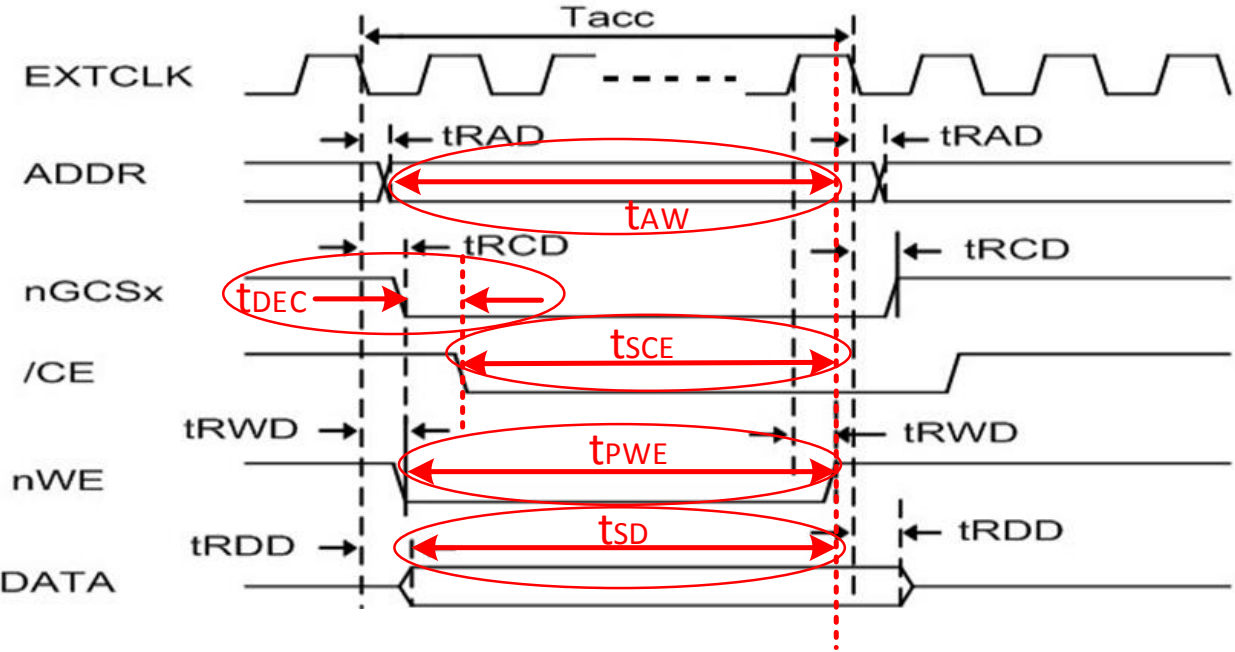
			N=5	Req'd
tWC	$N \times T_{cyc} + t_{RAD} - t_{RAD}$	$N \times 20$	100	70
tSCE	$(N-0.5) \times T_{cyc} + t_{RWD} - t_{RCD} - t_{DEC}$	$(N-0.5) \times 20 + 14 - 11 - 15 = (N-0.5) \times 20 - 12$	78	60
tAW	$(N-0.5) \times T_{cyc} + t_{RWD} - t_{RAD}$	$(N-0.5) \times 20 + 14 - 12 = (N-0.5) \times 20 + 2$	92	60
tWPE	$(N-0.5) \times T_{cyc} + t_{RWD} - t_{RWD}$	$(N-0.5) \times 20$	90	45
tSD	$(N-0.5) \times T_{cyc} + t_{RWD} - t_{RDD}$	$(N-0.5) \times 20 + 14 - 14 = (N-0.5) \times 20$	90	30

Final Tacc = 5

S3C44B0X READ CYCLE:



S3C44B0X WRITE CYCLE:



Q3:

(i) $t_{cyc} = 1/50\text{MHz} = 20\text{ns}$

$t_{RCD} = 20/20 = 1 \text{ clock} \rightarrow 00$

SCAN (9-bit: CA0-CA8) $\rightarrow 01$

MT = 11

Bankcon6(or 7) = 1 1xxx xxxx xxxx xxxx 0001

(ii)

Enable refresh : REFEN = 1

CBR/Auto Refresh: TREFMD = 0

Precharge time = 20ns $\rightarrow 20/20 = 1 \text{ clock} \rightarrow t_{RP} = 00$

Minimum RC = 66ns $\rightarrow 64/20 = 4 \text{ clocks} \rightarrow t_{RC} = 00$

Tchr (N/A)

Refresh period = $64\text{ms}/4096 = 15.625\mu\text{s}$

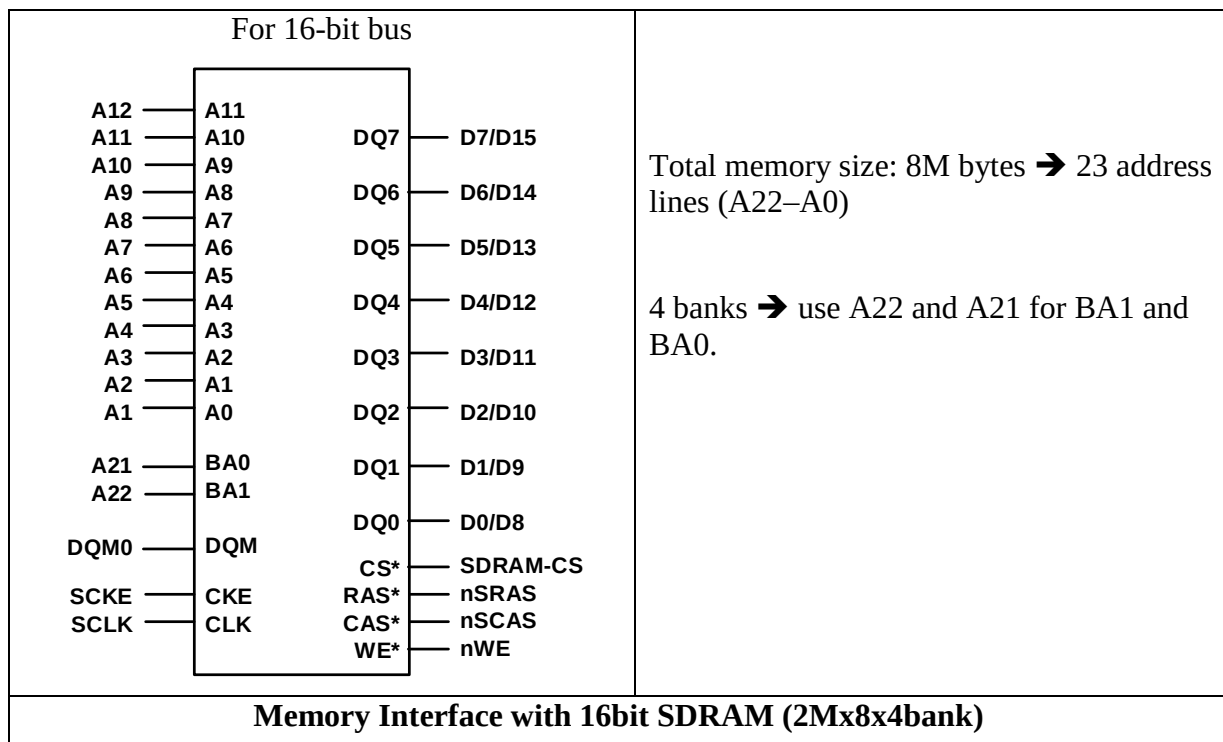
Refresh counter = $2^{11} + 1 - 50 \times 15.625 = 1267.5 \approx 1268 = 0x4F4$

Thus, **rREFRESH = 0b1 0 00 00 00 0000 10011110100**

= 0b1000 0000 0000 0100 1111 0100

= 0x008004F4

(iii)



For 8-bit bus, A0 $\rightarrow$ A0, For 32-bit bus, A0 $\rightarrow$ A2