

EE 2000 Logic Circuit Design
Semester A 2014

Tutorial 2

- Q1: (a) Complete the following table by encoding the decimal number 215 in the following format. Please show the bit configuration and count the number of bits used.

	Bit representation	No. of bit used
Binary	1101 0111	8
8421 Code	0010 0001 0101	12
2421 Code	0010 0001 0101	12
Excess-3 Code	0101 0100 1000	12
2-of-5 Code		
ASCII		21

- (b) There are many ways to represent decimal digits on computers. For the weighted code, you have learnt 8421 code, 5421 code and 2421 code. The numbers in the code name indicated the weights of each digit. Can you guess how will (8, 4, -2, -1) code look like?

Please complete the following table:

Decimal	BCD (8, 4, -2, -1) Code	Decimal	BCD (8, 4, -2, -1) Code
0	0000	5	1011
1	0111	6	1010
2	0110	7	1001
3	0101	8	1000
4	0100	9	1111

- (c) State some properties of this code?

self- complementing code

- Q2. The following words are to be transmitted by a vertical parity system. Horizontal parity is to be odd; vertical parity is to be even. An all-1s character marks the end of the block (EOB). Calculate the necessary parity bits and list the complete sequence that is involved in the transmission.

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1 0 1 0 1 1 0
0 1 0 1 1 1 1
1 1 0 0 0 0 0
0 0 1 1 0 1 0
1 1 0 1 0 1 0
1 1 1 1 1 1 1

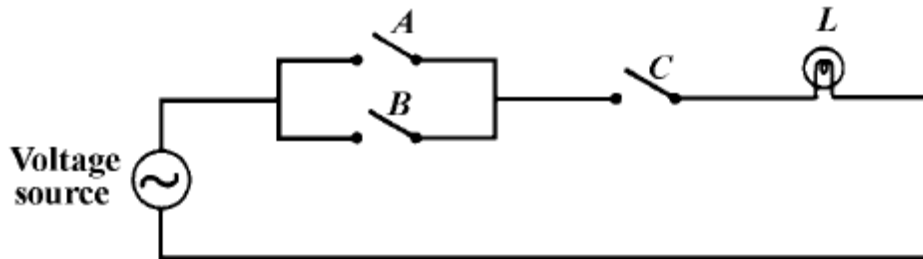
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Q3: The following block of data is received from the transmission system with a vertical parity system. Horizontal parity is to be odd; vertical parity is to be even. An all-1s is EOB.

0	1	0	1	0	1	0	0
1	0	1	0	1	0	1	1
0	1	0	0	1	1	0	1
0	0	1	1	1	1	1	0
1	0	1	0	0	0	1	0
1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	0
0	0	1	1	1	1	0	1

- Find any parity failure.
- Correct the error, if possible.
- Assuming that there are three bits in error, show several possible locations.

Q4: Express the switching circuit shown in the figure in binary logic notation:



Q5: Draw the logic circuit diagram of the Boolean function $f(x, y, z) = (x' + y')(x + y + z')$ using AND, OR, NOT gates. The diagram should correspond exactly to the equation. Assume that the complements of the inputs are not available.

Q6: Simplify the expression using Boolean algebra

- $x'y' + xy + x'y$
- $x' + xy + xz' + xy'z'$
- $[AB'(C+BD) + A'B']C$
- $A'BC + AB'C' + A'B'C' + AB'C + ABC$

Q7: Using DeMorgan's theorem, convert the following Boolean expressions to equivalent expressions that (i) have only OR and complement operations, and show that the functions can be implemented with NOR gates only; (ii) have only AND and complement operations, and show that the functions can be implemented with NAND gates only.

- $f = \bar{x}\bar{y} + \bar{x}z + \bar{y}z$
- $f = (y + \bar{z})(x + y)(\bar{y} + z)$