

EE3122: Analogue Circuit Fundamentals

Operational Amplifier (Op-amp)

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Introduction

1940s

- The original concept of the operational amplifier (op-amp) came from the field of analog computers.
- It is derived from the concept of an extremely high gain, differential-input amplifier, the operating characteristics of which were determined by the feedback elements used with it.
- Different analog operations could be implemented by changing the types and arrangement of feedback elements.
- Early operational amplifiers used basic hardware of that era - the vacuum tube.

Introduction

1960s

- Significantly widespread use of op-amps did not really begin until the 1960s.
- Solid-state techniques were applied to op-amp circuit design.
- In the mid-1960s the first integrated circuit (IC) op-amp was produced which is well known as **μA709**.
- In 1968, **μA741** was produced (Lojek, 2007).

Some Op-amp models



Figure 1. GAP/R's K2-W: a vacuum-tube op-amp (1951).

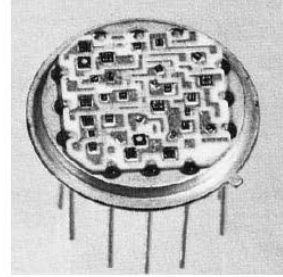


Figure 4. ADI's HOS-050: a high speed hybrid IC op-amp (1979).

1950s

1960s

1970

Recent trends

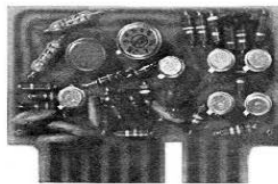


Figure 2. GAP/R's model P45: a solid-state, discrete op-amp (1961).

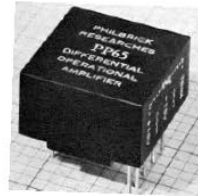


Figure 3. GAP/R's model PP65: a solid-state op-amp in a potted module (1962).



Figure 5. An op-amp in a modern mini Dual-in-line Package (DIP).

Example: 741 Opamp



Figure 5. An op-amp in a modern mini Dual-in-line Package (DIP).

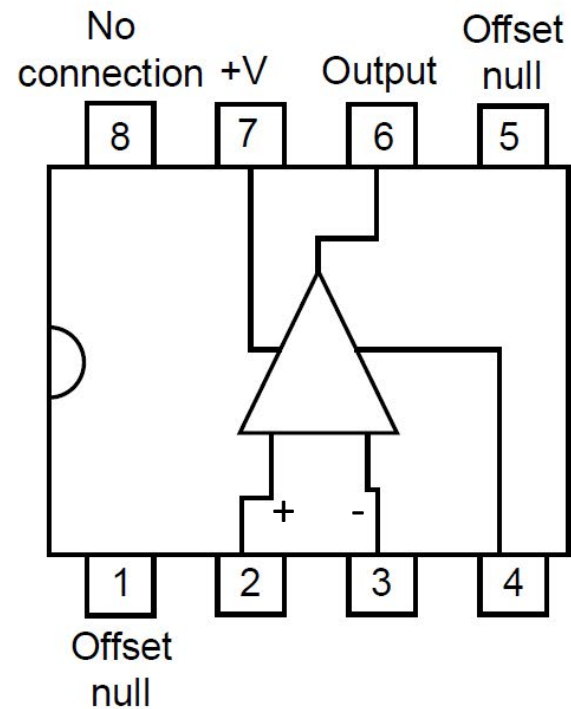


Figure 6. A typical 8 pin DIP op-amp integrated circuit.

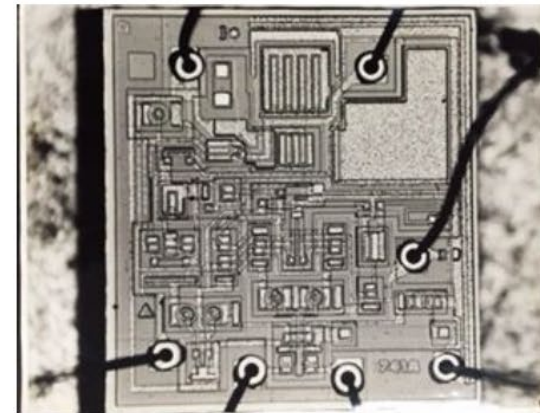


Figure 7. A micro-photograph of the 741 op-amp.

How are the circuits related to what we have learnt?

741 Opamp: What's inside?

What is inside the op-amp?

Basically we may divide an op-amp into three main stages:

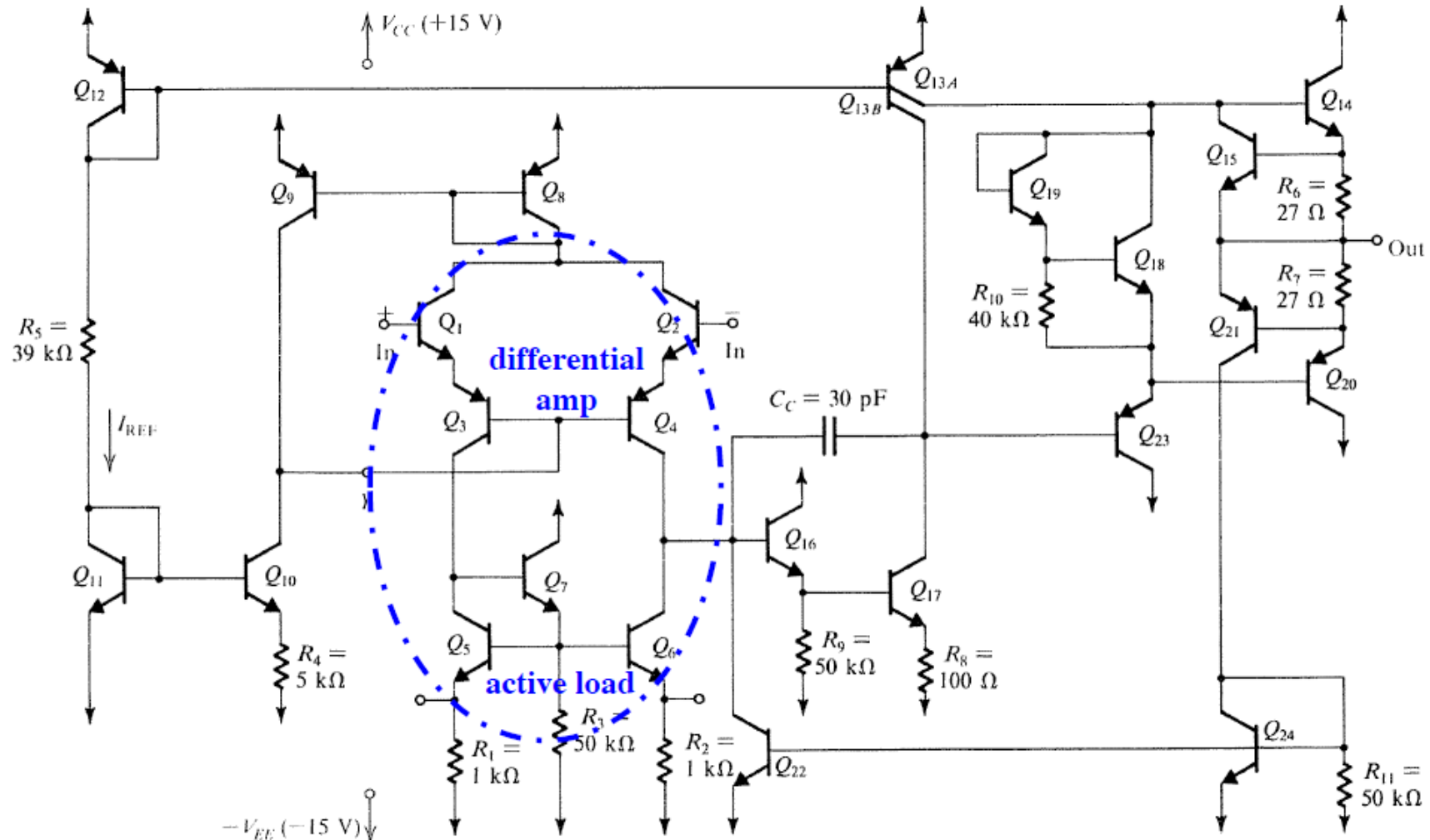
Main functional parts

1. Input stage (Differential Amplifier (DE))
2. Second stage (gain stage) (Common Emitter (CE))
3. Output stage (Emitter follower (EF) based Class AB)

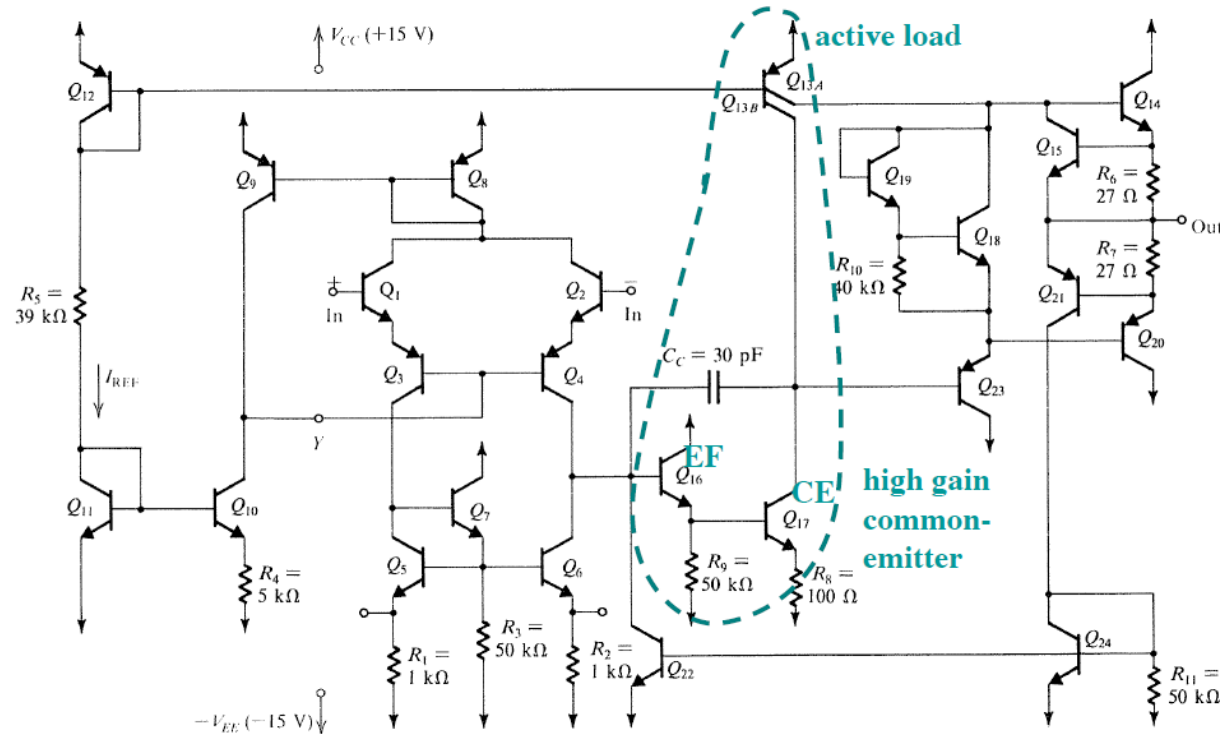
Other parts

- Bias circuit
- Short-circuit protection circuit

741 Opamp: Input Stage



741 Opamp: Second Stage



Q16 is an emitter follower, providing high input resistance for the stage so as to minimize its loading effect.

Q17 is a common-emitter amplifier, loaded by Q13B.

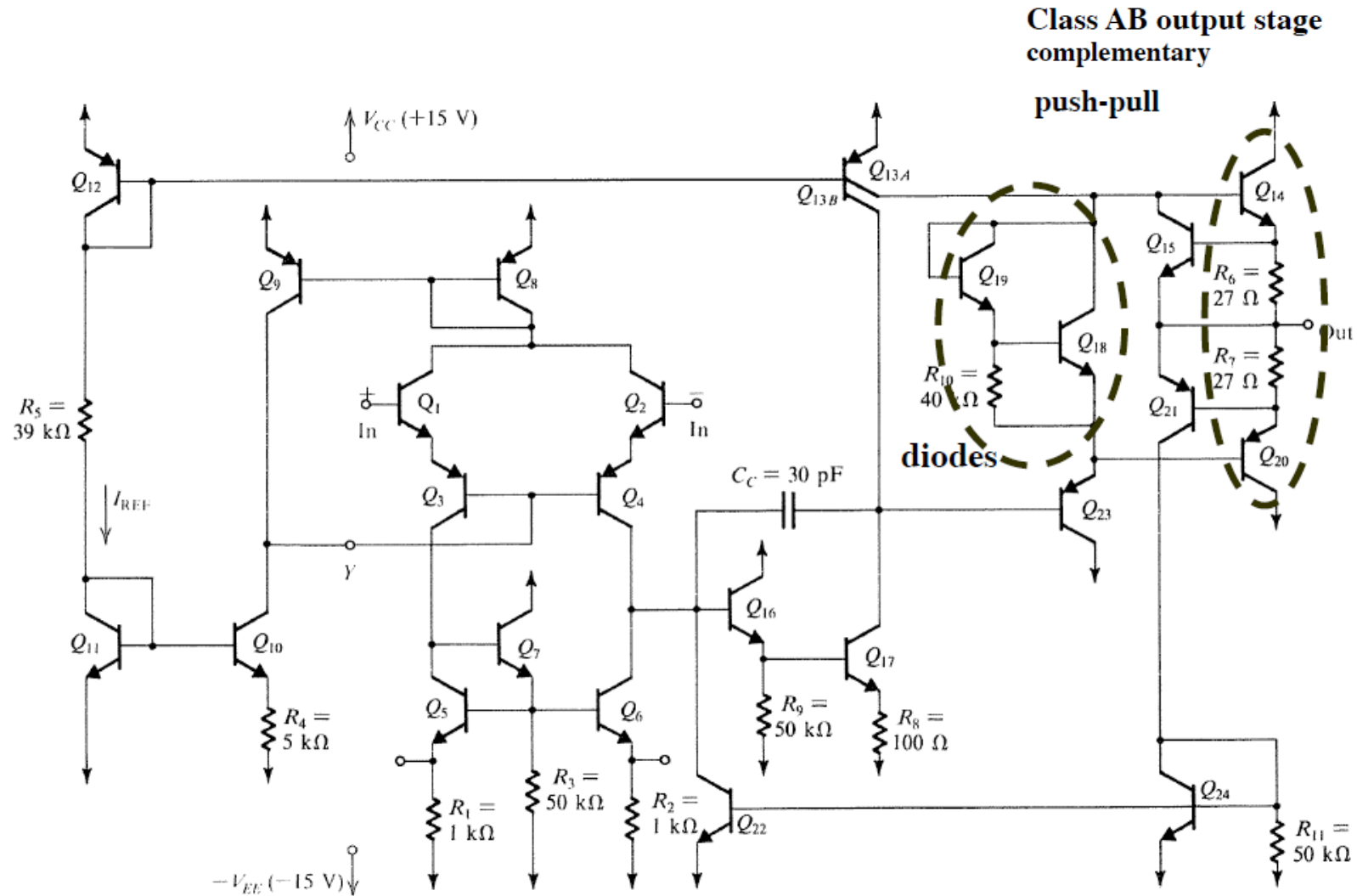
Q13B is a current mirror and serves as active load.

The gain is

$$\text{GAIN}_{\text{second stage}} \approx g_{m,17} r_{o,13B}$$

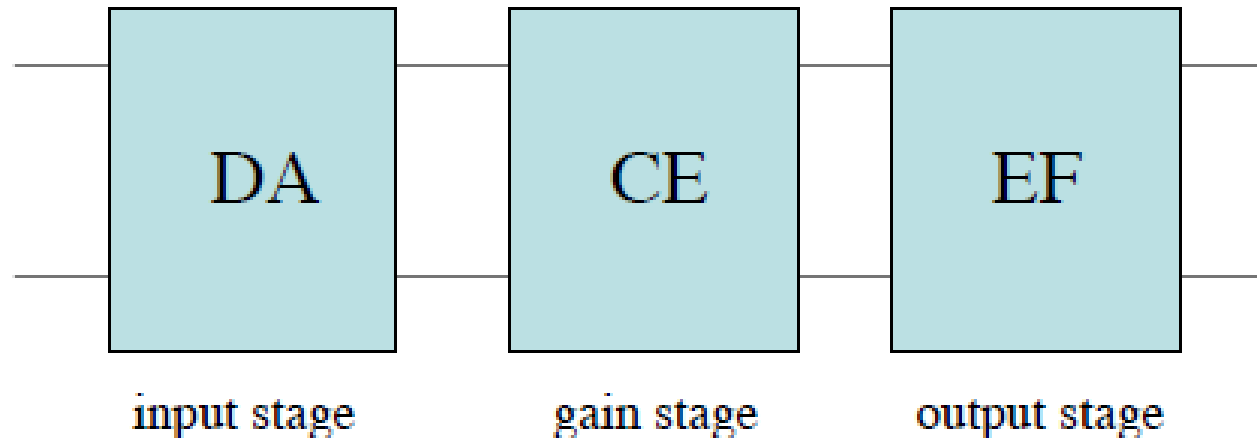
Note the capacitor C_C . This is called internal compensation cap and is used for maintaining stability in when the op-amp is used in a feedback configuration. We'll revisit this issue later when we study feedback and stability.

741 Opamp: Output Stage



Summary: Internal circuits

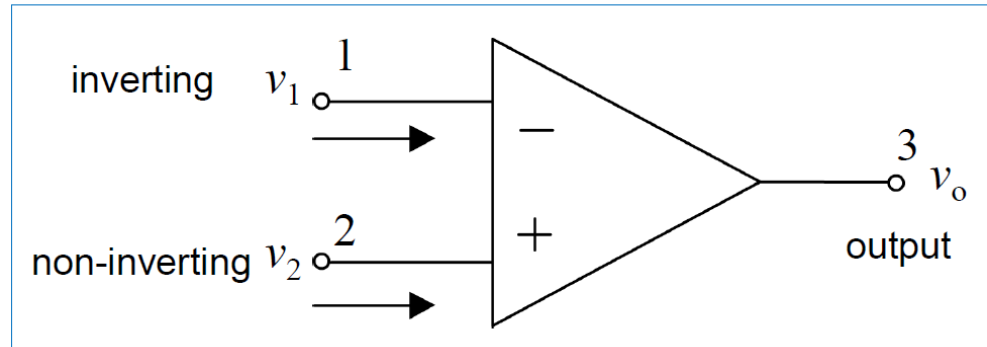
- Input stage: Differential amplifier (DA) of high input resistance, e.g., MOSFET/JFET pair
- Second stage: Common-emitter (CE) stage with **active load**
- Output stage: Emitter follower (EF) with low output resistance



More details in Appendix

Op-amp Terminals

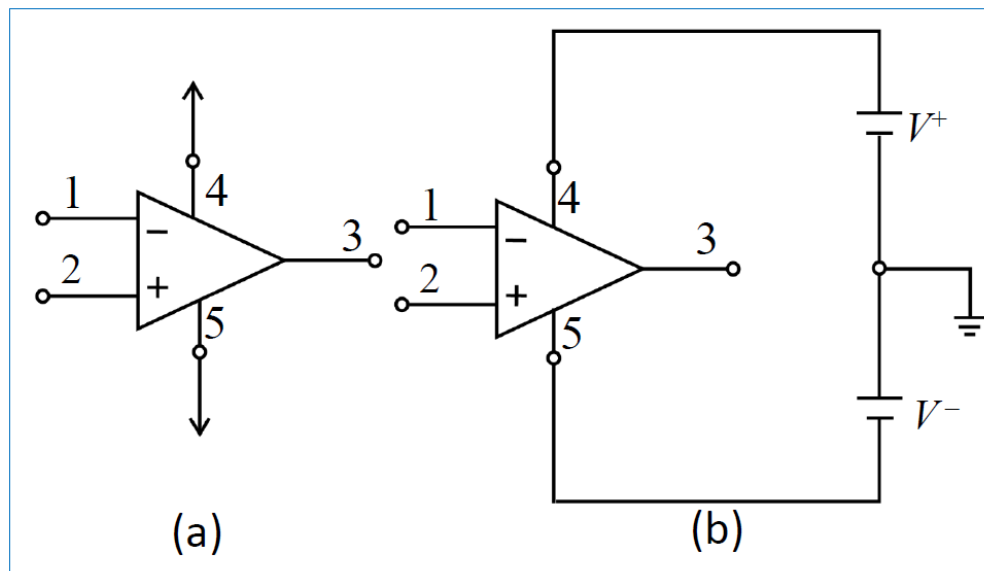
From a signal point of view, op-amp has three terminals: two input terminals for differential signal input and one single-ended output terminal.



$$v_o = A_{\text{VOL}} v_{\text{id}}$$
$$= A_{\text{VOL}} (v_2 - v_1)$$

where

$$v_{\text{id}} = (v_2 - v_1)$$



Most IC op-amps require two power supplies V^+ and V^- sometimes given as $[+V_{\text{CC}}; V_{\text{CC}}; V_{\text{DD}}]$ and $[-V_{\text{CC}}; V_{\text{EE}}; V_{\text{SS}}]$

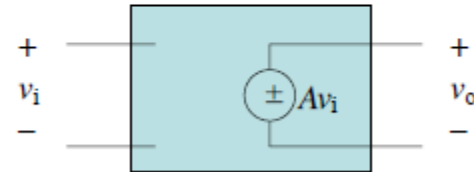
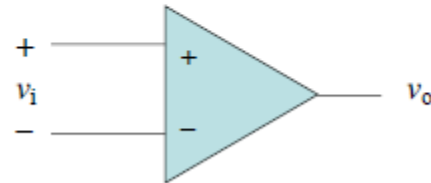
Ideal Op-amp

In EE2301/2005, you have studied the op-amps and simple op-amp circuits, assuming that the op-amp is an ideal element satisfying the following conditions:

Output resistance = 0 (perfect output stage)

Input resistance = ∞ (perfect input stage)

Differential voltage gain = ∞



Multiply $v_2 - v_1$ by a number A_{voL} (open-loop voltage gain) to cause $A_{\text{voL}}(v_2 - v_1)$ to appear at the output terminal.

$$\begin{aligned} v_o &= A_{\text{voL}} (v_2 - v_1) \\ &= A_{\text{voL}} v_{\text{id}} \end{aligned}$$

The real op-amp has a very large gain, A_{voL} , but not infinite.

Ideal Op-amp: Properties

- i. The voltage gain is infinite i.e. $A_{\text{voL}} = \infty$.

This implies that with finite output voltage, the required differential input is zero.

Negative Feedback

$$v_{\text{id}} = (v_2 - v_1) = \frac{v_o}{A_{\text{voL}}} \rightarrow 0$$

as $A_{\text{voL}} \rightarrow \infty$ and $v_o \neq \infty$ since the output is finite.

- ii. The input differential resistance is infinite, $R_{\text{id}} = R_{\text{in}} = \infty$.

Ideal op-amp does not draw any input current; the signal current into terminal 1 and terminal 2 are both zero.

Ideal Op-amp: Properties

- iii. The output resistance is zero, $R_o = 0$.

The output voltage at terminal 3 with respect to the voltage at the input terminals is always

$A_{voL}(v_2 - v_1) = A_{voL}v_{id}$; independent of the current that may be drawn from output terminal into a load if the load current is finite, $|I_{R_L}| < \infty$.

- iv. The bandwidth is infinite, $BW = \infty$.

This implies that there will be no phase shift between the input and output signals.

- v. There is zero input offset voltage, $v_{IO} = 0$. This implies that $v_o = 0$ if $v_{id} = 0$.

Ideal Op-amp: Properties

vi. Slew rate, $SR = \infty$.

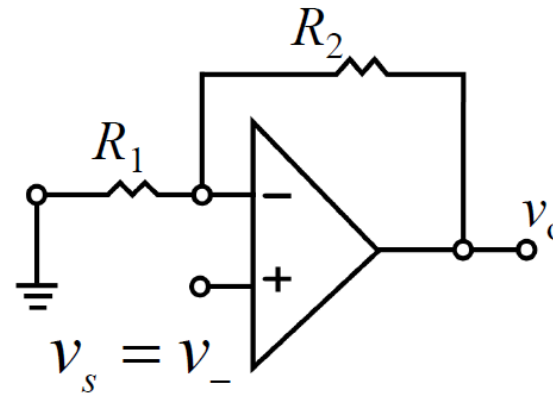
However, slew rate is defined as the maximum rate of change of the output voltage, and therefore,

$$SR > \left. \frac{dv_o}{dt} \right|_{\max} = \infty$$

Example: Perform Mathematical Operations

Examples of Negative Feedback:

Negative Feedback
Non-inverting Gain Amplifier



$$v_s = v_+ = v_- = v_{R_1}$$

$$\frac{v_{R_1}}{R_1} = i_{R_1}$$

$$v_{R_2} = i_{R_2} \times R_2$$

$$\text{But } i_{R_1} = i_{R_2} \because I_- = I_+ = 0$$

$$\therefore v_{R_2} = \frac{v_{R_1}}{R_1} \times R_2 = \frac{v_s}{R_1} \times R_2$$

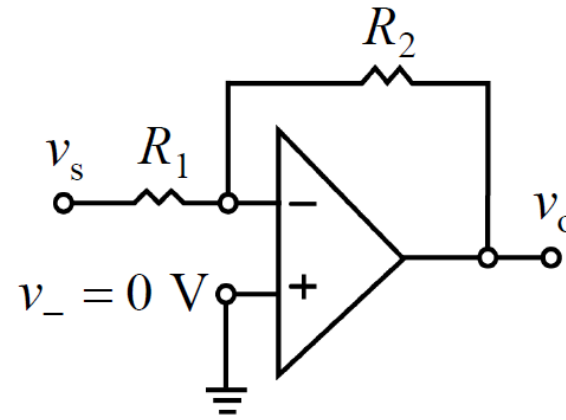
$$v_o = v_{R_1} + v_{R_2} = v_s + \frac{v_s}{R_1} \times R_2$$

$$\frac{v_o}{v_s} = 1 + \frac{R_2}{R_1} = A_{\text{VCL}}$$

Example: Perform Mathematical Operations

Examples of Negative Feedback:

Negative Feedback
Inverting Gain Amplifier



$$v_- = v_+ = 0$$

$$\frac{v_s}{R_1} = i_{R_1}$$

$$v_{R_2} = i_{R_2} \times R_2$$

$$\text{But } i_{R_1} = i_{R_2} \because I_- = I_+ = 0$$

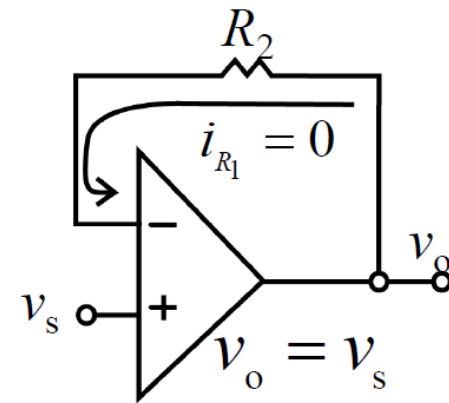
$$\begin{aligned} v_o &= -v_{R_2} = -i_{R_2} \times R_2 \\ &= -i_{R_1} \times R_2 = -\frac{v_s}{R_1} \times R_2 \end{aligned}$$

$$\frac{v_o}{v_s} = -\frac{R_2}{R_1} = A_{vCL}$$

Example: Perform Mathematical Operations

Examples of Negative Feedback:

Negative Feedback
Non-inverting Unity Gain Amplifier



Voltage
Buffer

$$\begin{aligned}v_s &= v_+ = v_- = v_o \\v_o &= v_- + (i_- \times R_2) \\&= v_+ + (i_- \times R_2) \\&= v_s + (i_- \times R_2) \\&= v_s \quad \because i_- = 0\end{aligned}$$

Alternatively,

$$\begin{aligned}\frac{v_o}{v_s} &= 1 + \frac{R_2}{R_1} = 1 + \frac{R_2}{\infty} \\&= 1 + 0 \\&= 1 = A_{vCL}\end{aligned}$$

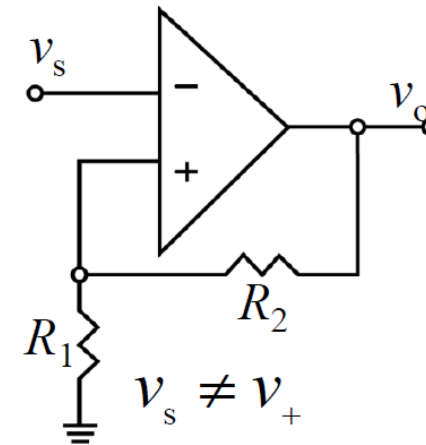
As $i_- = 0$, $v_{R_2} = 0$

Hence, R_2 has
no effect, and
can be shorted
for convenience.

Example: Perform Mathematical Operations

Examples of Positive Feedback:

Note: Output is in Non-linear Region and Input Differential is not Zero



$$v_s = v_-$$

$$v_o = -V_{CC} \text{ for } v_- > v_+$$

$$\therefore v_+ = -V_{CC} \times \frac{R_1}{R_1 + R_2} \left(\begin{array}{l} \text{a potential divided voltage} \\ \text{of the output voltage, } -V_{CC} \end{array} \right)$$

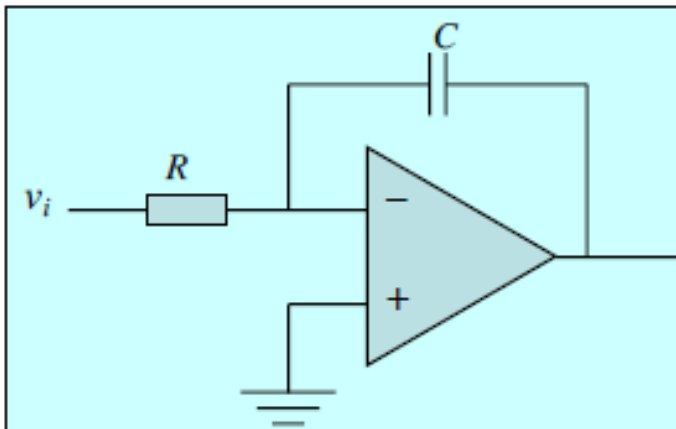
$$v_o = +V_{CC} \text{ for } v_- < v_+$$

$$\therefore v_+ = +V_{CC} \times \frac{R_1}{R_1 + R_2} \left(\begin{array}{l} \text{a potential divided voltage} \\ \text{of the output voltage, } +V_{CC} \end{array} \right)$$

Comparator

Example: Perform Mathematical Operations

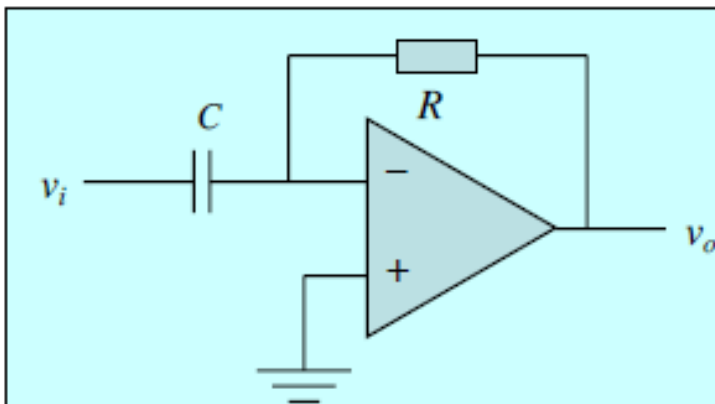
More examples



$$v_i = Ri \quad \text{and} \quad C \frac{dv_o}{dt} = -i$$

$$v_o = -\frac{1}{CR} \int_0^t v_i dt + v_{o,\text{init}}$$

This is the integrator.

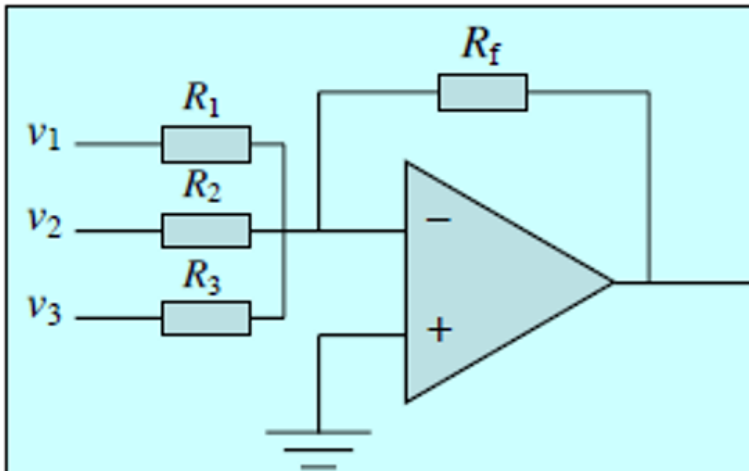


$$C \frac{dv_i}{dt} = i \quad \text{and} \quad -v_o = iR$$

$$v_o = -CR \frac{dv_i}{dt}$$

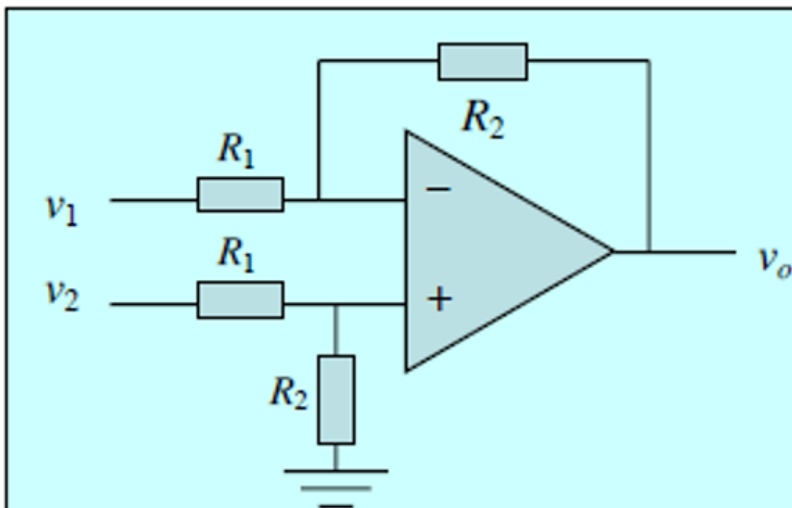
This is the differentiator (theoretically).
In practice, this circuit won't work!!!

Example: Perform Mathematical Operations



$$v_o = - \left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3 \right)$$

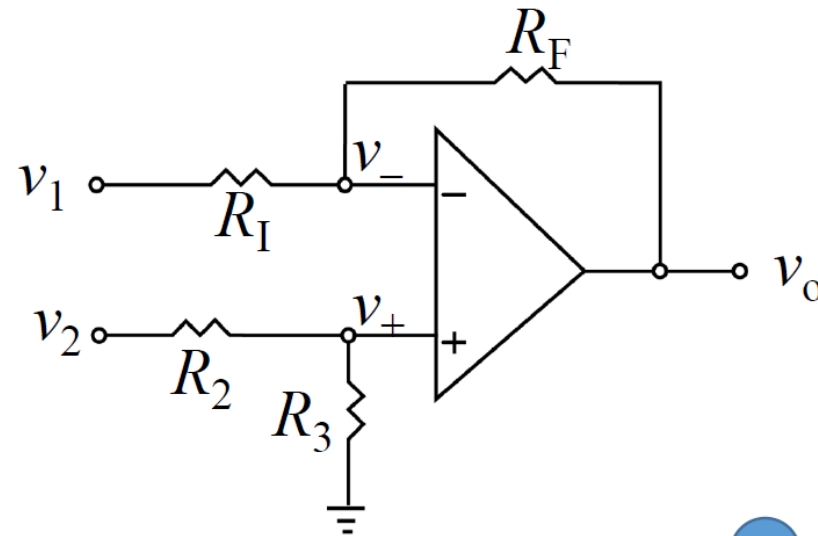
This is the summing amplifier.



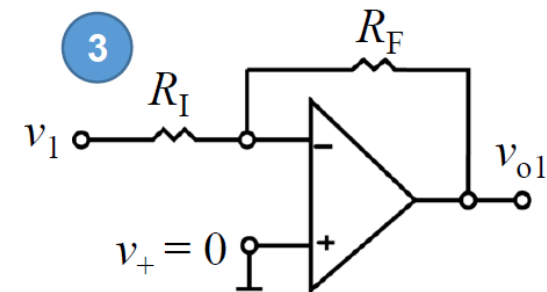
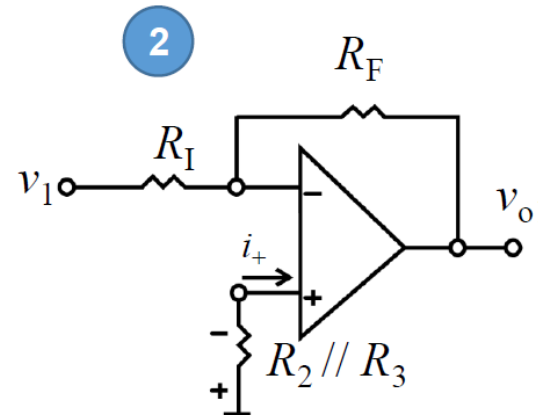
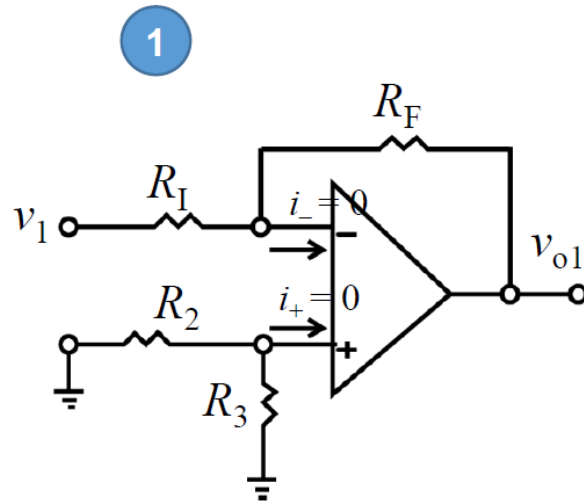
$$v_o = \frac{R_2}{R_1} (v_2 - v_1)$$

This is the difference amplifier.

Scaling subtractor or Difference Amp

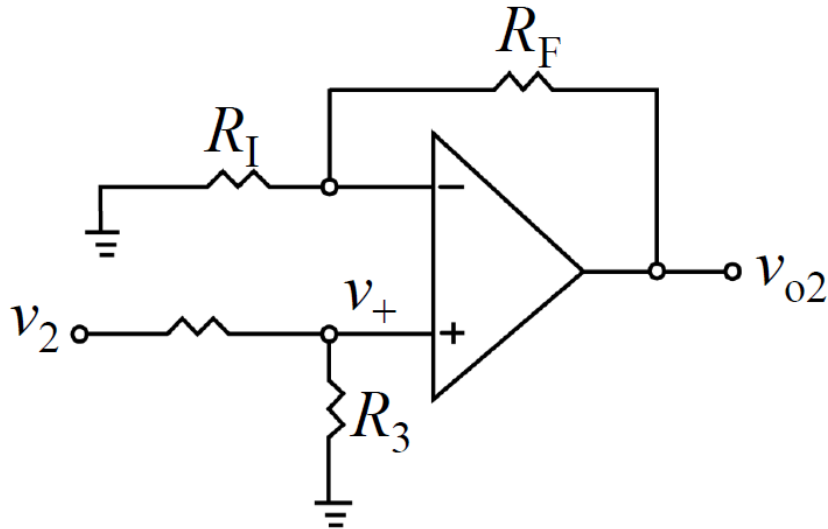


i.



Scaling subtractor or Difference Amp

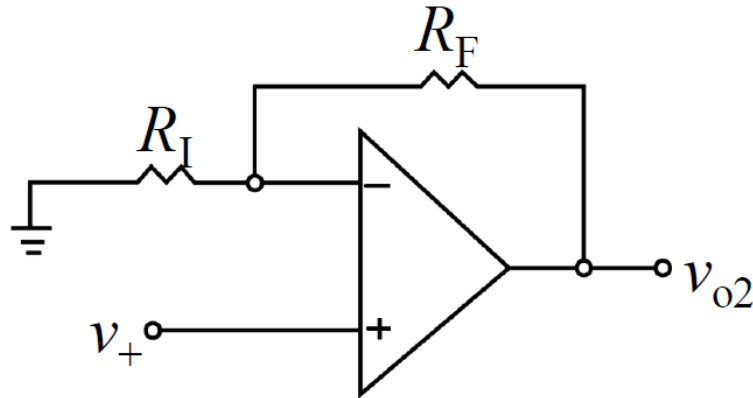
ii.



Non-inverting amplifier

$$v_{o2} = \left(\frac{R_3}{R_2 + R_3} \right) \left(\frac{R_F + R_I}{R_I} \right) v_2$$

$$v_+ = \left(\frac{R_3}{R_2 + R_3} \right) v_2$$



Scaling subtractor or Difference Amp

By using Linear Superposition Principle:

$$\begin{aligned} v_o &= v_{o1} + v_{o2} \\ &= \left(-\frac{R_F}{R_I} \right) v_1 + v_2 \left(\frac{R_3}{R_2 + R_3} \right) \left(\frac{R_F + R_I}{R_I} \right) \end{aligned}$$

$$\begin{aligned} \text{If } \frac{R_F}{R_I} = \frac{R_3}{R_2}, \text{ then } v_o &= -\frac{R_F}{R_I} v_1 + \frac{R_F}{R_I} v_2 \\ &= \frac{R_F}{R_I} (v_2 - v_1) \end{aligned}$$

Special Case

When $R_F = R_3$ and $R_I = R_2$ it is simply called,

Difference Amplifier with a gain of $\frac{R_F}{R_I}$.

This scaling subtractor gives an output that is proportional to the difference between the two inputs.

For $R_F = R_I = R_3 = R_2$, then $v_o = v_2 - v_1$.

The circuit is called **subtractor**.

Op-amp nonidealities

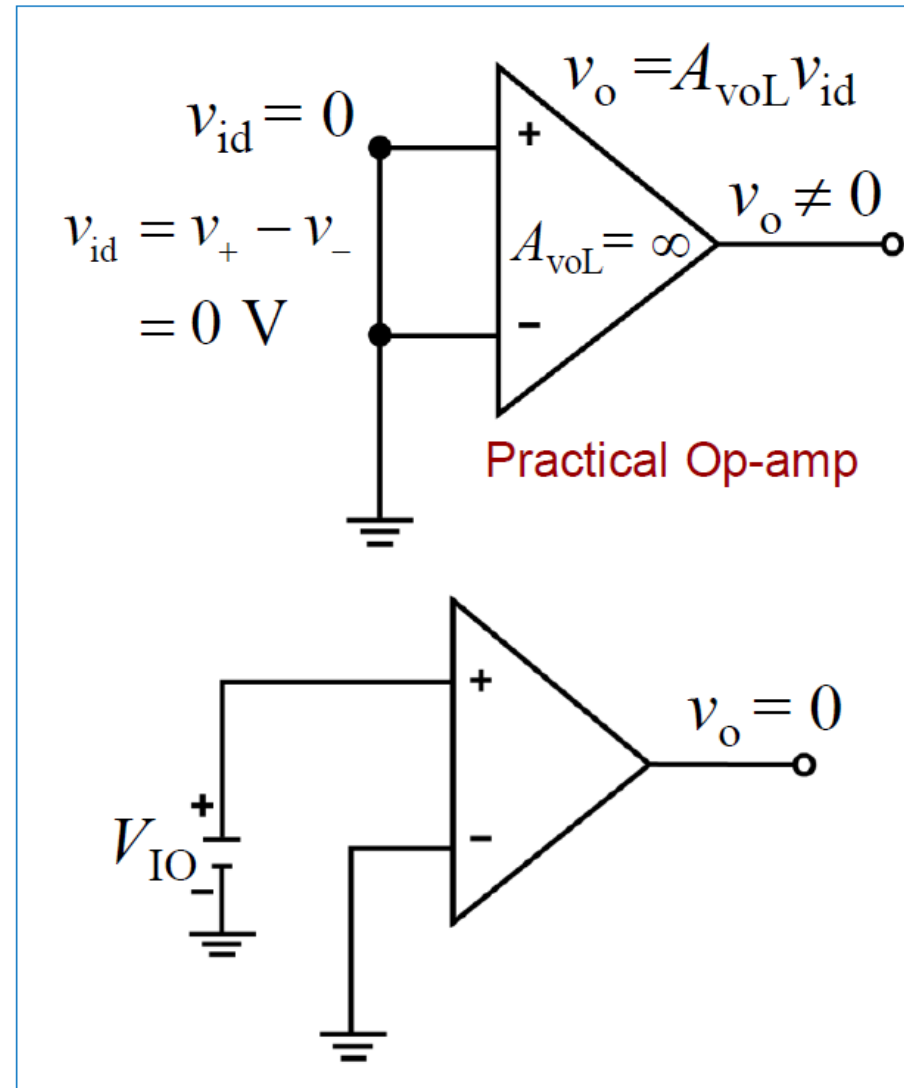
- Previous part was about Ideal op-amp → Real op-amp has several non-idealities
- Offset voltage – caused by circuit mismatch between + & - terminals
- Input current can be non-zero – BJT input
- Actual differential gain is not infinite
- Finite time taken for op-amp output to change → slew rate & bandwidth

Op-amp nonidealities: Offset

V_{IO} is defined as negative of the DC voltage that must be applied between the inputs of an op-amp to force v_o to zero under open-loop conditions (Figure 21).

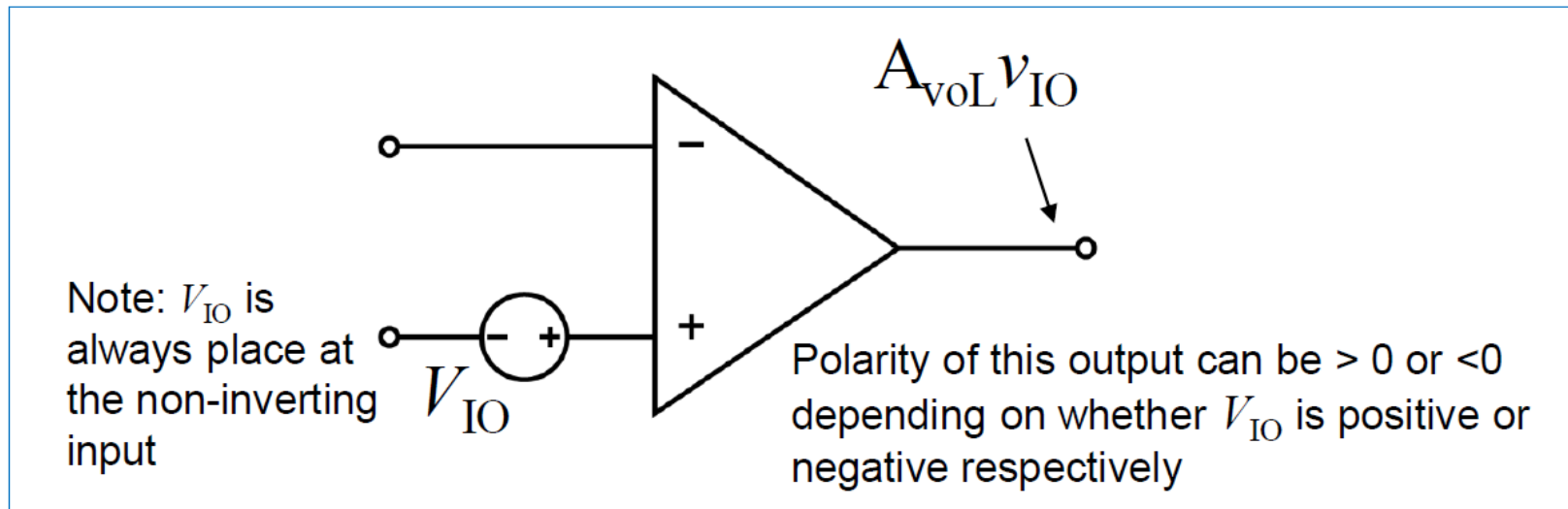
The V_{IO} can be either positive or negative and typically has a value between 10 mV and 1 μ V, depending on the type of op-amp.

It may also vary with temperature.



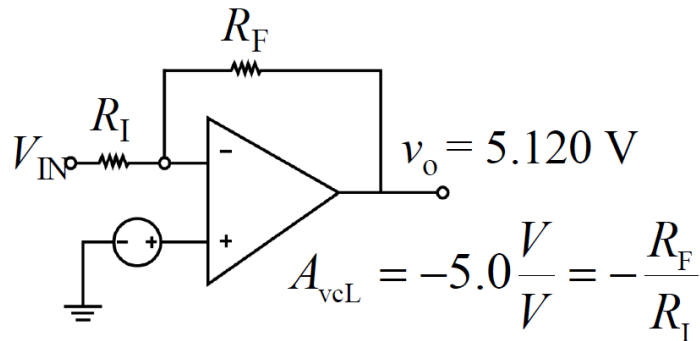
Op-amp nonidealities: Offset

The effect of V_{IO} on an op-amp circuit can be modelled by adding a DC voltage source V_{IO} in series with the non-inverting input terminal, as shown in the Figure.



Offset: Example

An inverting feedback amplifier has a closed-loop gain of $A_{\text{vcL}} = -5\text{V/V}$. The input signal V_{IN} is -1.0 VDC . The output voltage is 5.120 VDC . What's the V_{IO} for the op-amp?



Solution:

i) The expected output voltage is $v_o = \left(-\frac{R_F}{R_I}\right)V_{\text{IN}}$

$$= -5(-1)$$
$$= 5.0\text{ VDC}$$

ii) The actual $v_o = 5.120\text{ VDC}$

iii) The difference between (i) and (ii) is

$$5.120 - 5.0 = 0.120\text{ VDC}$$

iv) The input offset voltage V_{IO} will contribute to an output given by

$$v_o = \left(1 + \frac{R_F}{R_I}\right)V_{\text{IO}}$$
$$= (1 + 5)V_{\text{IO}}$$
$$= 6 V_{\text{IO}}$$

(v) The output obtained in (iv) must be 0.120 VDC .

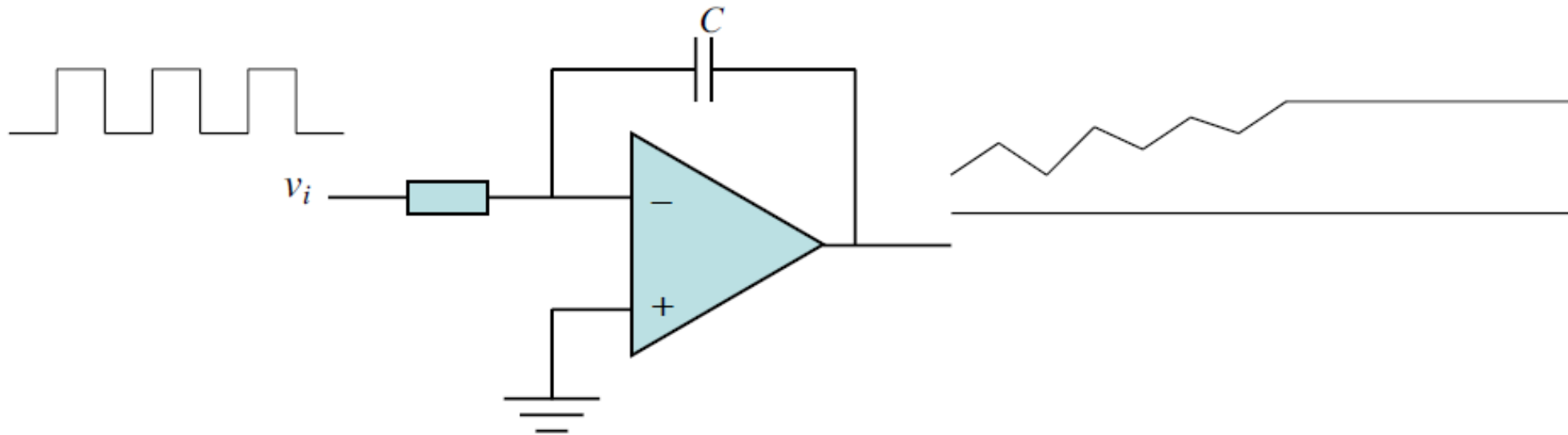
$$\text{Thus, } 6V_{\text{IO}} = 120\text{ mV}$$

$$V_{\text{IO}} = 20\text{ mV}$$

Offset: Practical problem

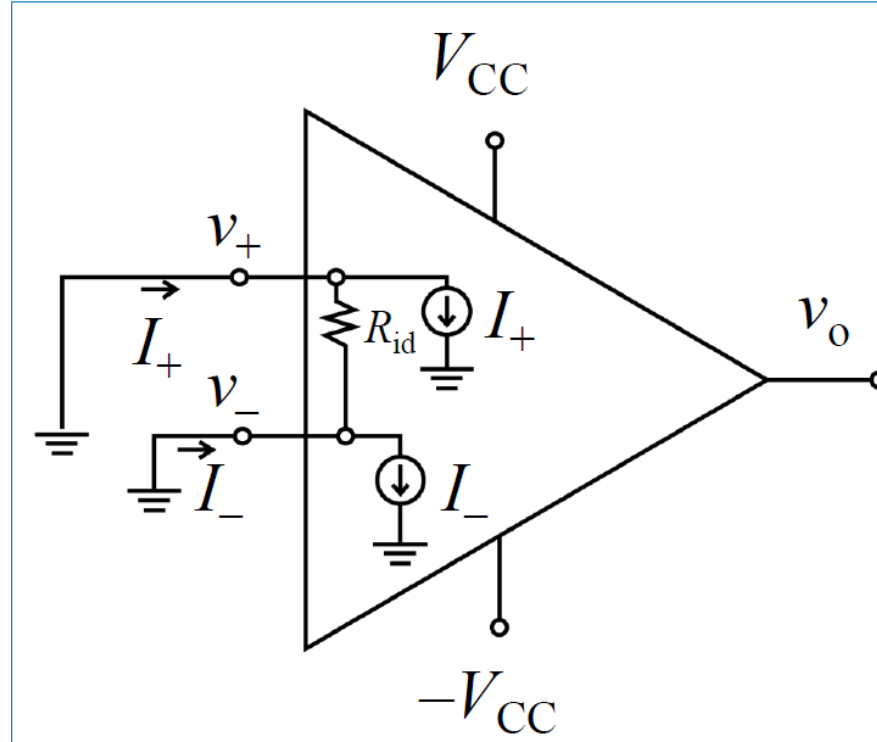
- **Offset in integrator**

- The op-amp integrator is very easily saturated if there is a small lack of symmetry. This is because the error gets integrated quickly and the output will soon move towards the maximum voltage.



Op-amp nonidealities: Input current

- A real op-amp must draw a small amount of DC bias currents (I_+ , I_-) into its v_+ and v_- terminals for proper operation of its internal circuit.
- These input bias currents are designated I_+ and I_- and they are modelled by placing DC current sources inside an otherwise ideal op-amp.



The input bias current is formally defined as the average of I_+ and I_- :

$$I_{\text{BIAS}} = \frac{1}{2}(I_+ + I_-)$$

Typical input bias currents range in value from **0.1 pA to 10 uA** and can be positive or negative, depending on the type of op-amp.

In some op-amps, the DC input bias currents I_+ and I_- are not equal.

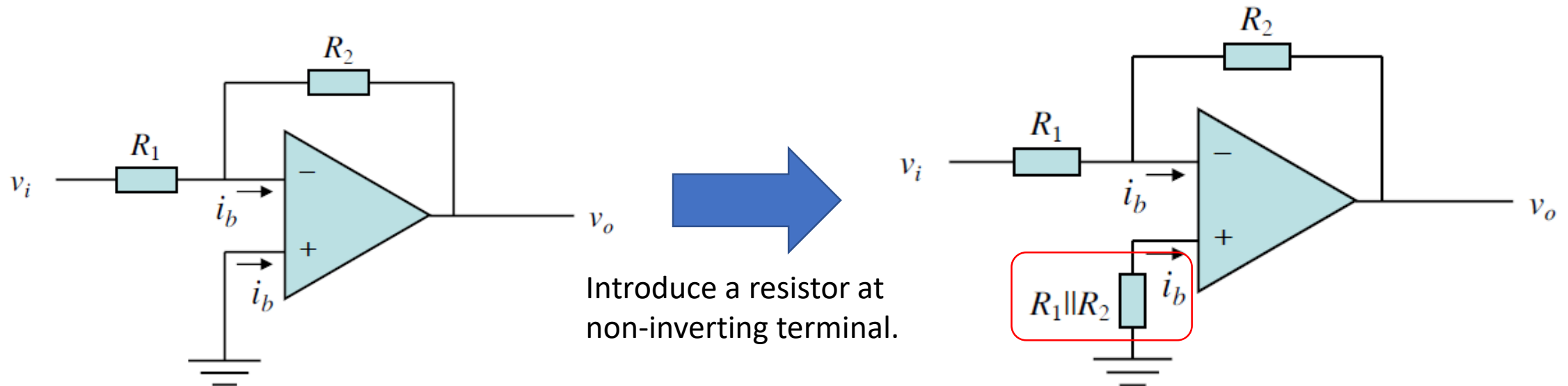
Their difference is called the **input offset current**, defined by the relation $I_{IO} = I_+ - I_-$

The imbalance is typically of **5 to 10%** of the average input bias current.

Op-amp nonidealities: Input current

- **Input bias current**

- **Unwanted offset:** Since i_b flows into both inputs, the negative input side will have a slightly negative dc voltage even when $v_i = 0$, whereas the positive input side is still 0V because there is no resistor there!



Op-amp nonidealities: Slew rate

The output of an ideal op-amp is able to change instantaneously.

In real op-amp the rate of change of the output is **finite**, in $V/\mu s$, can never exceed a specified value called the **slew rate, S_R** .

For $\mu A741$, $SR = 0.5 V/\mu s$

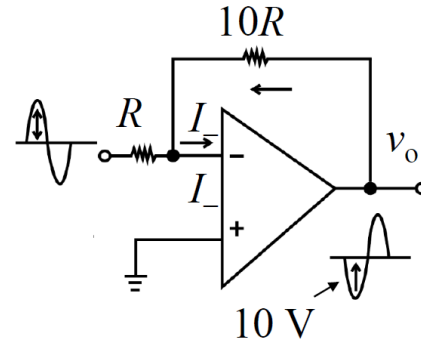
$SR = \text{Max } |dv_o/dt|$ of an opamp

When op-amp is driven to its slew rate limit, the **output exhibits non-linear behavior**.

Under such conditions, the output of an otherwise linear circuit will not be a faithful reproduction of the input signal and will exhibit **non-linear distortion**. Here, $V_+ \neq V_-$.

Slew rate: Example

An op-amp with $S_R = 1 \text{ V}/\mu\text{s} = 10^6 \text{ V/s}$ is used to build an inverting amplifier with a gain of -10 V/V . With a $1.0V_p$ sinusoid the output has a peak of 10 V .



Solution: $v_{in} = a_m \cos \omega t$

a) The slope of $v_o = a_m \times A_{VCL} \cos \omega t$ is $\frac{dv_o}{dt} = \omega a_m \times A_{VCL} \sin \omega t$ and

$$\begin{aligned} \max \left\{ \frac{dv_o}{dt} \right\} &= \omega a_m A_{VCL} \\ &= 2\pi f a_m A_{VCL} \end{aligned}$$

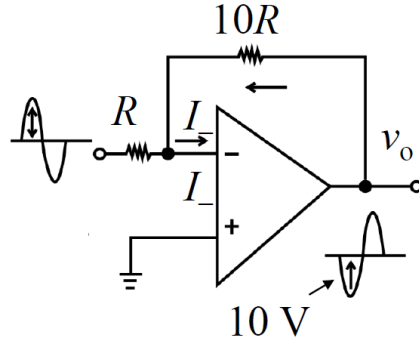
The $\text{Max}|dv_o/dt|$ should be less than S_R to avoid non-linear distortion, i.e., $\omega a_m A_{VCL} \leq S_R$.

For a $10V_p$ sinusoid, the frequency at which S_R limitation begins is

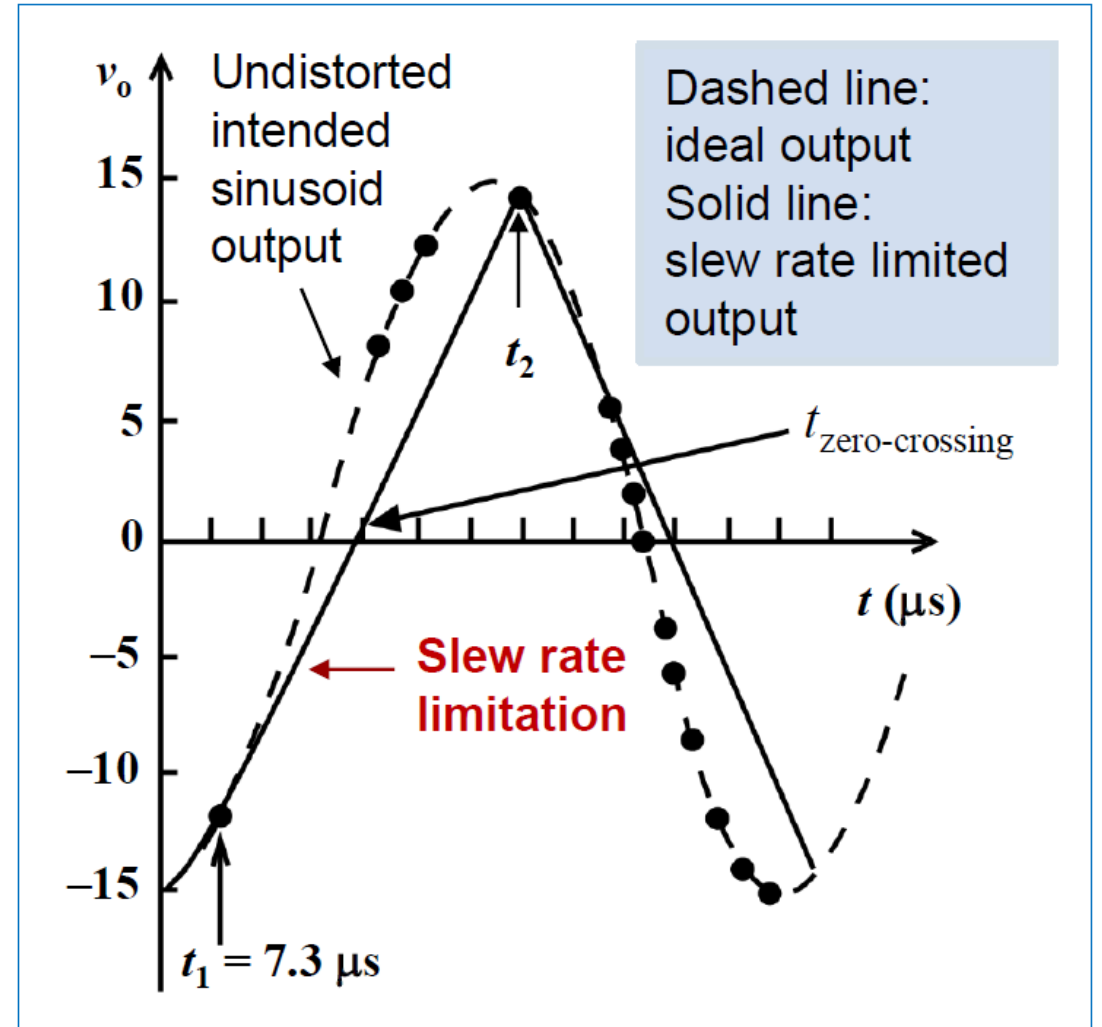
$$\begin{aligned} S_R &= 2\pi f_m a_m A_{VCL} \\ f_m &= \frac{S_R}{2\pi a_m A_{VCL}} \\ &= \frac{10^6 \text{ V/s}}{2\pi(10)} \\ &\approx 16 \text{ kHz} \end{aligned}$$

Slew rate: Example

An op-amp with $S_R = 1 \text{ V}/\mu\text{s} = 10^6 \text{ V/s}$ is used to build an inverting amplifier with a gain of -10 V/V . With a 1.0 V_p sinusoid the output has a peak of 10 V .



- At what frequency will the output be affected by S_R ?
- If the sinusoidal input is increased to 1.5 V at this frequency, sketch the resulting waveform.



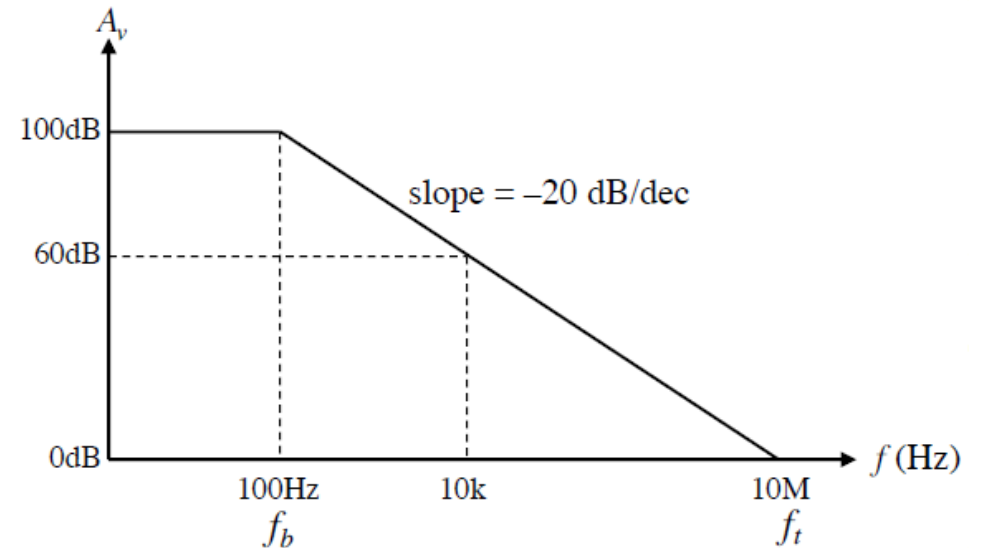
Op-amp nonidealities: Finite gain

- **Finite loop gain and bandwidth**

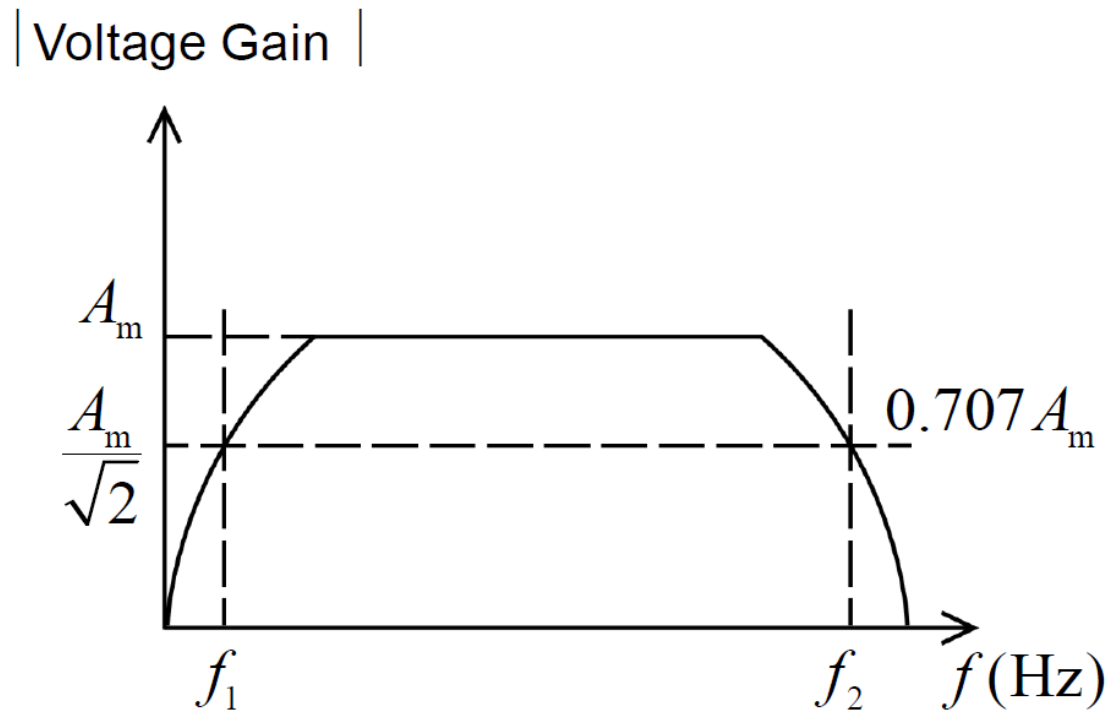
- The open-loop gain of practical op-amps is not infinite and drops as frequency increases.

- Open-loop gain: $A_o = \frac{V_o}{V_+ - V_-}$

- The gain is given by $A_v = \frac{A_o}{1 + \frac{j\omega}{\omega_b}}$
- ($\omega_b = 2\pi f_b$ is the break frequency)



Op-amp nonidealities: Bandwidth



Bandwidth

$$BW = f_2 - f_1$$

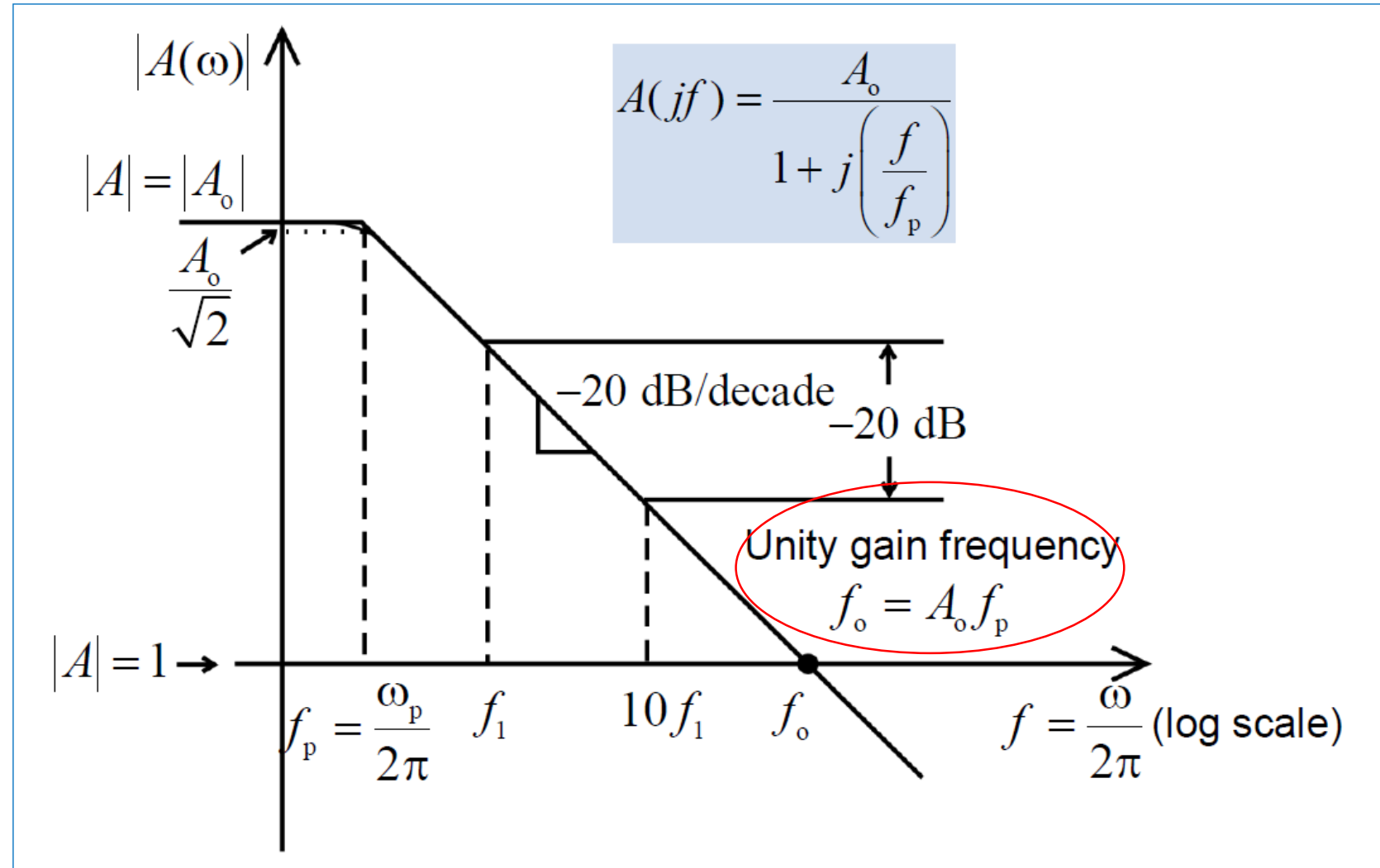
f_1 = lower cutoff frequency

f_2 = upper cutoff frequency

Op-amp nonidealities: Open-loop Bandwidth

The dominant pole frequency f_p is often in the low frequency hertz range (normally below 1 kHz).

Above f_p , the gain falls at a rate of -20 dB/decade.



Op-amp nonidealities: Open-loop Bandwidth

Gain [in dB] = 20 log Gain

$$A(jf) = \frac{A_o}{1 + j \frac{f}{f_p}}$$
$$\therefore |A(jf)| = \frac{A_o}{\sqrt{1 + \left(\frac{f}{f_p}\right)^2}}$$

UGF = Gain*BW
Gain-Bandwidth
product is constant

At unity-gain frequency, f_o , $|A(jf_o)|=1$

$$A_o = \left[1 + \left(\frac{f_o}{f_p} \right)^2 \right]^{\frac{1}{2}}$$

$$\left(\frac{f_o}{f_p} \right)^2 = A_o^2 - 1$$

$$f_o = f_p (A_o^2 - 1)^{\frac{1}{2}}$$

$$\therefore f_o = A_o f_p \quad (A_o \gg 1)$$

where

f_o = unity-gain frequency (freq.)
of the op-amp $A(jf)$

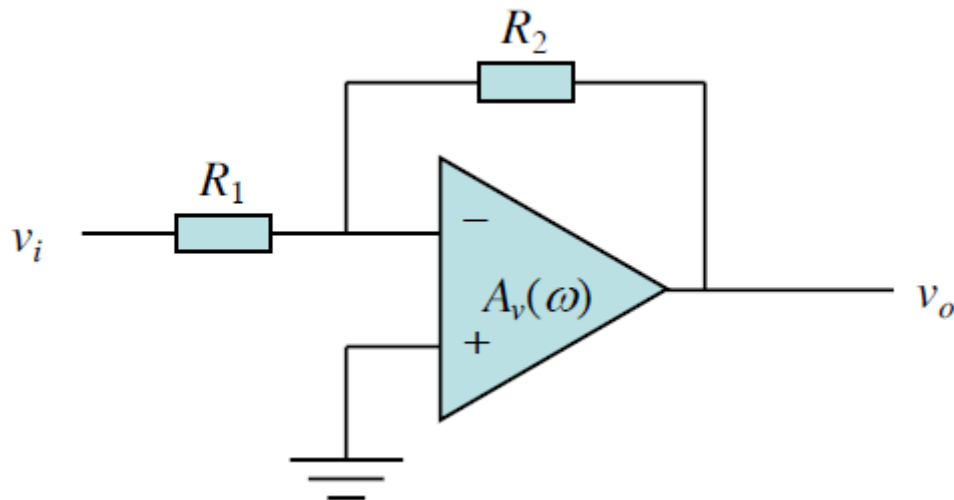
A_o = DC value of $A(jf)$

f_p = -3dB cutoff freq. of $A(jf)$

$A_o f_p$ = gain-bandwidth product

Op-amp nonidealities: Closed-loop Bandwidth

- Inverting amplifier: Suppose the op-amp gain is $A_v(\omega)$, not infinity! The inverting amplifier gain at ω becomes



$$\frac{v_o}{v_i} = \frac{-R_2/R_1}{1 + \frac{\left(1 + \frac{R_2}{R_1}\right)}{A_v(\omega)}}$$

Since

$$A_v(\omega) = \frac{A_o}{1 + \frac{j\omega}{\omega_b}}$$

and

$$A_o\omega_b = \omega_t$$

we have

$$\frac{v_o}{v_i} = \frac{-R_2/R_1}{1 + \frac{1}{A_o} \left(1 + \frac{R_2}{R_1}\right) + \frac{j\omega}{\omega_t} \left(1 + \frac{R_2}{R_1}\right)}$$

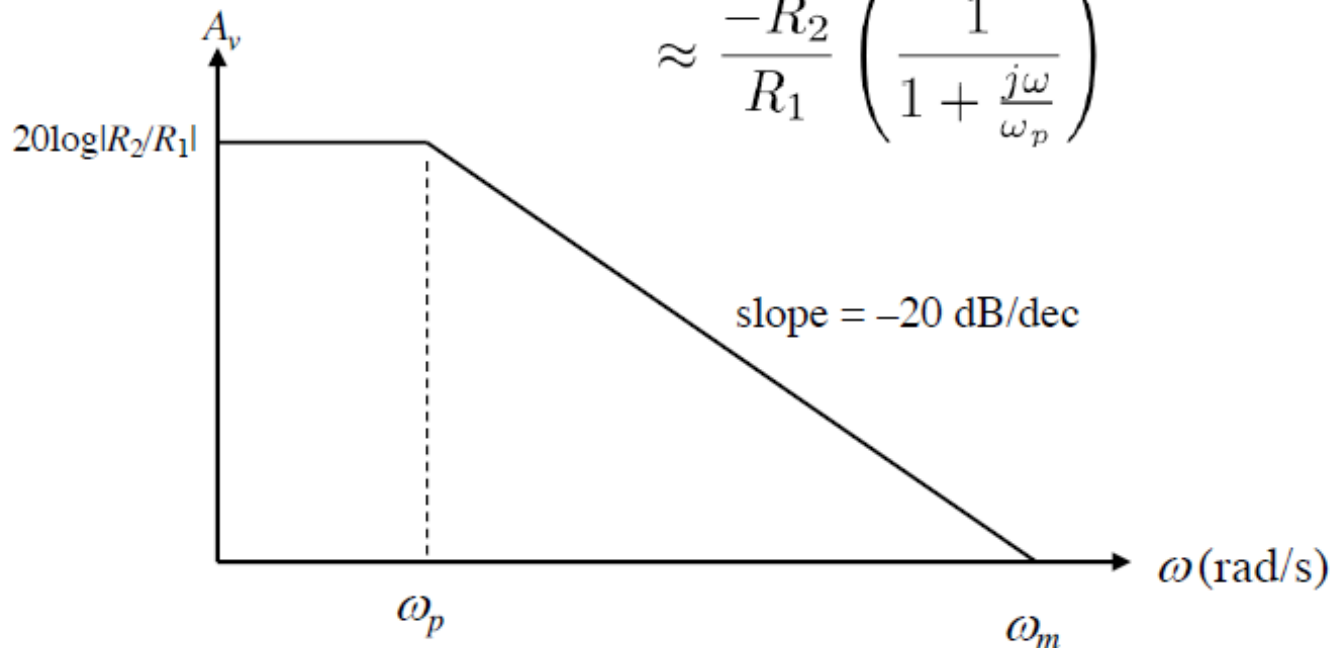
Op-amp nonidealities: Closed-loop Bandwidth

Clearly the transfer function has a typical first-order response.

$$\frac{v_o}{v_i} = \frac{-R_2/R_1}{1 + \frac{1}{A_o} \left(1 + \frac{R_2}{R_1}\right) + \frac{j\omega}{\omega_t} \left(1 + \frac{R_2}{R_1}\right)}$$

$$\approx \frac{-R_2}{R_1} \left(\frac{1}{1 + \frac{j\omega}{\omega_p}} \right)$$

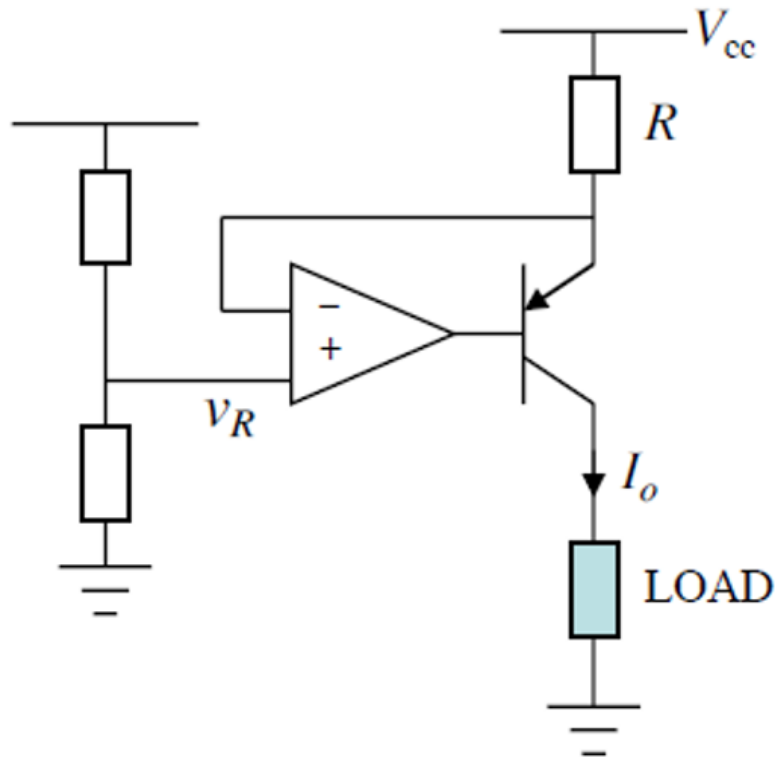
$$\text{where } \omega_p = \frac{\omega_t}{1 + \frac{R_2}{R_1}}$$



$$\omega_m = \omega_p (R_2 / R_1)$$

Op-amp : Other Applications

Current Source



Again v_R is fixed by the voltage divider.

The op-amp will make sure that the voltage at the lower end of R is also equal to v_R , which is fixed!

Therefore the current flowing down R must be

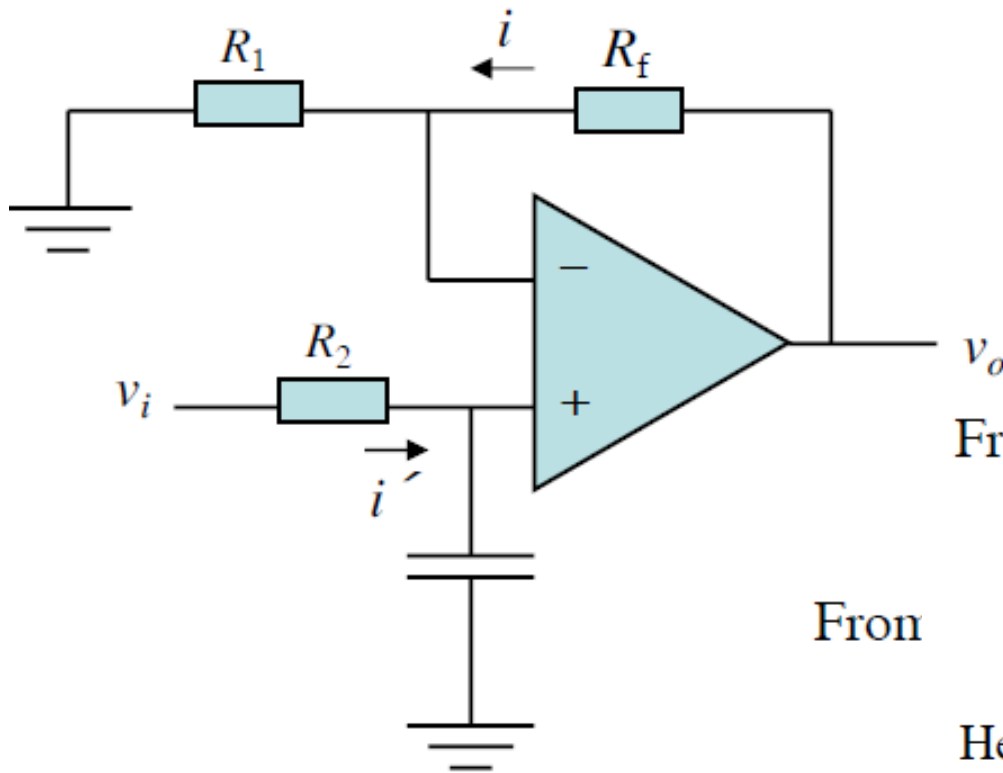
$$I_o = \frac{V_{cc} - v_R}{R}$$

which is very close to the load current (if base current is small and op-amp draws very small current).

Thus, this circuit provide a constant current source for the grounded load.

Op-amp : Other Applications

Low-pass Filter



$$v_o = i(R_1 + R_f) \quad (1)$$

$$iR_1 = i' \frac{1}{j\omega C} \quad (2)$$

$$iR_1 = v_i - i'R_2 \quad (3)$$

From (2) and (3), we get

$$i(j\omega CR_1) + i \frac{R_1}{R_2} = \frac{v_i}{R_2}$$

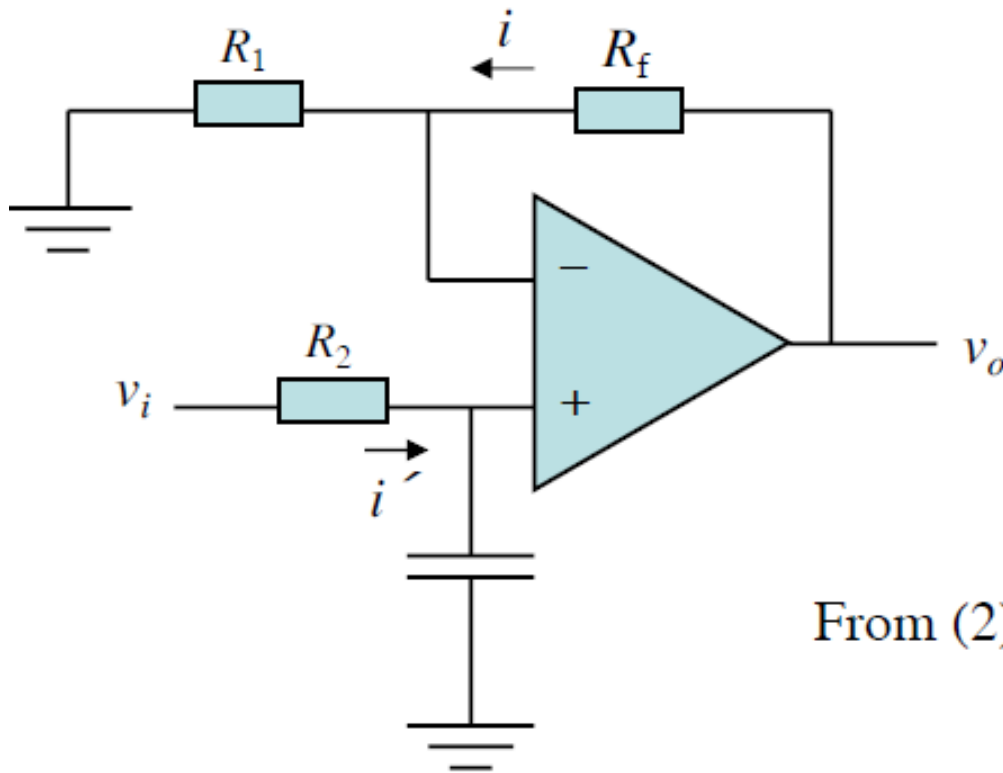
From

Hence, we have

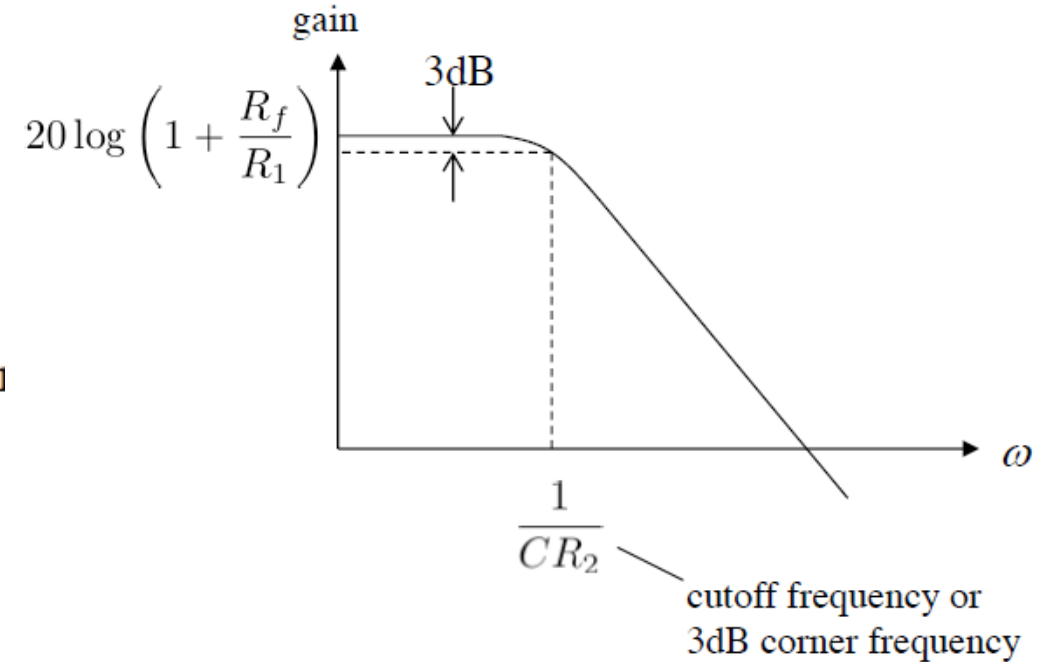
$$\begin{aligned} i &= \frac{v_i}{R_1 R_2} \left[\frac{1}{\frac{1}{R_2} + j\omega C} \right] \\ &= \frac{v_i}{R_1} \left[\frac{1}{\frac{1}{R_2} + j\omega C} \right] \end{aligned}$$

Op-amp : Other Applications

Low-pass Filter



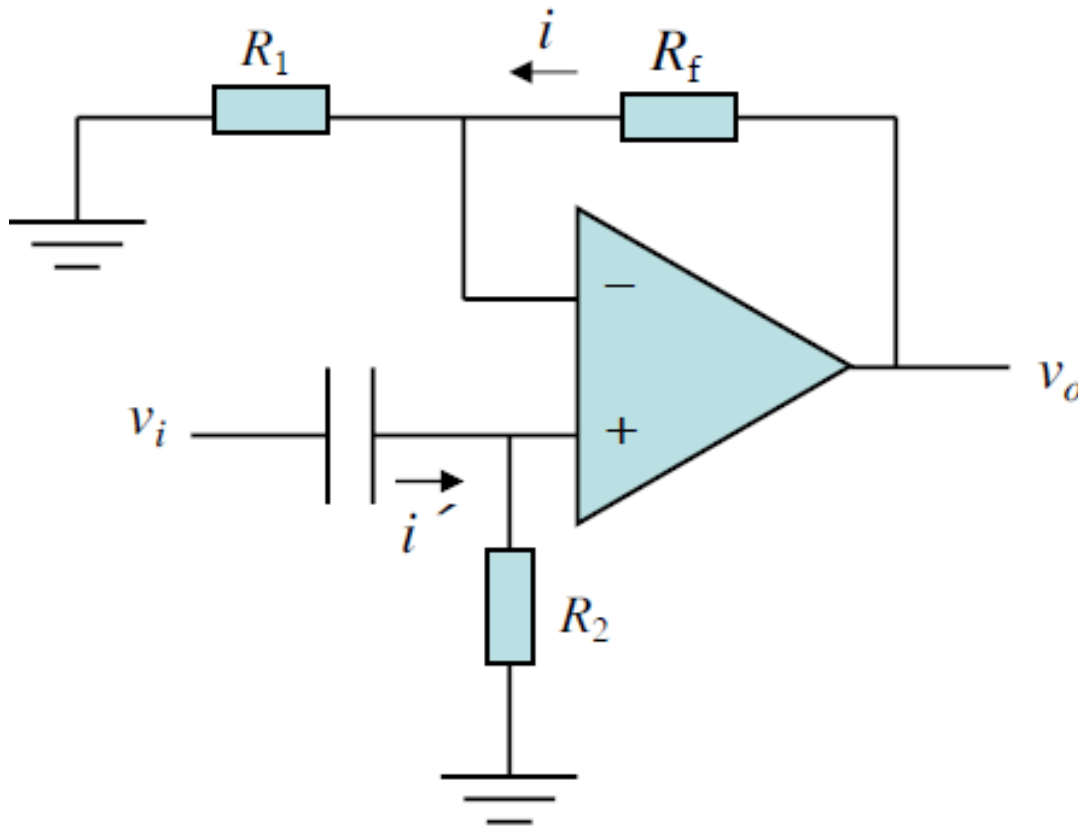
$$\frac{v_o}{v_i} = \frac{R_1 + R_f}{R_1} \left[\frac{1}{1 + j\omega CR_2} \right]$$



From (2) at

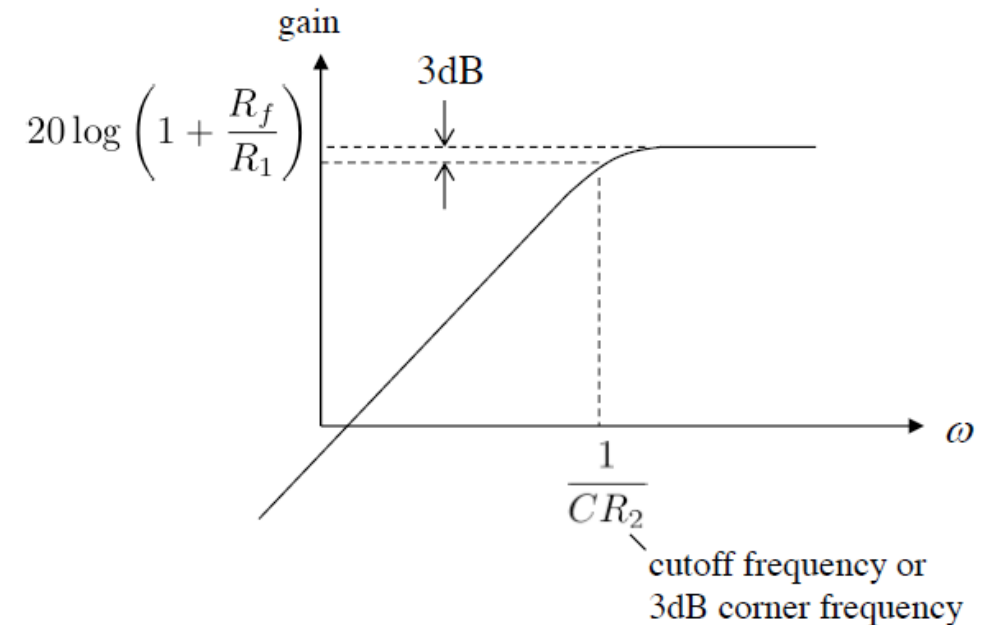
Op-amp : Other Applications

High-pass Filter



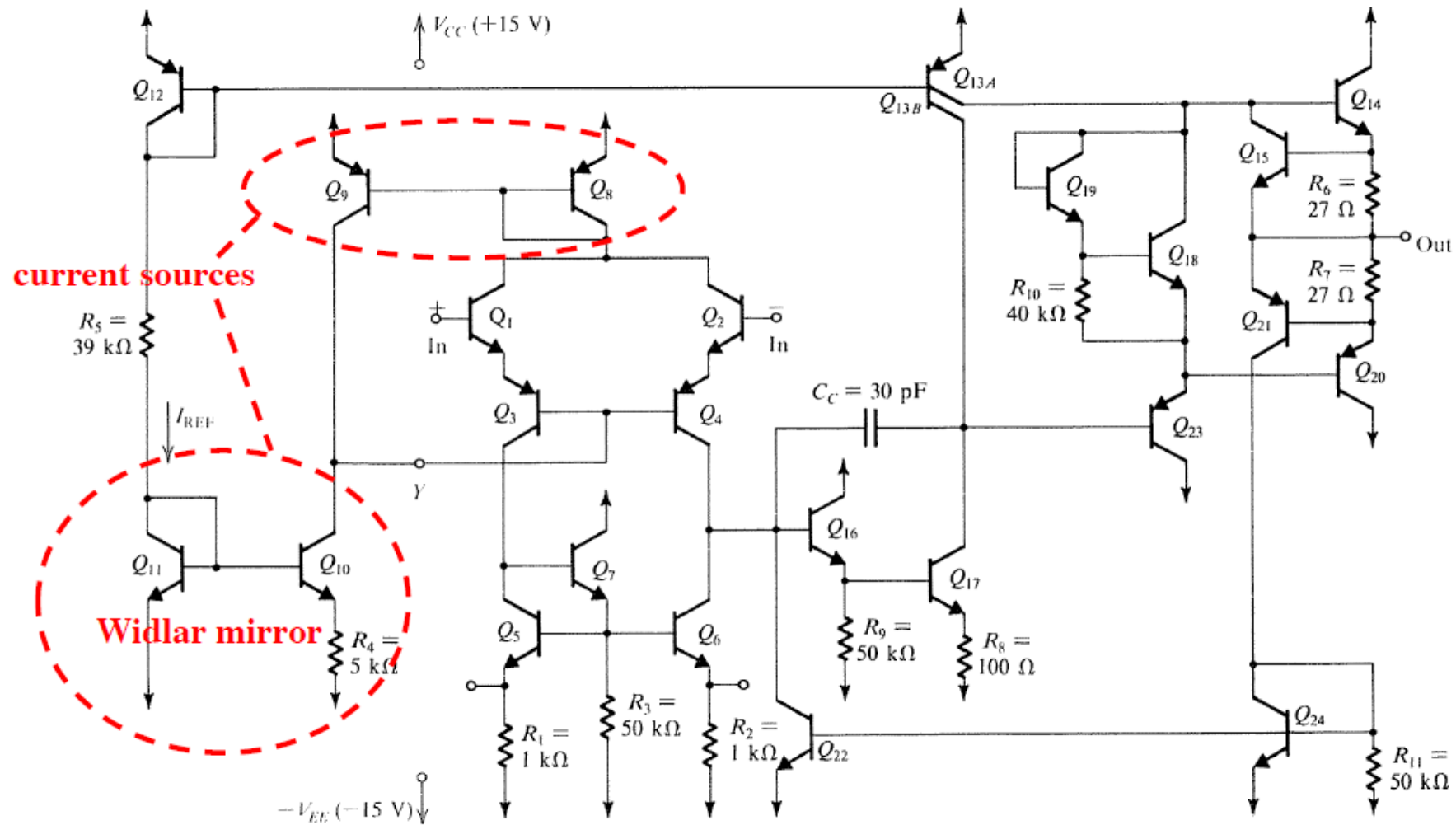
We can easily derive the transfer function as

$$\frac{v_o}{v_i} = \left[1 + \frac{R_f}{R_1} \right] \left[\frac{j\omega CR_2}{1 + j\omega CR_2} \right]$$

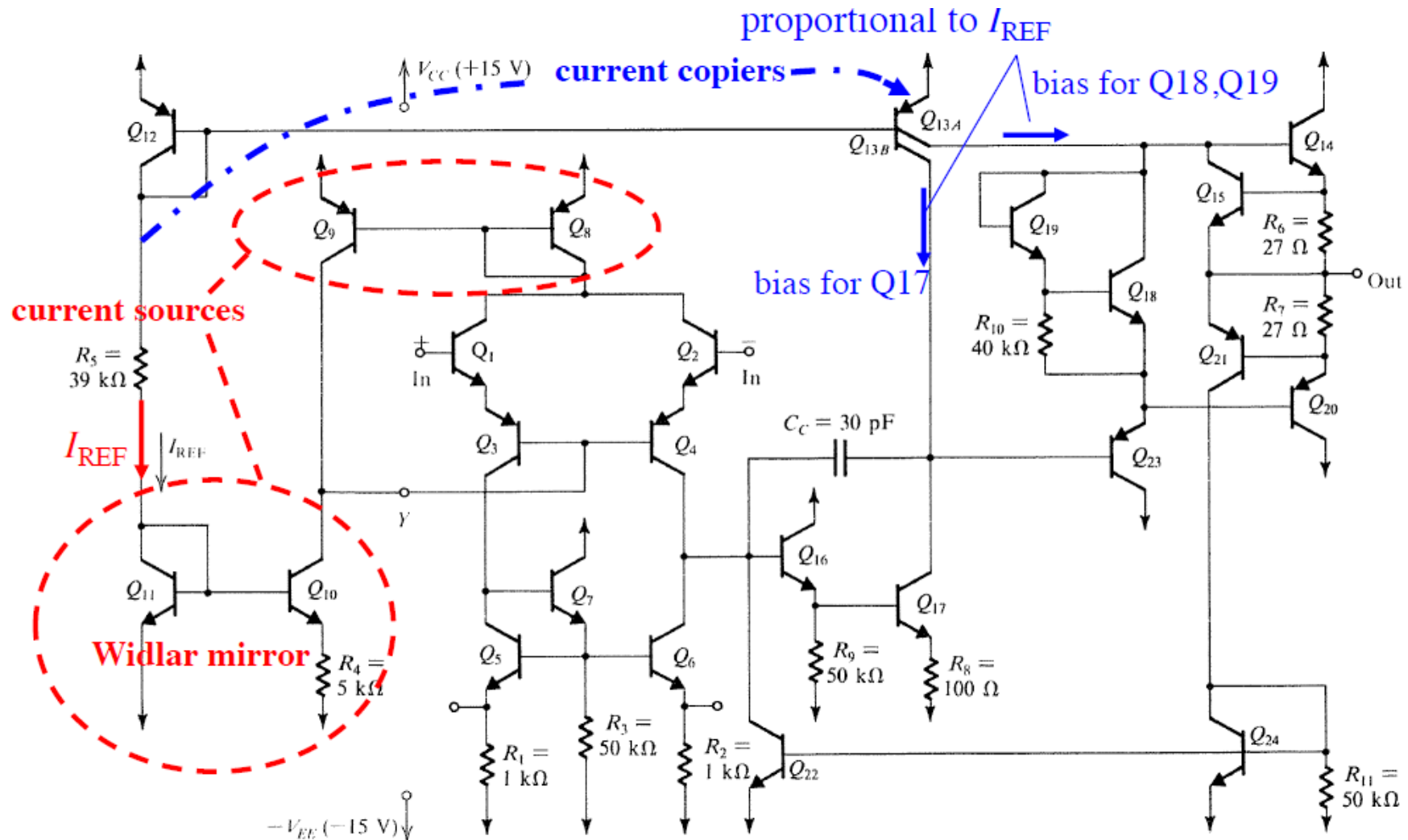


Appendix

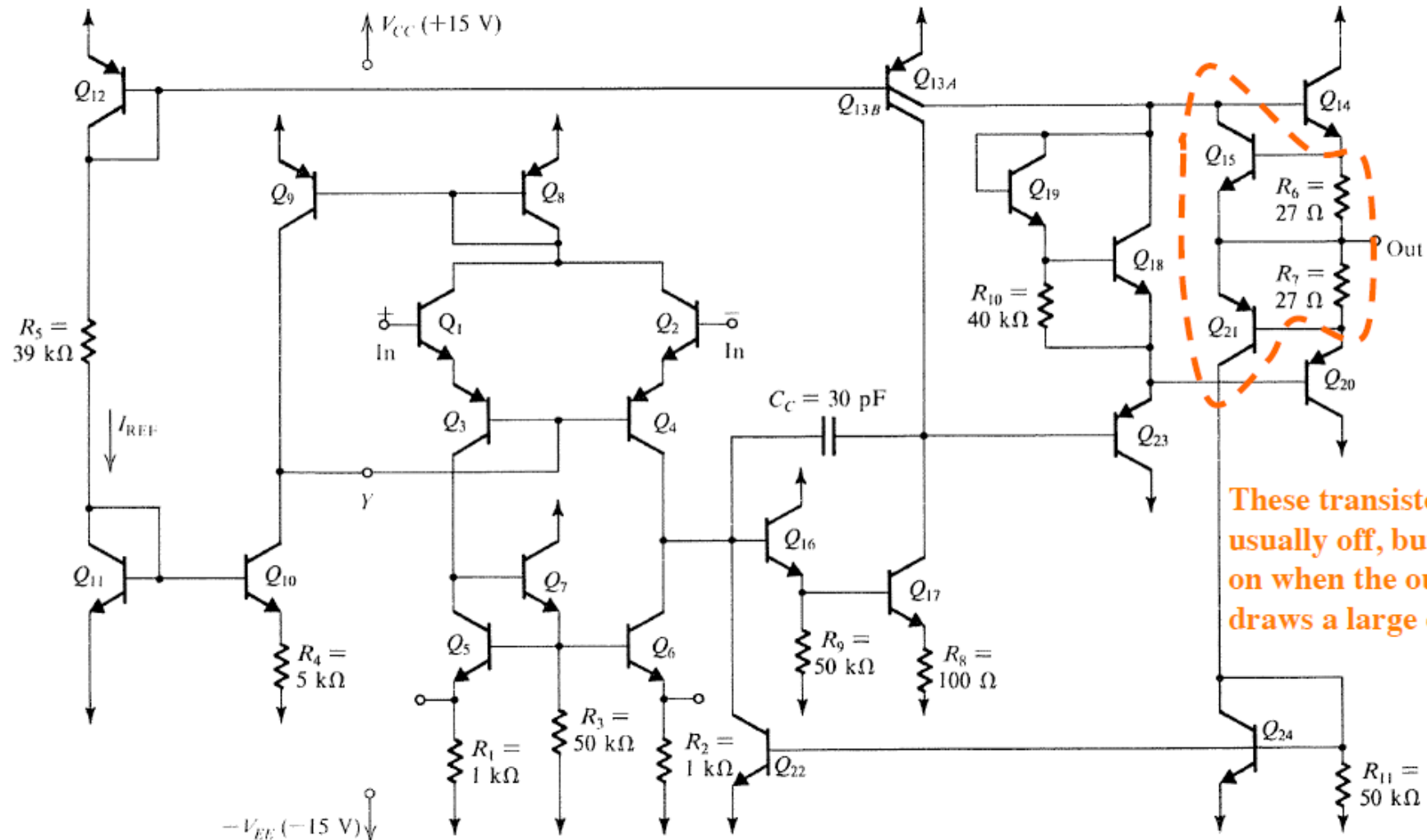
The bias circuit in 741



The bias circuit in 741

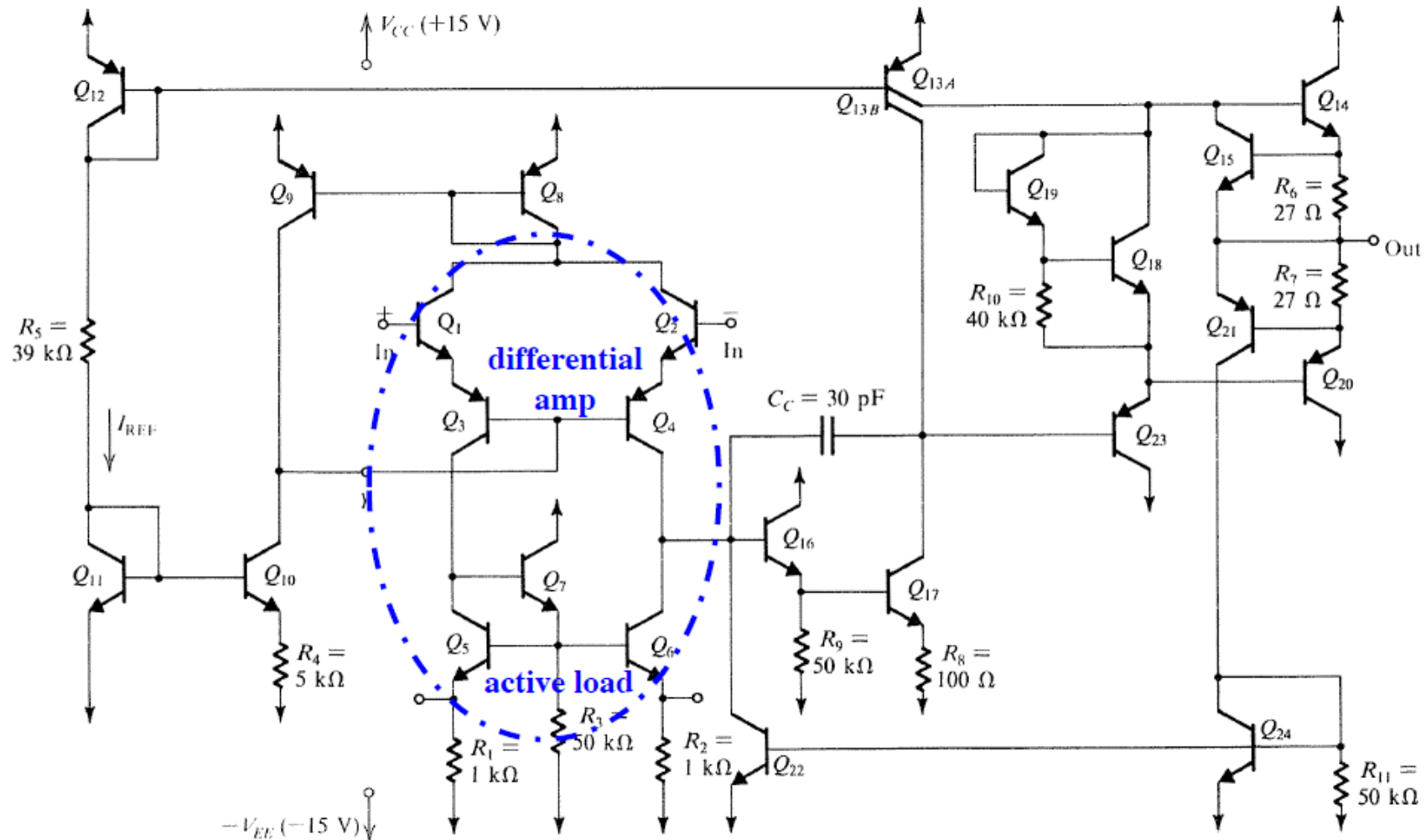


Short-circuit protection circuit in 741

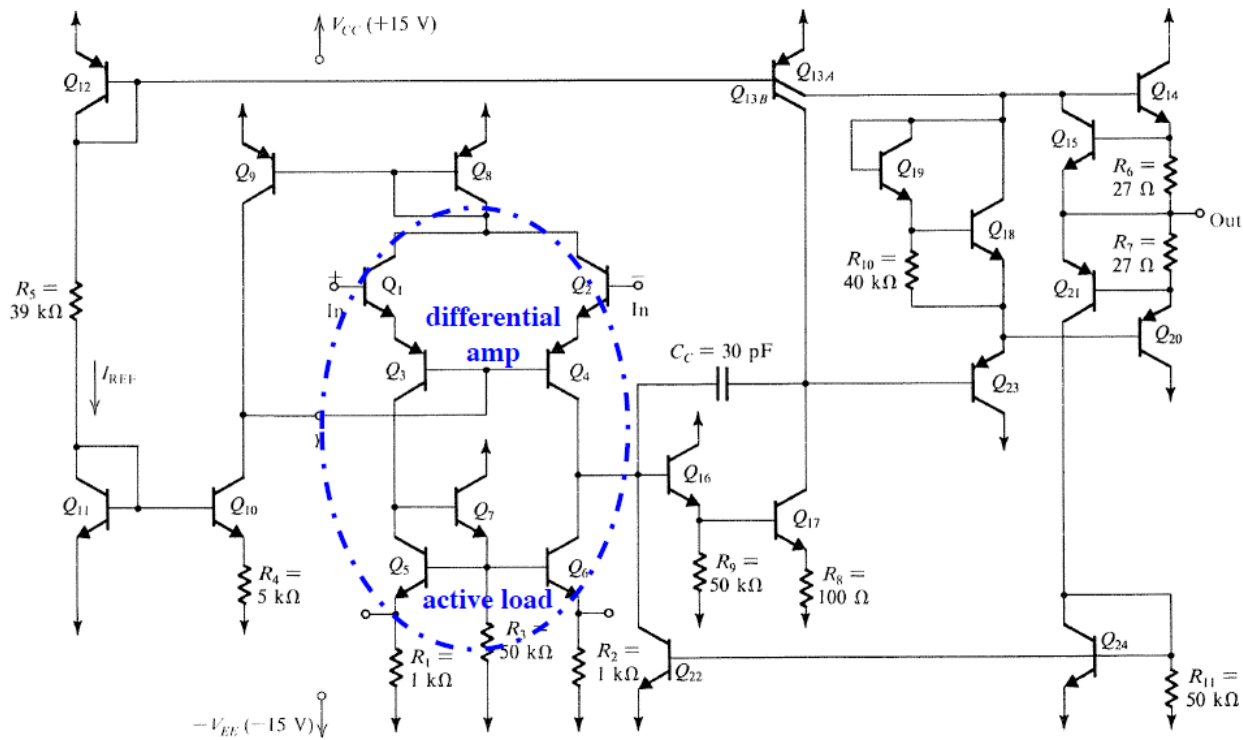


These transistors are usually off, but will be on when the output draws a large current.

Input stage



Input Stage



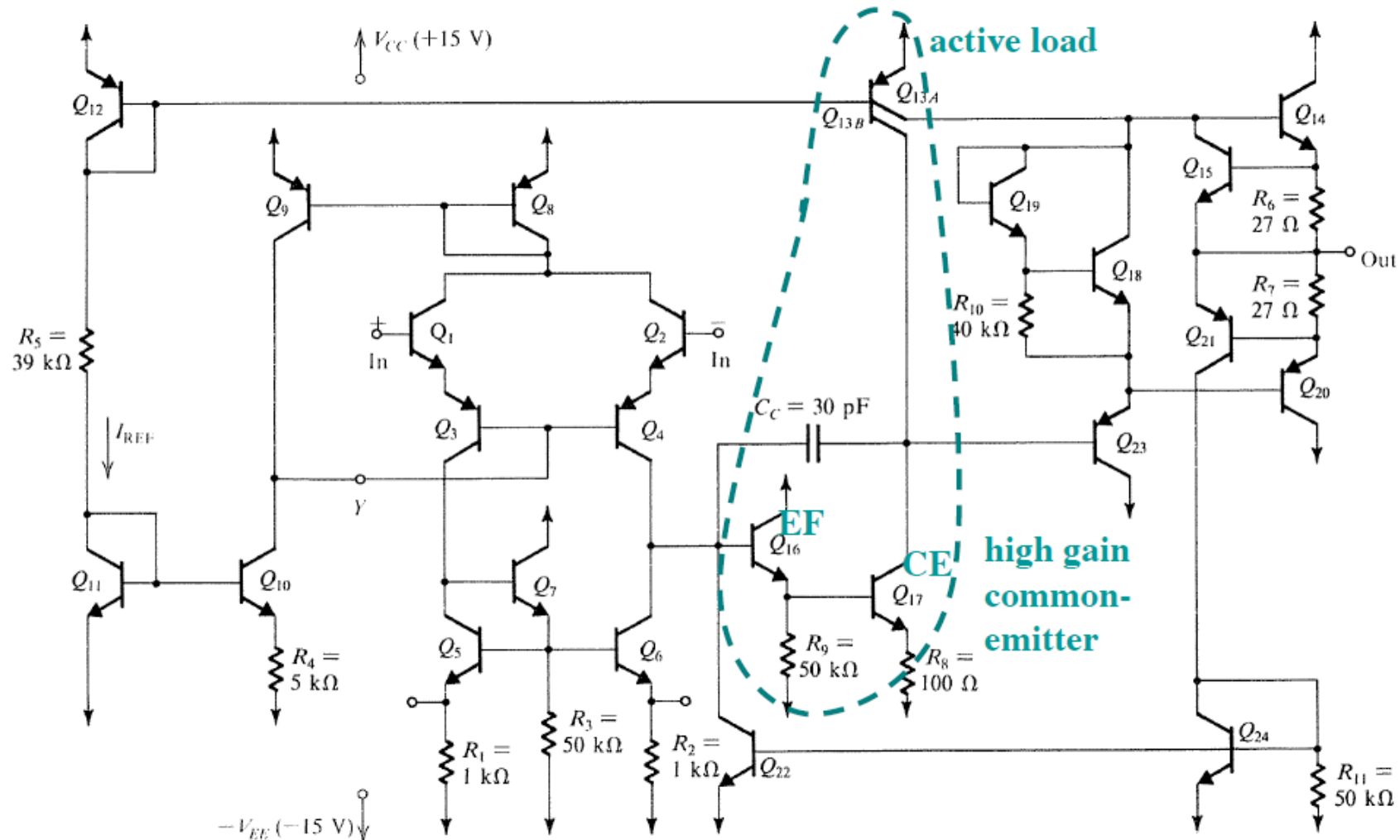
Q1 and Q2 are emitter followers, providing high input resistance.

Q3 and Q4 serve as differential amplifier, providing high CMRR.

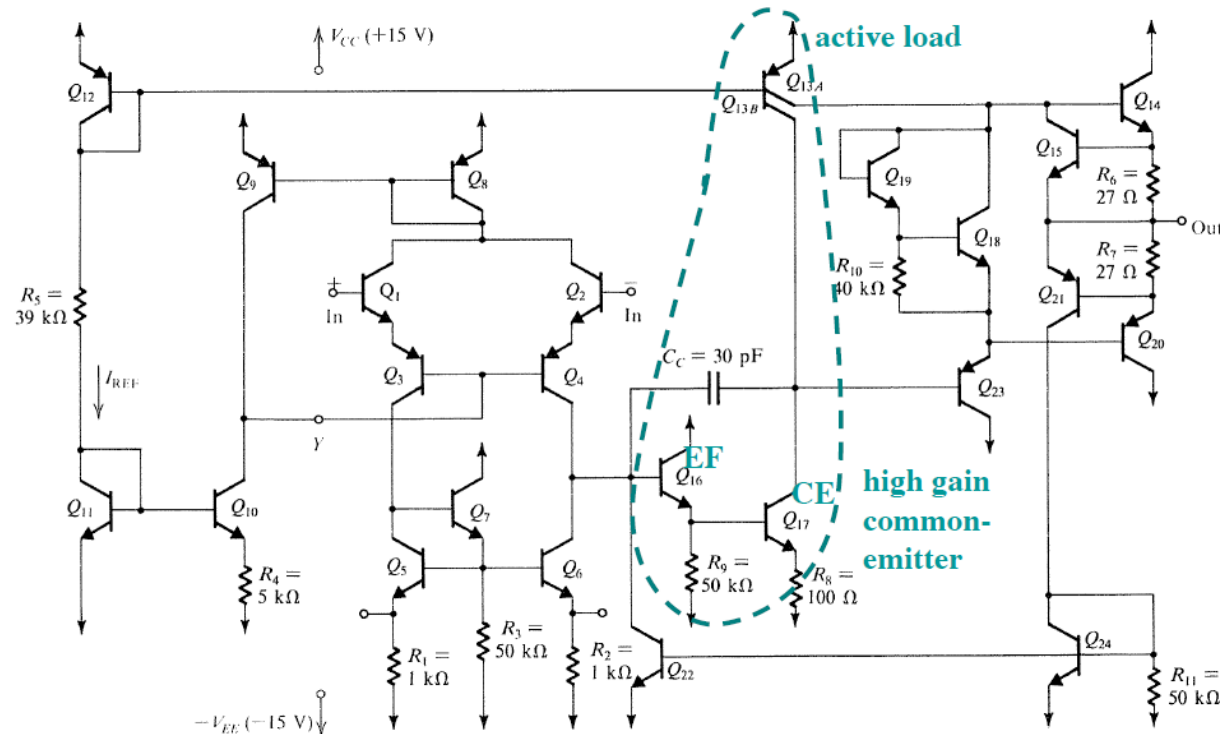
Q5, Q6, Q7 and R1, R2, R3 provide the load (active load) for the differential amplifier.

This loading circuit also provides a single-ended output for the next stage.

Second stage (gain stage)



Second stage (gain stage)



Q16 is an emitter follower, providing high input resistance for the stage so as to minimize its loading effect.

Q17 is a common-emitter amplifier, loaded by Q13B.

Q13B is a current mirror and serves as active load.

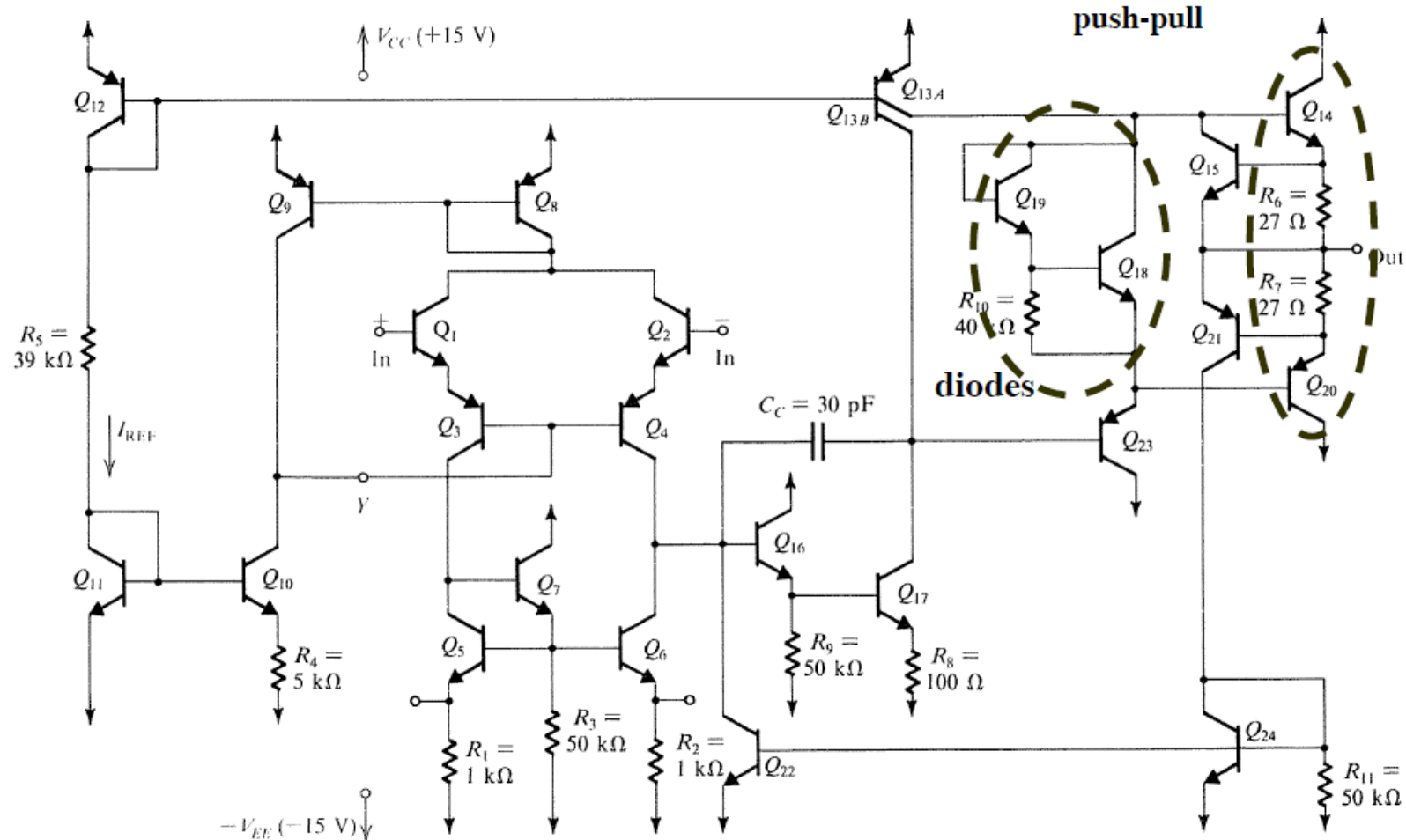
The gain is

$$\text{GAIN}_{\text{second stage}} \approx g_{m,17} r_{o,13B}$$

Note the capacitor C_c . This is called internal compensation cap and is used for maintaining stability in when the op-amp is used in a feedback configuration. We'll revisit this issue later when we study feedback and stability.

Output stage

Class AB output stage
complementary



Output stage

Provides low output resistance.

Class AB output stage provided by Q14 and Q20 as complementary push-pull.

Q19 and Q18 maintain a V_{BE} drop to smooth out the crossover distortion, as in the class AB amplifier.