

EE2000 Assignment 2

- Use (i) implication table and (ii) partitioning methods to obtain a reduced state table with minimum number of states from the state table shown in Fig. Q1.
- Find the state diagram and the function of this circuit shown in Fig. Q2. (Show all the steps involved solving this question.)

PS	NS/Output	
	x=0	x=1
A	D/0	F/0
B	D/0	A/1
C	D/1	B/0
D	C/1	E/0
E	D/0	F/1
F	C/0	G/0
G	D/0	F/0
H	E/0	G/1

Fig. Q1

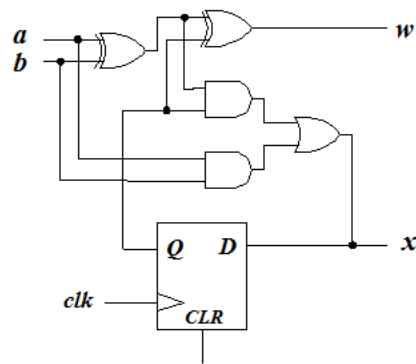


Fig. Q2

- Use JK FFs to design a sequential circuit that follows the operation as described below:
 - For current output-count is (0,2,4,6), its next count will be its next odd count when E=0, otherwise, its next count will be its next even count.
 - For current output-count is (1,3,5,7), its next count will be its next even count when E=1, otherwise, its next count will be its next odd count.
- A sequential logic circuit with one input and one output is used to stretch the first two bits of a 4-bit sequence as follows:

Input, x	Output, y
00XX	0000
01XX	0011
10XX	1100
11XX	1111

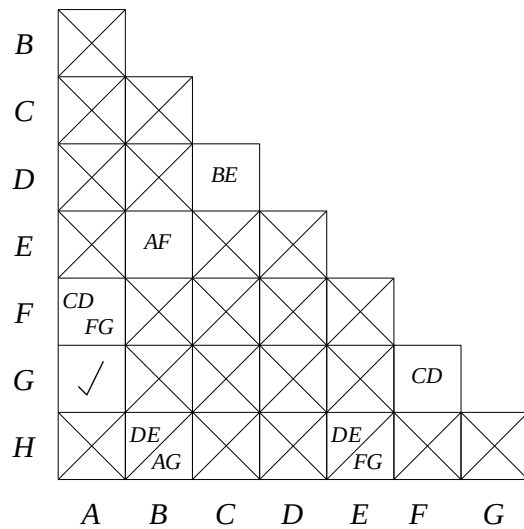
The circuit will ignore the third and fourth bits of the input sequence. After every four bits, the circuit resets.

- Draw a Mealy machine to describe the behavior of this sequential circuit.
 - Obtain a state table for the circuit (minimum of 7 states).
- A sequential data a is fed a monitoring circuit with 2 output w and x . w will set to 1 if a pattern of 1100 is detected; and x will be set 1 to if a pattern of 1011. Draw a state diagram to illustrate the operation of this monitoring circuit (a single state diagram to cover both detections). Use state reduction technique to obtain a minimal state diagram.

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Answers

1.



[5 marks]

$A=G$

$C=D \Rightarrow F=G$

$C=D \Rightarrow B=E \Rightarrow A=F \Rightarrow (C=D \ \& \ F=G)$

Hence $C=D \Rightarrow B=E \Rightarrow A=F \Rightarrow F=G$

$C=D \Rightarrow B=E \Rightarrow A=F=G$

[3 marks]

Reduced state table:

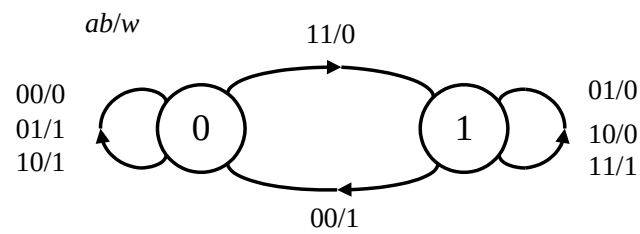
PS	NS/Output	
	x=0	x=1
A	C/0	A/0
B	C/0	A/1
C	C/1	B/0
H	B/0	A/1

[2 marks]

2. $w = a \oplus b \oplus Q$, $x = D = ab + (a \oplus b)Q$

Q_n	a	b	Q_{n+1}, D, x	w
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

[5 marks]



[3 marks]

A serial 1-bit full adder, a and b are inputs, w is sum and x is carry out.

[2 marks]

PS	I/P	NS	FF inputs		
$Q_2Q_1Q_0$	E	$Q_2Q_1Q_0$	J_2K_2	J_1K_1	J_0K_0
000	0	001	0x	0x	1x
000	1	010	0x	1x	0x
001	0	010	0x	1x	x1
001	1	011	0x	1x	X0
010	0	011	0x	X0	1x
010	1	100	1x	x1	0x
011	0	100	1x	x1	X1
011	1	101	1x	x1	X0
100	0	101	x0	0x	1x
100	1	110	x0	1x	0x
101	0	110	X0	1x	x1
101	1	111	X0	1x	X0
110	0	111	X0	x0	1x
110	1	000	X1	X1	0x
111	0	000	x1	X1	X1
111	1	001	X1	X1	x0

[10 marks]

Q_0E	Q_2Q_1		
		X	X
	1	X	X
	1	X	X
	1	x	x

$$J_2 = EQ_1 + Q_1Q_0$$

Q_0E	Q_2Q_1		
	X	X	
	X	X	1
	X	X	1
	x	x	1

$$K_2 = EQ_1 + Q_1Q_0$$

[2 marks]

Q_0E	Q_2Q_1		
		X	X
	1	X	X
	1	X	X
	1	x	x

$$J_1 = E + Q_0$$

Q_0E	Q_2Q_1		
	X		X
	X	1	1
	X	1	1
	x	1	1

$$K_1 = E + Q_0$$

[2 marks]

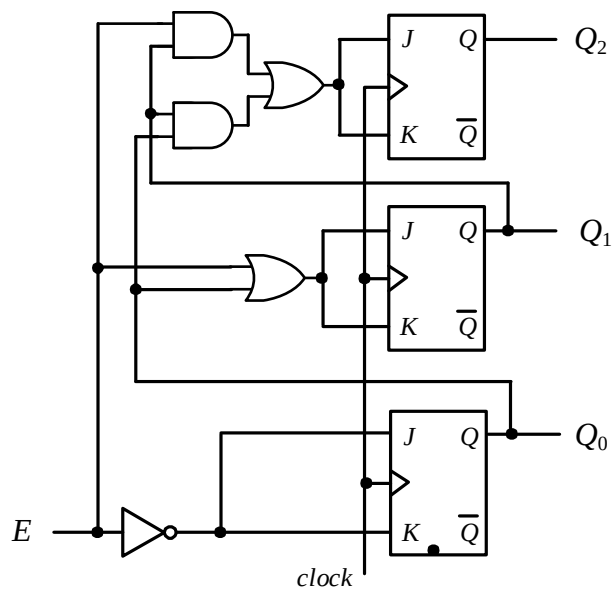
Q_0E	Q_2Q_1		
	1	1	1
	X	X	X
	x	x	x

$$J_0 = \bar{E}$$

Q_0E	Q_2Q_1		
	X	X	X
	X	X	X
	1	1	1

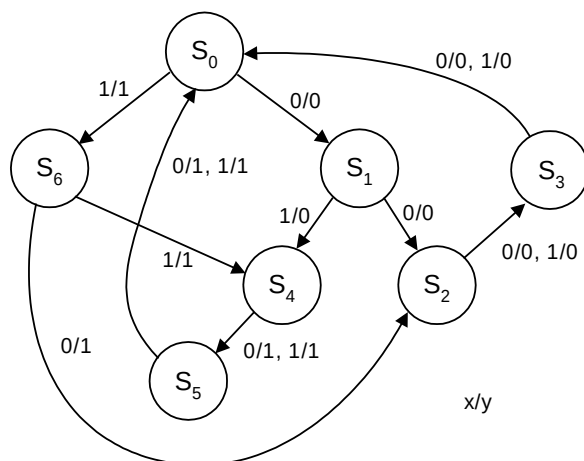
$$K_0 = \bar{E}$$

[2 marks]



[4 marks]

4(i)



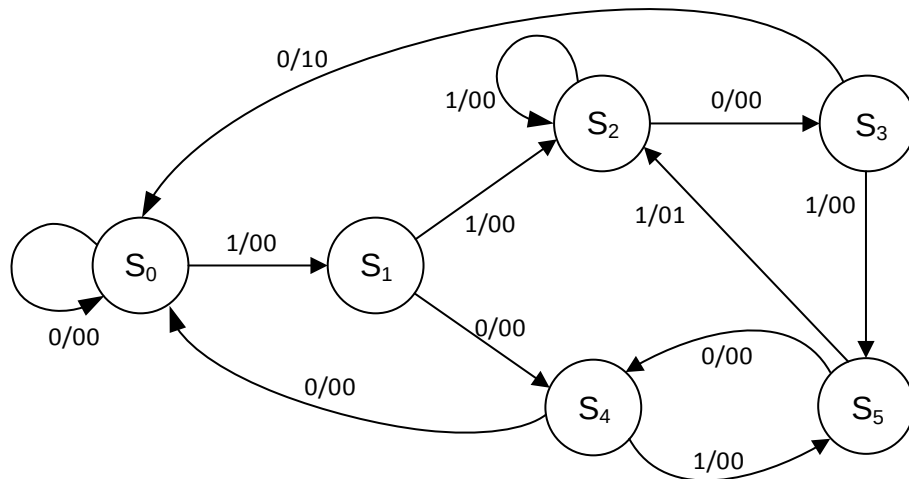
[10 marks]

4(ii)

PS	NS/output	
	$x = 0$	$x = 1$
S_0	$S_1/0$	$S_6/1$
S_1	$S_2/0$	$S_4/0$
S_2	$S_3/0$	$S_3/0$
S_3	$S_0/0$	$S_0/0$
S_4	$S_5/1$	$S_5/1$
S_5	$S_0/1$	$S_0/1$
S_6	$S_2/1$	$S_4/1$

[4 marks]

Q5.



[10 marks]

PS	NS/output(w,x)	
	$a = 0$	$a = 1$
S_0	$S_0/00$	$S_0/00$
S_1	$S_4/00$	$S_2/00$
S_2	$S_3/00$	$S_2/00$
S_3	$S_0/10$	$S_5/00$
S_4	$S_0/00$	$S_5/00$
S_5	$S_4/00$	$S_2/01$

Partition P_0	$S_0 S_1 S_2 S_4 S_3 S_5$					
Output for $a = 0$	0 0 0 0 1 0					
Output for $a = 1$	0 0 0 0 0 1					
Partition P_1	S_0	S_1	S_2	S_4	S_3	S_5
Next state for $a = 0$	S_0	S_4	S_3	S_0	S_0	S_4
Next state for $a = 1$	S_0	S_2	S_2	S_5	S_5	S_2
Partition P_2	S_0	S_1	S_2	S_4	S_3	S_5
Next state for $a = 0$	S_0	S_4	S_3	S_0	S_0	S_4
Next state for $a = 1$	S_0	S_2	S_2	S_5	S_5	S_2

Minimum no of states is 6.

[5 marks]