
EE4803: Analog IC Design

Laboratory Manual

City University of Hong Kong
Department of Electrical Engineering

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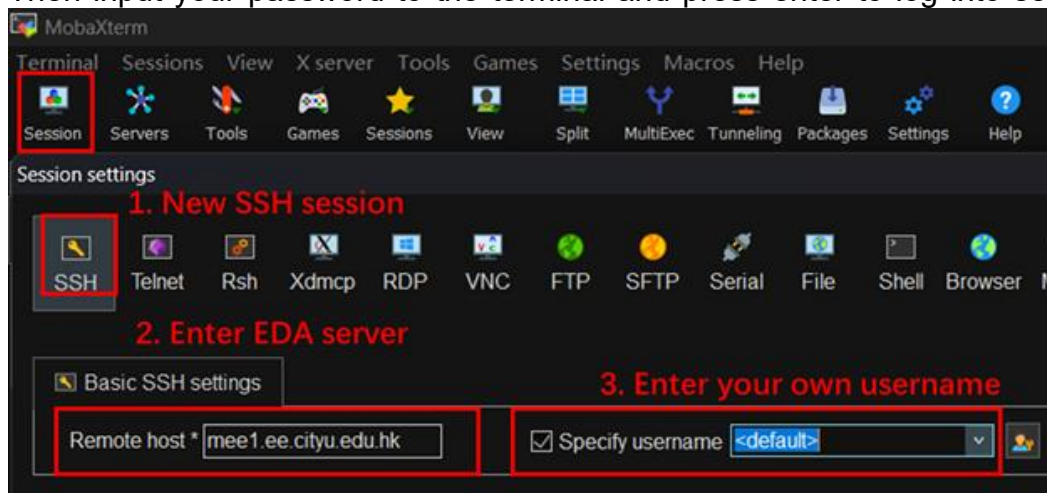
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Lab 1: Understanding MOS and VIRTUOSO Environment

Environment Setup

Cadence Virtuoso is an industrial-level EDA platform for analog IC design. Follow the below steps to access the software on our server through X11 forwarding.

1. Open MobaXterm on your desktop and start a new SSH session.
2. In the pop-up window, enter the EDA server address: mee1.ee.cityu.edu.hk and your username.
3. Then input your password to the terminal and press enter to log into server.



4. After logging in, stay in your home directory and source the setup script with the command below. You should see the sky130 directory after installation.

```
source /opt/ee4803/sky130_install/sky130_release_0.1.0/sky_install
```

5. Use the below commands to start Cadence Virtuoso under sky130 directory with the correct environment variables.

```
cd ~/sky130
module load cadence
module load mentor-graphics
. .bashrc
virtuoso &
```

6. It is always good to learn to use some basic Linux shell commands to work with Virtuoso.

cd: change directory
rm: remove
cp: copy
mv: move
ls: list files
mkdir: create directories

touch: create files
pwd: print working directory

Other references:

<https://missing.csail.mit.edu/2020/course-shell/>

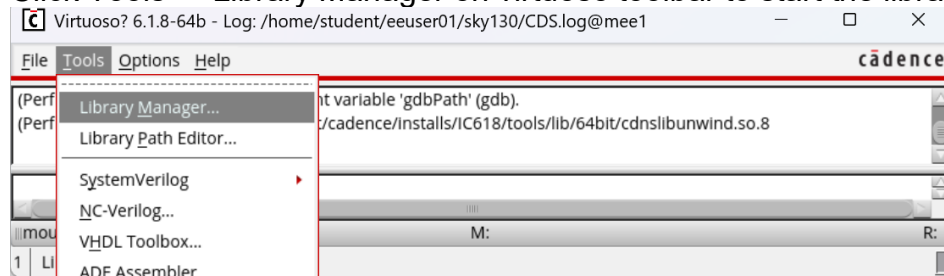
<https://www.runoob.com/linux/linux-command-manual.html>

Getting Familiar with Cadence Virtuoso

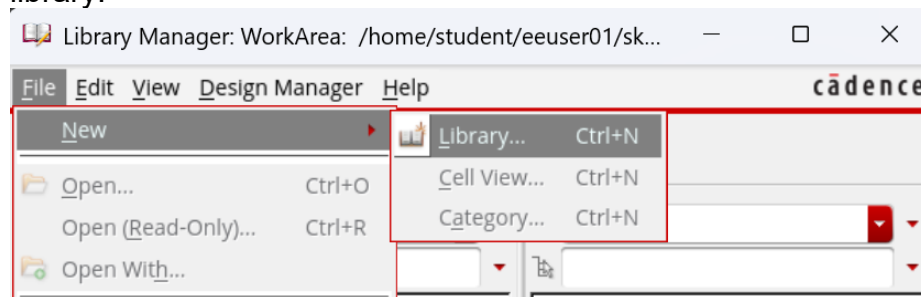
Now proceed with the steps below to draw a new schematic and simulate it. You may also need this schematic in Lab 1.1.

Create new cells and libraries

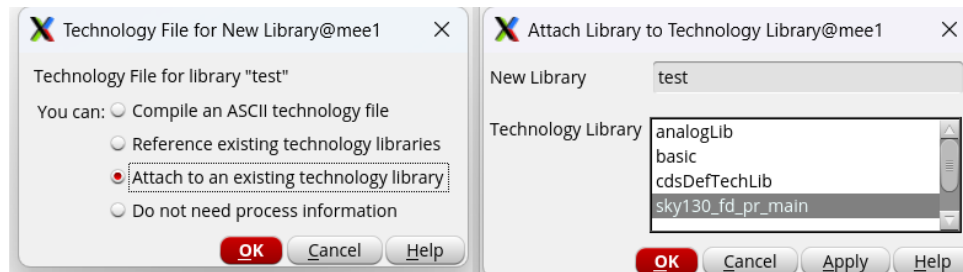
1. Click Tools -> Library Manager on virtuoso toolbar to start the library manager.



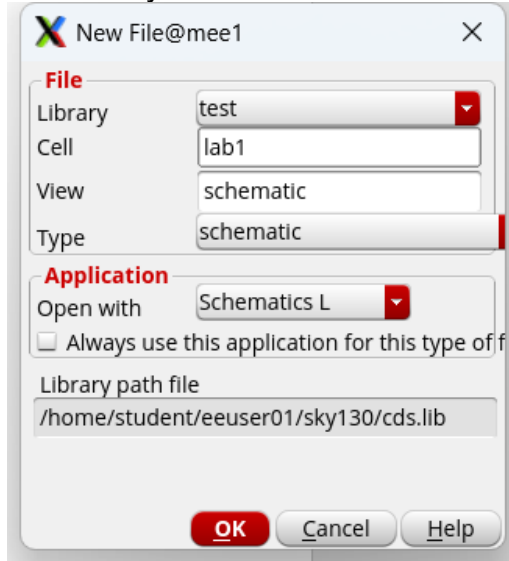
2. Click File -> New -> Library on the library manager toolbar to create a new library.



Attached this library to *sky130_fd_pr_main* technology.

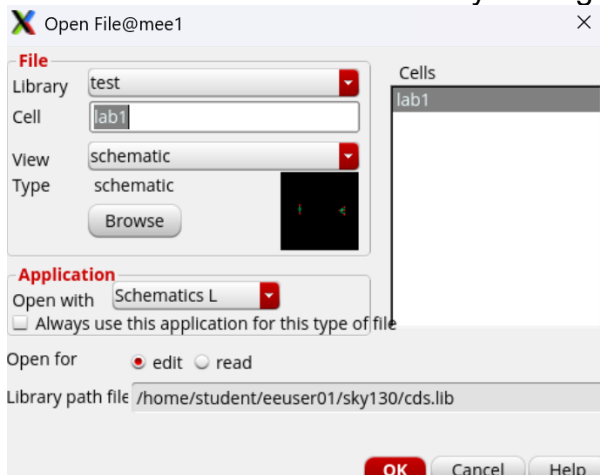


3. Click File -> New -> Cell View to create a new cell with schematic view in the new library.

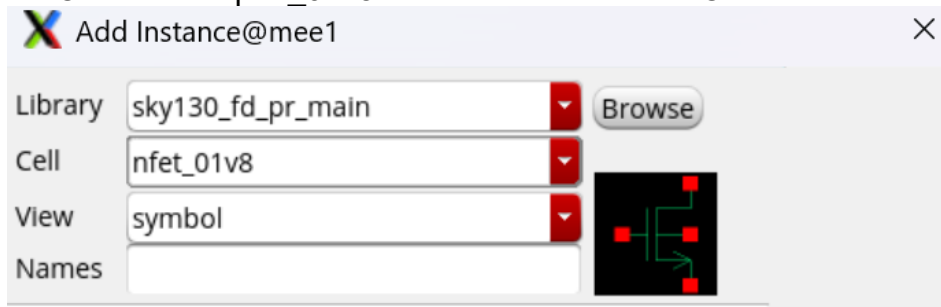


Drawing schematics

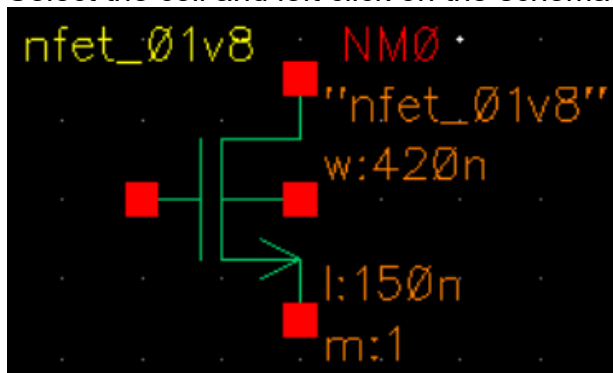
1. Now double click the cell in library manager to view its schematic.



2. Use shortcut **!** to add schematic instances. In our technology library sky130_fd_pr_main, the regular NMOS is called nfet_01v8 and the regular PMOS is called pfet_01v8. Let's start with an NMOS.



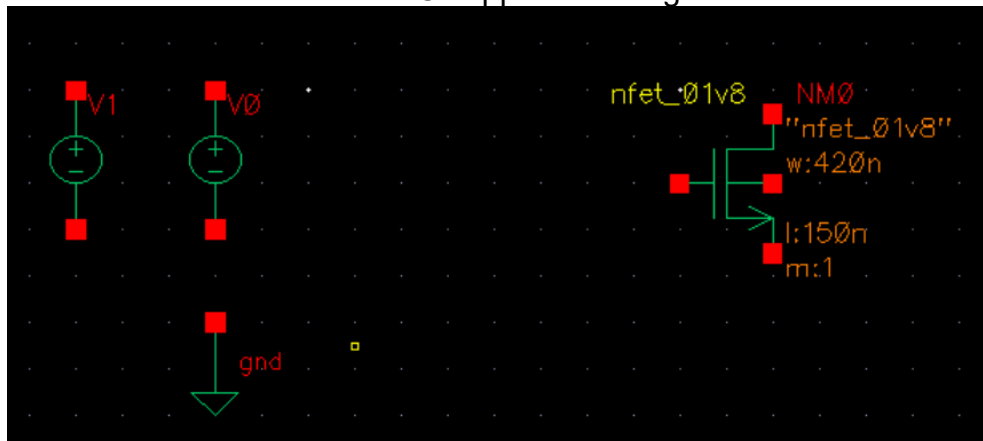
Select the cell and left click on the schematic to place it.



3. We also need to add voltage sources and ground to run the simulation. They can be found in the cadence library analogLib. DC voltage source is called vdc and ground is called gnd.



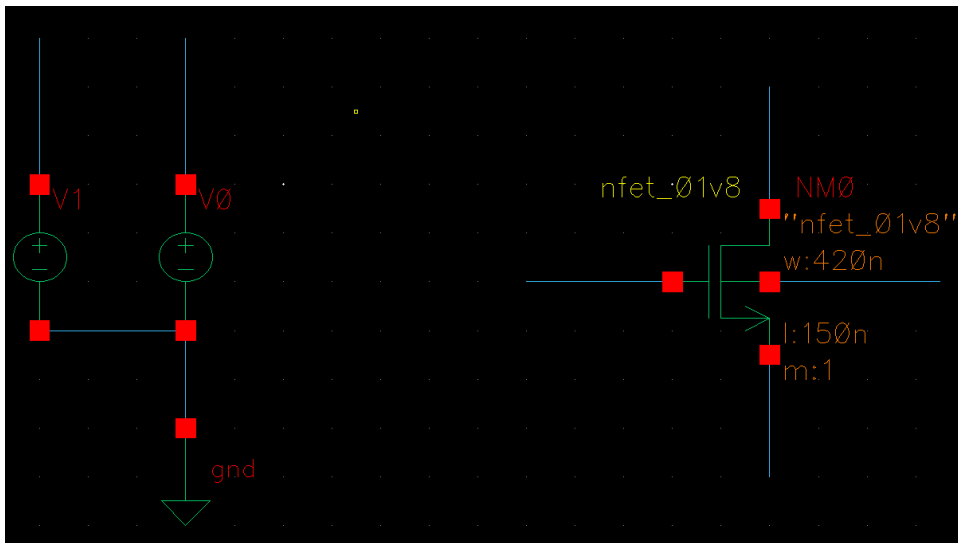
We need to instantiate two DC supplies and a ground in this simulation.



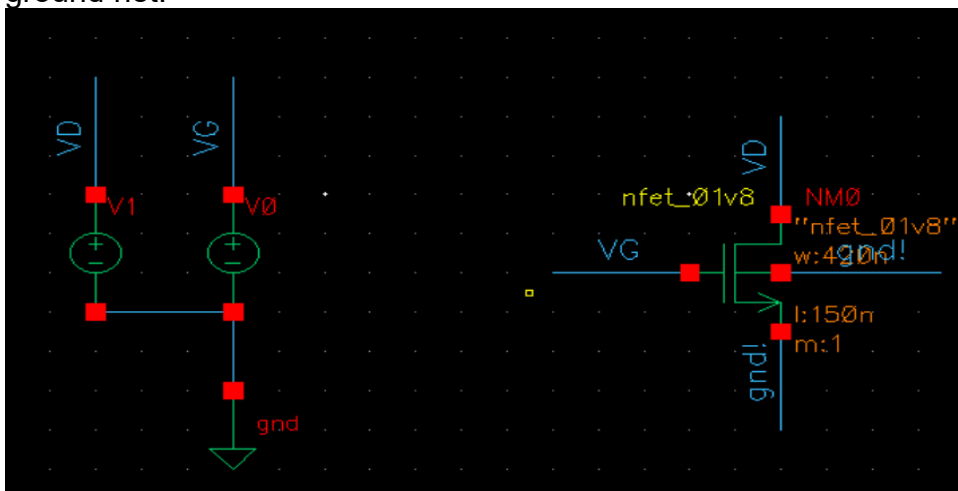
Summary of often used schematic shortcuts:

- scroll: zoom the schematic
- shift/ctrl + scroll: pan vertically/horizontally
- F: zoom to fit
- M: move instances
- del: delete instances

4. Next step is to wire the schematic. Use shortcut W and then click on schematic to create wires. Connect the negative terminals of vdc to ground and lead out the other terminals:



After that, use shortcut L to label the wires. The wires with the same label shall form a connection. In this experiment, we label the voltage sources as VG and VD and connect to the gate and drain of NMOS respectively. We also need to ground the source and bulk of NMOS, here the label gnd! denotes the global ground net:



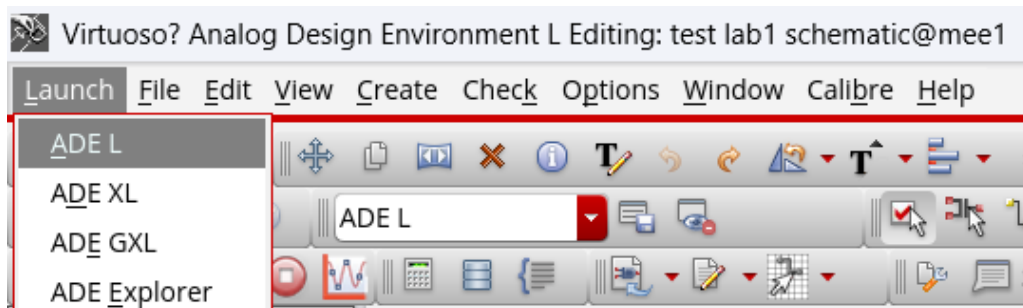
Before running simulations, we have to assign values to the voltage sources. Click on the voltage source and press q to edit its properties. In the pop-up window, enter vg in the term DC voltage for the VG source and enter vd for the VD source. Here the lower-case vg and vd represent a design variable for simulation.



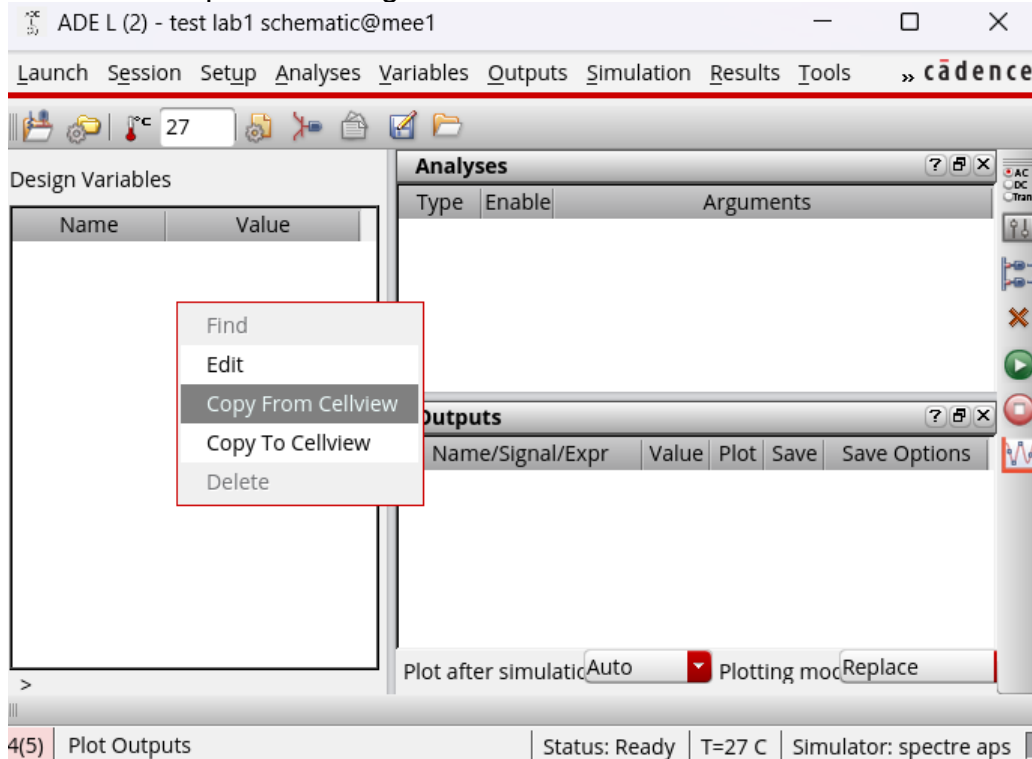
5. Now the schematic is completed! You can use shift + x to save and check the schematic to avoid missing connections. Always use shift + x after you have modifications to your schematic.

Running simulations

1. On the schematic editor toolbar, click Launch -> ADE L to start the simulation environment.



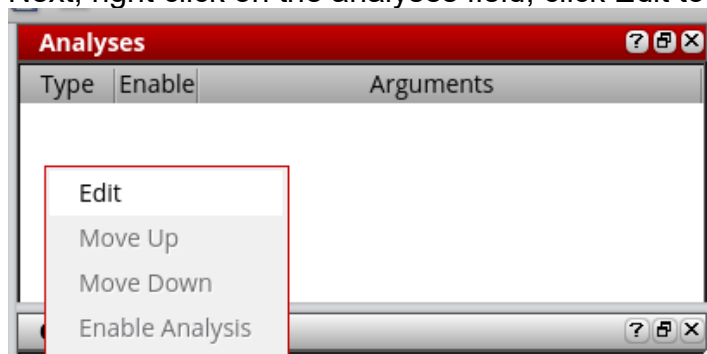
2. Right click on the design variables field of ADE L windows, click Copy From Cellview to import the design variables.



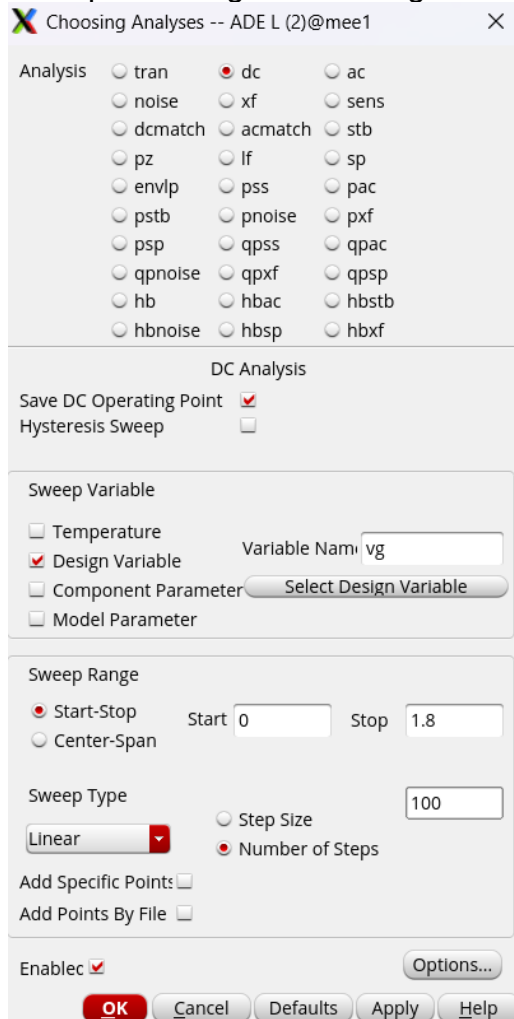
Set set vd at 1.4V in this experiment, this is to ensure that the NMOS works in saturation and minimize early effect.

Design Variables	
Name	Value
1 vd	1.4
2 vg	0

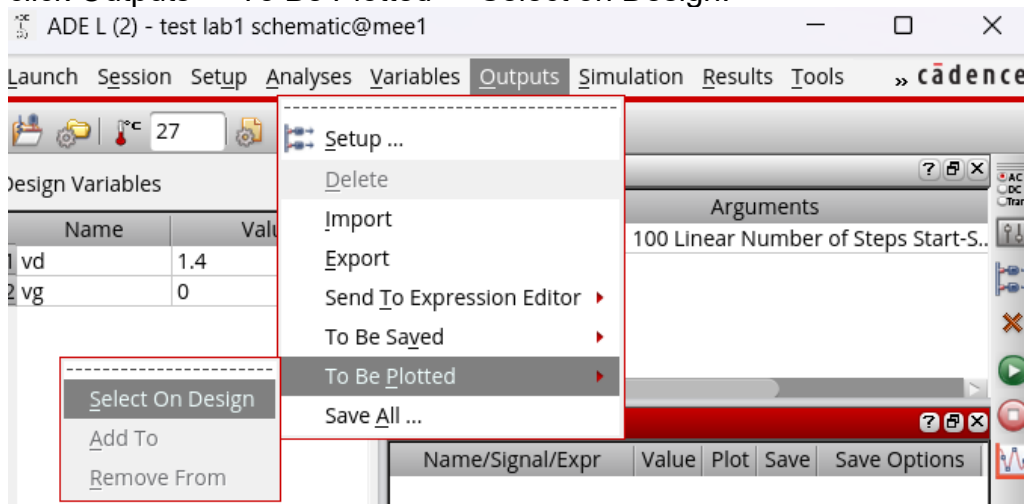
3. Next, right click on the analyses field, click Edit to add an analysis.



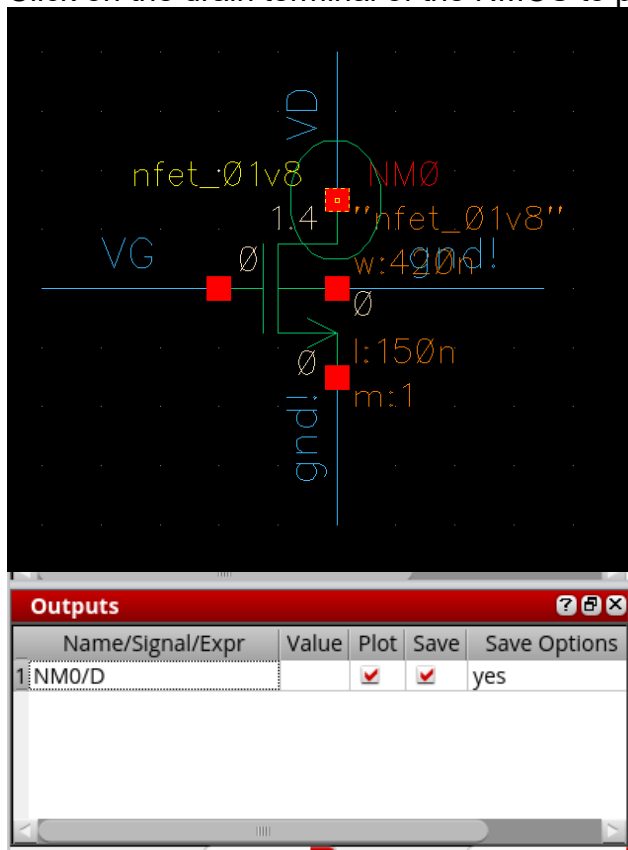
4. Choose DC simulation and save DC operation point. Save DC operation points. Sweep the design variable vg from 0 to 1.8V.



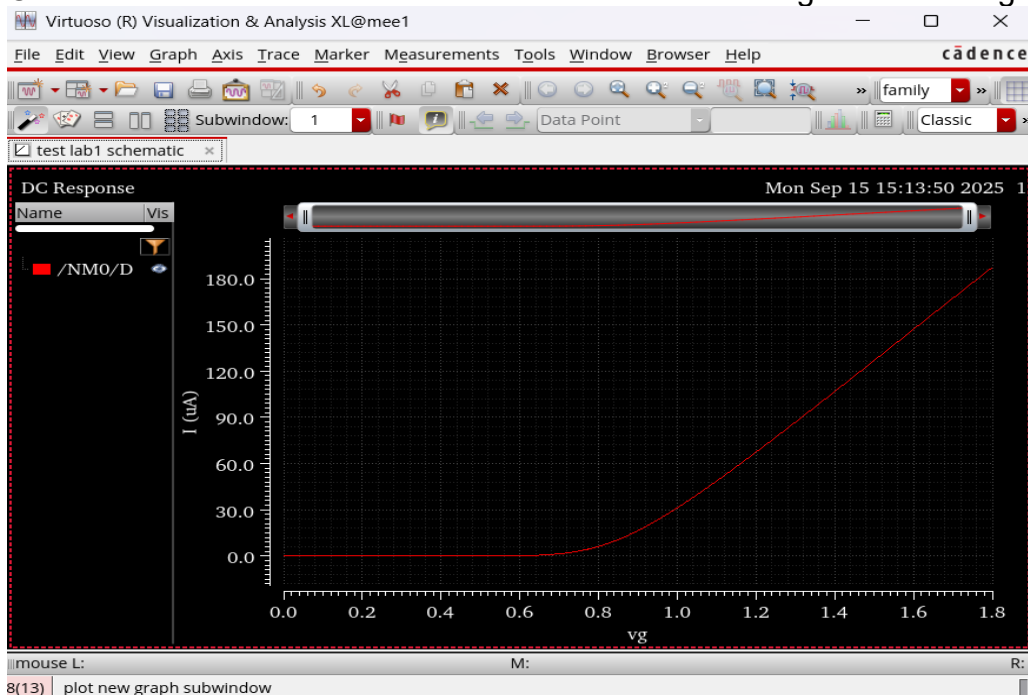
5. We still need to add the signal to be plotted in simulation. On ADE L tool bar, click Outputs -> To Be Plotted -> Select on Design.



Click on the drain terminal of the NMOS to plot the drain current.



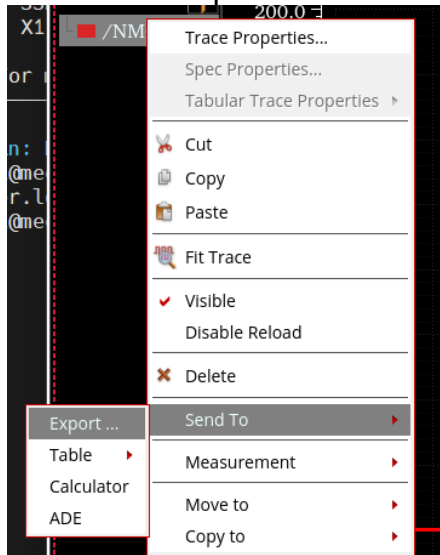
6. Click the run button  on ADE L window. And we will get the Id vs Vg curve:



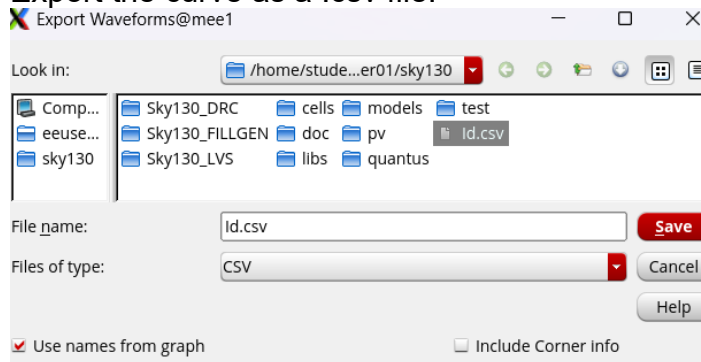
There are some useful shortcuts in the plot axis:

- M: mark a data point
- H: horizontal marker
- V: vertical marker

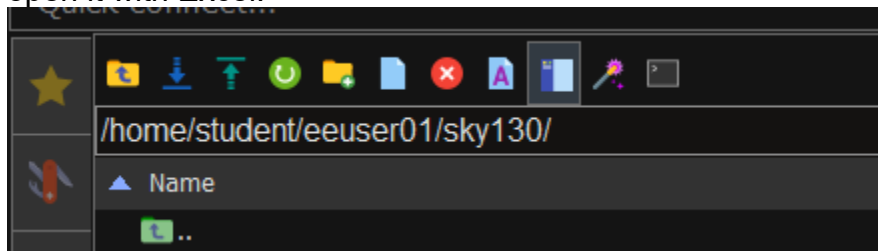
7. We can export this curve for further analysis. Right click on the curve and select Send To -> Export.

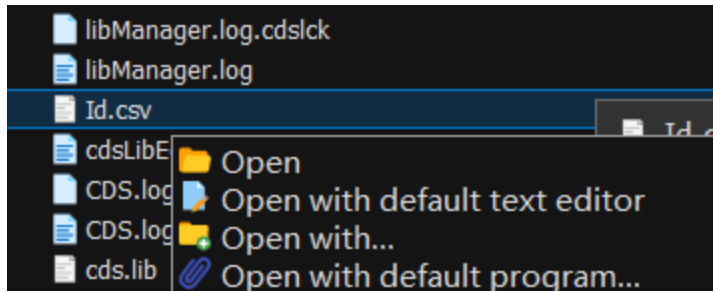


Export the curve as a .csv file:

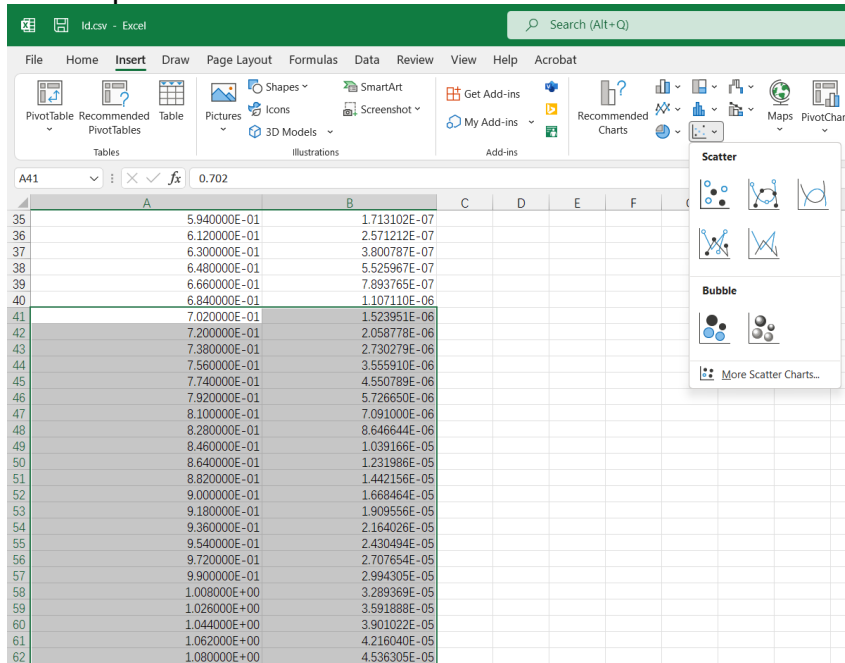


Navigate to the saved .csv file in MobaXterm file explorer, double click and open it with Excel.

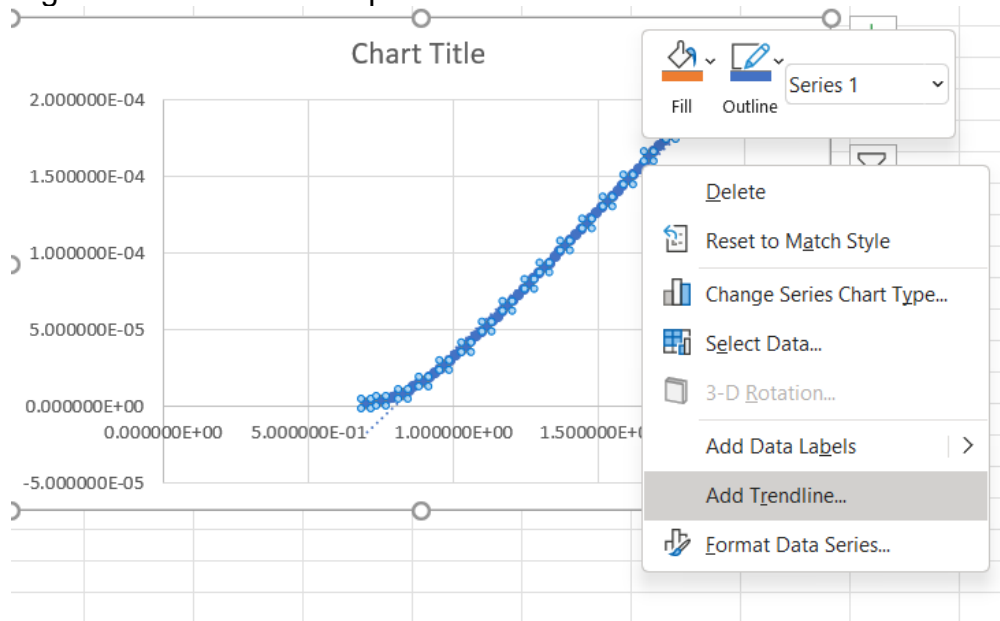




Select the data points in saturation region (V_{gs} above 0.7V) and create a scatter plot from them



Right click on the scatter plot and click Add Trendline.



On the sidebar, choose 2-order polynomial trendline and toggle display equation.

Format Trendline

Trendline Options

☐ Linear

☐ Logarithmic

☒ Polynomial Order

☐ Power

☐ Moving Average Period

Trendline Name

☒ Automatic Poly. (Series1)

☐ Custom

Forecast

Forward periods

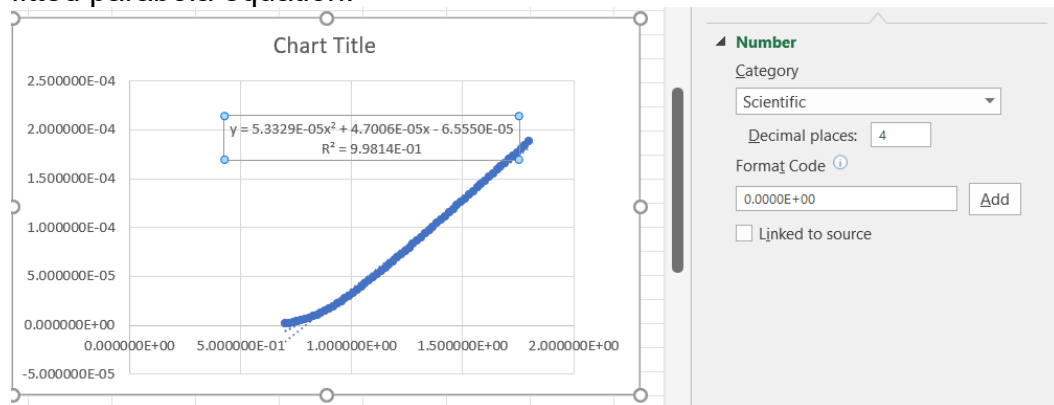
Backward periods

☐ Set Intercept

☒ Display Equation on chart

☒ Display R-squared value on chart

Format the equation label to display more decimals. Then we can see the fitted parabola equation:



Lab 1.1 Measuring MOS Characteristics: I_d vs V_{gs}

Recap in the lectures we have defined the process transconductance parameters of MOSFETs as:

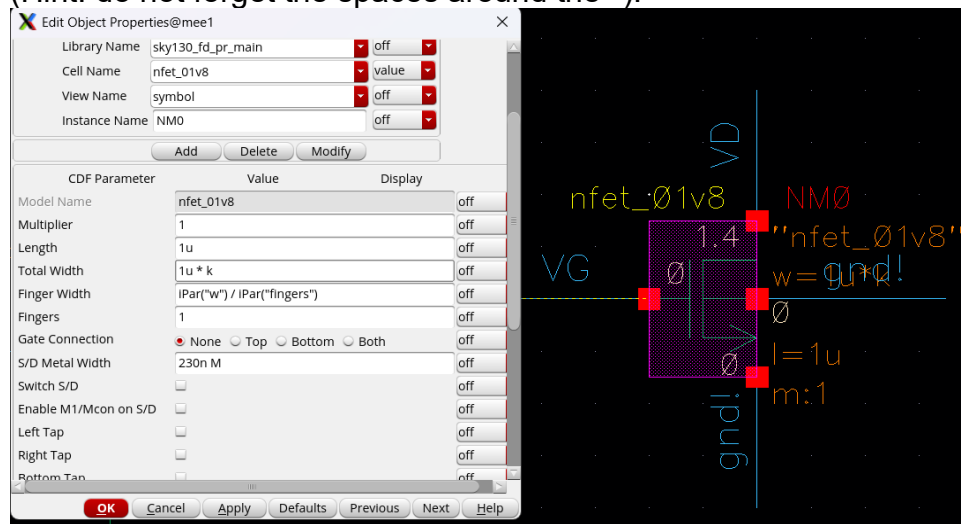
$$k'_n = \mu_n C_{ox}$$

This parameter is process-dependent and is crucial to our design. In this lab we will plot the I_d vs V_{gs} characteristics of NMOS and PMOS in this technology and fit curves to get this parameter. We will also define the aspect ratio of transistors as a design variable and sweep it in simulation.

NMOS parametric sweep

1. Use the schematic we have previously created. Select the NMOS in the schematic, then press q to edit its width and length. Here we set the length as 1u and total width as 1u * k.

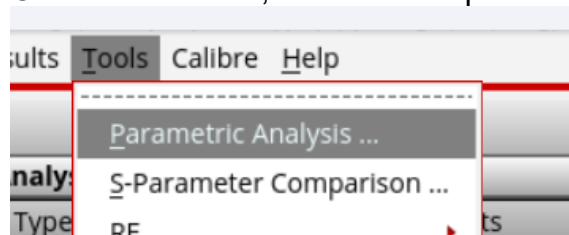
(Hint: do not forget the spaces around the *).



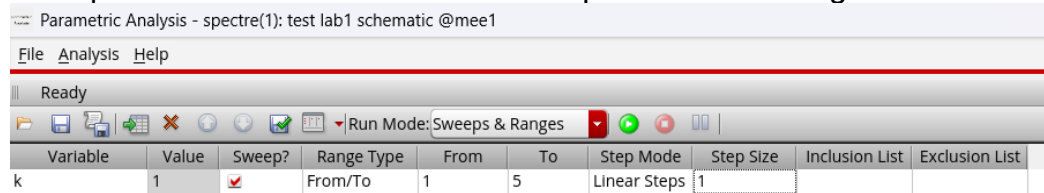
Remember to add k to ADE L and set its default to 1.

Design Variables	
Name	Value
1 k	1
2 vd	1.4
3 vg	0

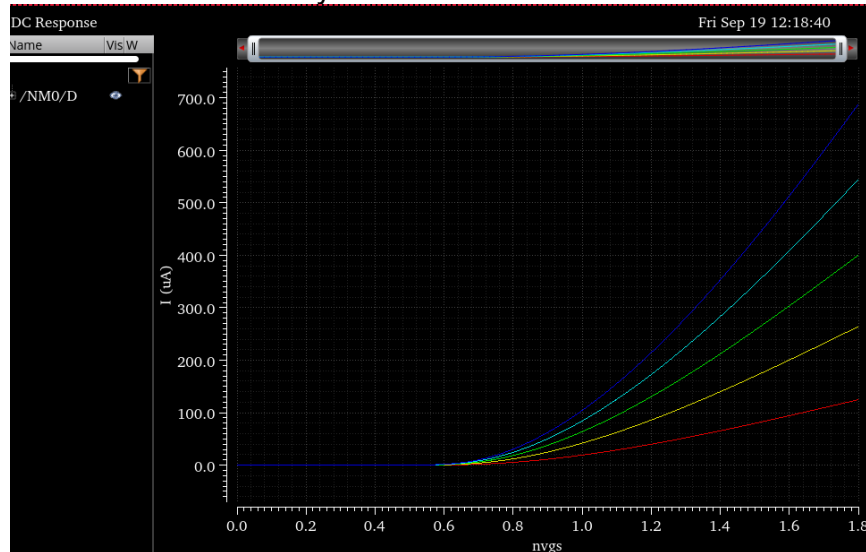
2. On ADE L toolbar, click tools -> parametric analysis



Sweep the variable k from 1 to 5 at a step of 1 and hit the green run button.

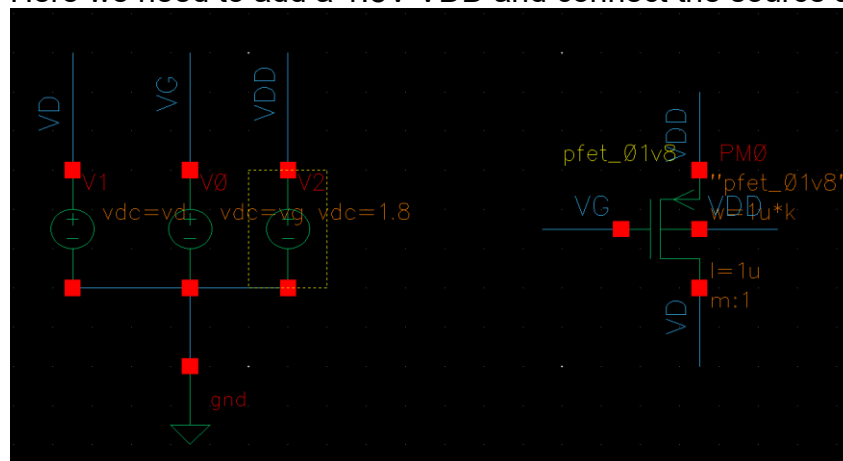


- You shall get five I_d vs V_{gs} curves. Take a screenshot and save them on your server for further analysis.



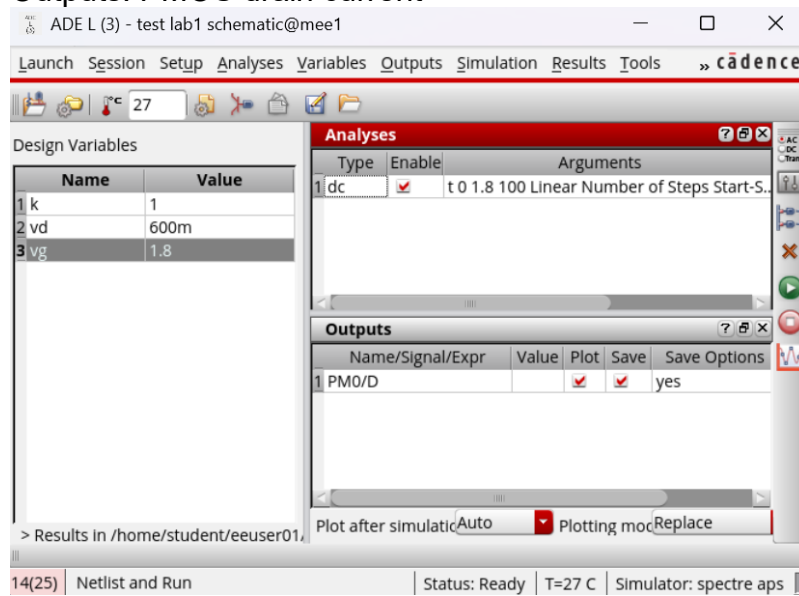
PMOS parametric sweep

- Next let's move on to PMOS simulation with the schematic below. Here we need to add a 1.8V VDD and connect the source and bulk to VDD.

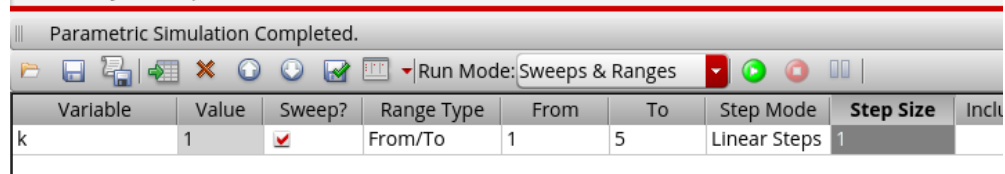


- Simulation configurations
Design Variables: Set vd at 0.6V to ensure saturation.
Analyses: Sweep vg from 0 to 1.8V

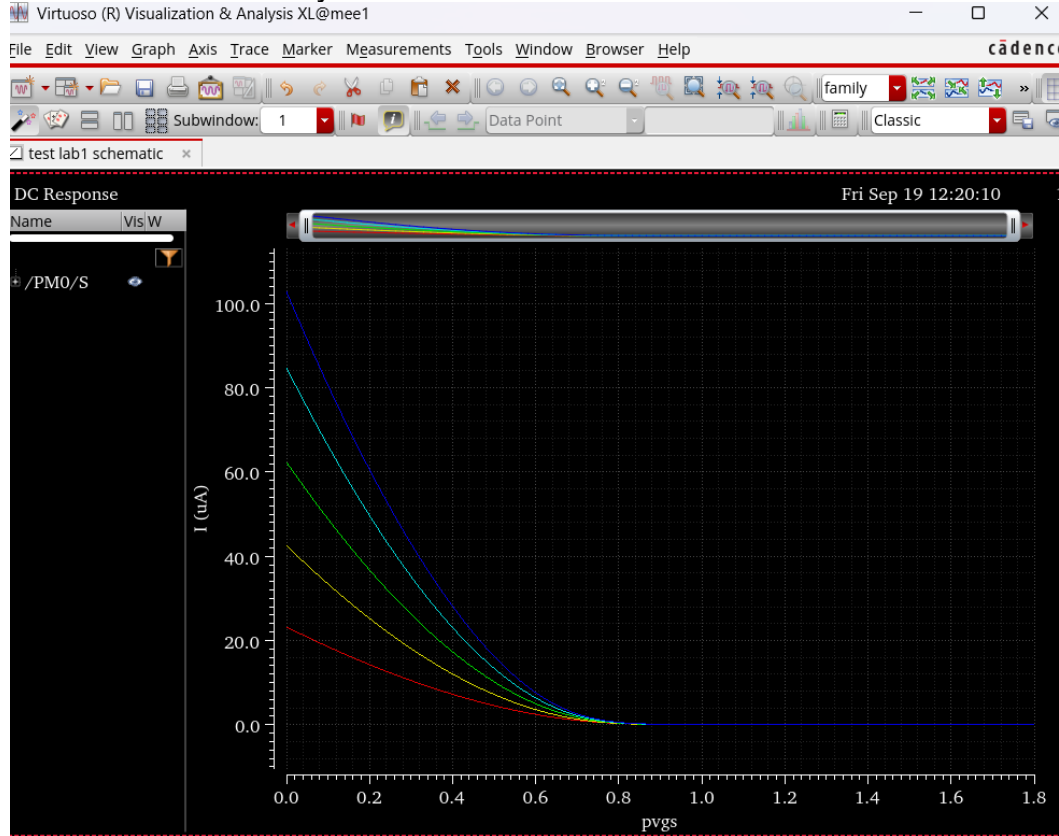
Outputs: PMOS drain current



- On ADE L toolbar, click Tools -> Parametric analysis and sweep k from 1 to 5 at a step of 1.



4. You shall get five I_d vs V_{gs} curves. Take a screenshot and save them on your server for further analysis.



Tasks

- Show your simulation waveform to TAs and save your schematic and waveform for your lab report.
- Lab1 Q1: What is the effect of increasing W/L on I_d vs V_{gs} ? (5 marks)
- Lab1 Q2: Can you fit the curves to get K_n' and K_p' ? (5 marks)

Lab 1.2 Measuring MOS Characteristics: I_d vs V_{ds}

The early effect of MOSFETs can be described by the device parameter λ . In this lab we will simulate the I_d vs V_{ds} curves of NMOS and PMOS. We will fix the aspect ratio of MOS and sweep the length to find the dependence of λ on L .

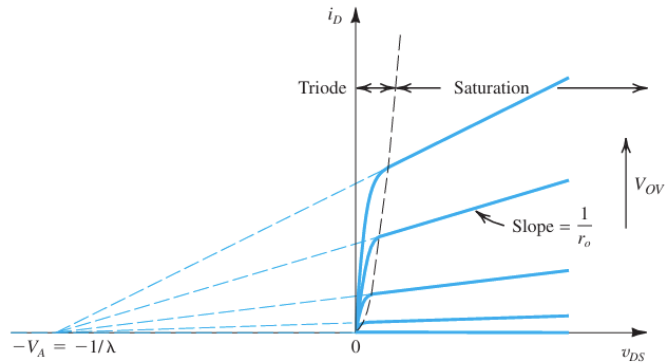
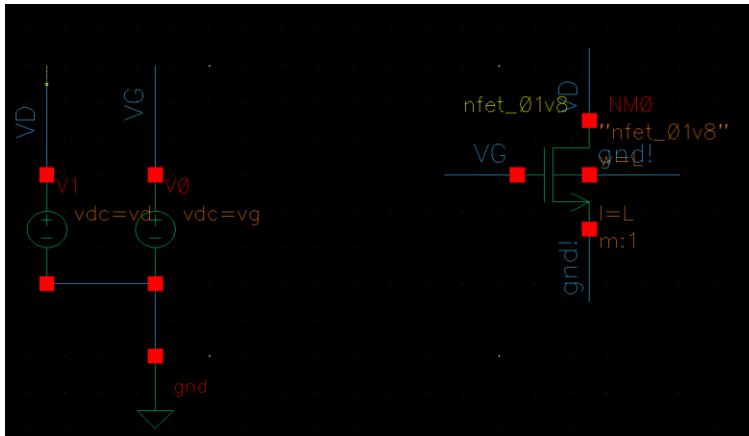


Figure 5.17 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L .

NMOS parametric sweep

1. Use the schematic below for NMOS simulation



Note that in this simulation, the aspect ratio is fixed at 1, both the length and width are defined by the design variable L .

Edit Object Properties@mee1

Property	Value	Display
Library Name	sky130_fd_pr_main	off
Cell Name	nfet_01v8	value
View Name	symbol	off
Instance Name	NM0	off

Add Delete Modify

CDF Parameter	Value	Display
Model Name	nfet_01v8	
Multiplier	1	
Length	L	
Total Width	4	

2. ADE L Settings

Design Variables: Set L at 1u. Set vg at 1.2V (or any value above threshold).

Design Variables	
Name	Value
1 L	1u
2 vd	0
3 vg	1.2

Analyses: Sweep vd from 0 to 1.8V.

Sweep Variable

☐ Temperature

☒ Design Variable Variable Name:

☐ Component Parameter

☐ Model Parameter

Sweep Range

☒ Start-Stop Start: Stop:

☐ Center-Span

Sweep Type

☒ Linear ☐ Step Size

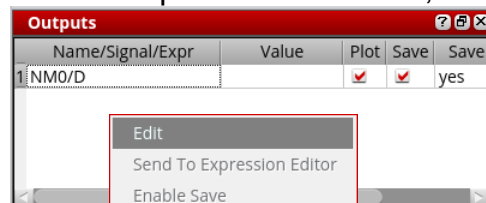
☒ Number of Steps

Outputs: First add the NMOS drain current as output.

To get the λ value, we need to use a calculator expression below:

$$\frac{\text{value}(\text{deriv}(\text{getData}("/\text{NM0/D}" ?\text{result 'dc'}})) 1.6))}{\text{value}(\text{getData}("/\text{NM0/D}" ?\text{result 'dc'}})) 1.6))}$$

You need to replace NM0 with the name of your transistor. The numerator of the expression denotes slope of the curve at $V_{ds} = 1.6V$. The denominator denotes the value of I_d at $V_{ds} = 1.6V$. To evaluate the expression, right click on the Outputs field of ADE L, click Edit.



Name the signal as lambda_n and enter its expression:

Setting Outputs -- ADE L (3)@mee1

Selected Output

Name (opt.):

Expression:

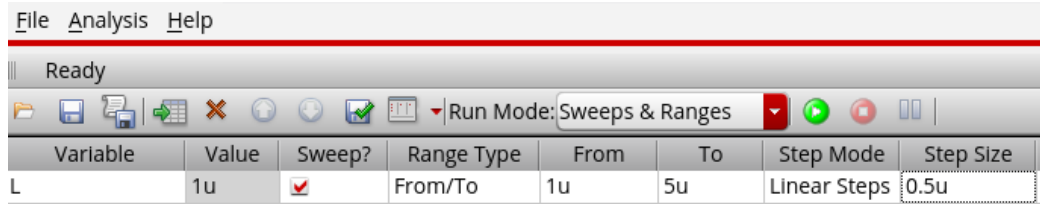
Calculator:

Will be: ☒ Plotted/Evaluated

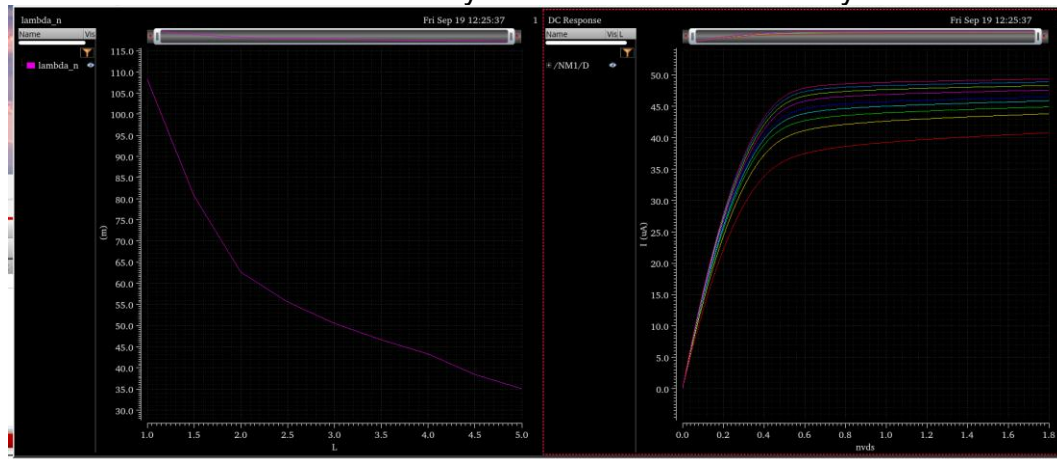
Table Of Outputs

Name/Signal/Expr	Value	Plot	Save Options
1 NM0/D		yes	yes

3. In Tools -> Parametric Analysis, sweep variable L from 1u to 5u at a step of 0.5u.

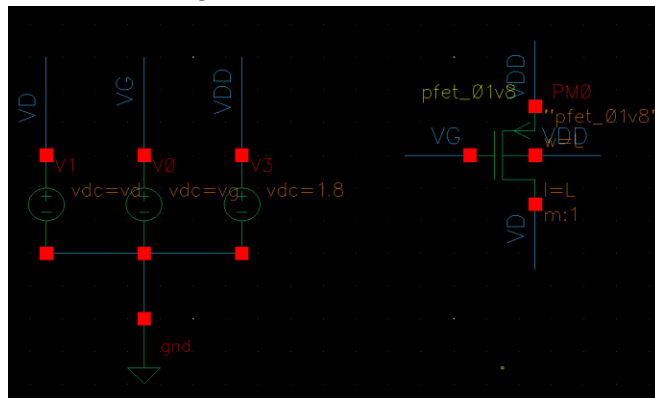


4. Run the simulation and you will get the λ vs L plot and the I_d vs V_{ds} plot. Take a screenshot and save them on your server for further analysis.

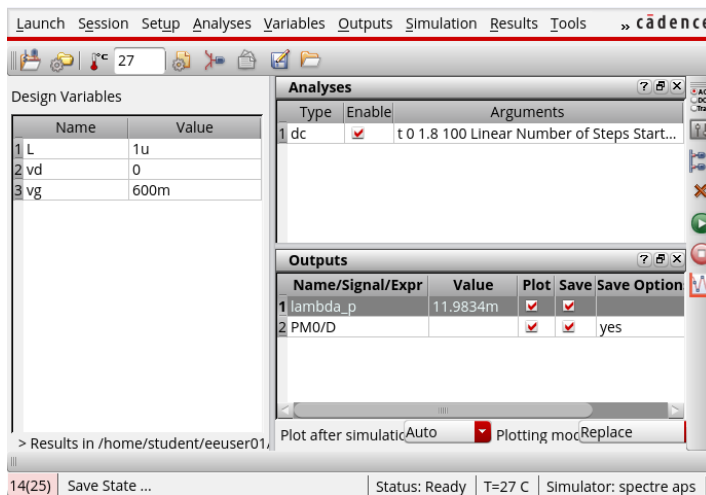


PMOS parametric sweep

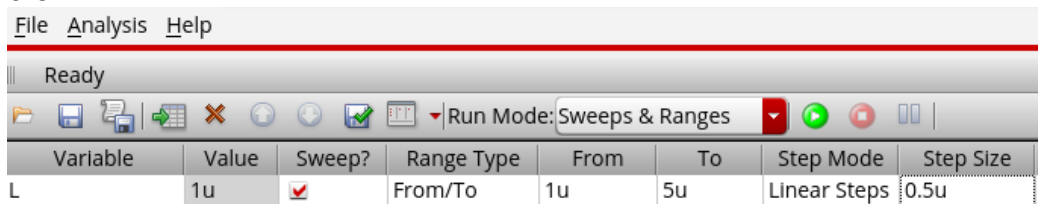
1. Build the PMOS simulation schematic below



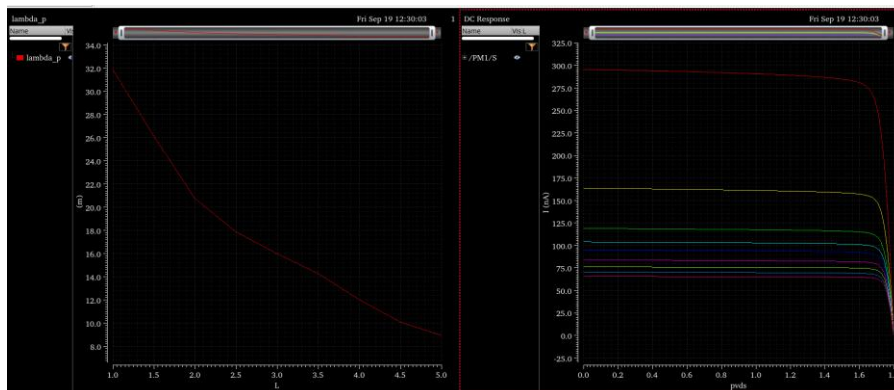
2. ADE L Settings:
 Design Variables: Set v_d at 0.6V to avoid cutoff.
 Analyses: Sweep v_d from 0 to 1.8V
 Outputs:
 First add the PMOS drain current.
 $\lambda_{p_} : (- (\text{value}(\text{deriv}(\text{getData}("/\text{PM0}/\text{D}")) ? \text{result 'dc'}) 0.2) / \text{value}(\text{getData}("/\text{PM0}/\text{D}")) ? \text{result 'dc'}) 0.2))$



- In Tools -> Parametric Analysis, sweep variable L from 1u to 5u at a step of 0.5u.



- Run the simulation and you will get the λ vs L plot and the I_d vs V_{ds} plot. Take a screenshot and save them on your server for further analysis.

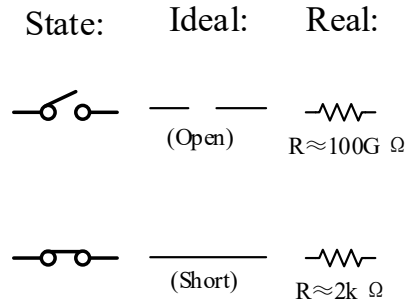


Tasks

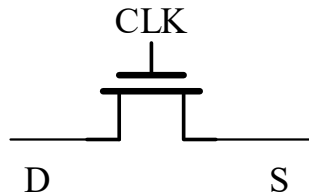
- Show your simulation waveform to TAs and save your schematic and waveform for your lab report.
- Lab1 Q3: What is effect of increasing L with fixed W/L on I_d vs V_{ds} ? (5 marks)
- Lab1 Q4: Can you fit curves to get dependence of λ on L? (5 marks)

Lab 1.3 Simulating MOS Switches

Switch is an important component in modern large-scale integrated circuits. An ideal circuit of the switch is as follows:



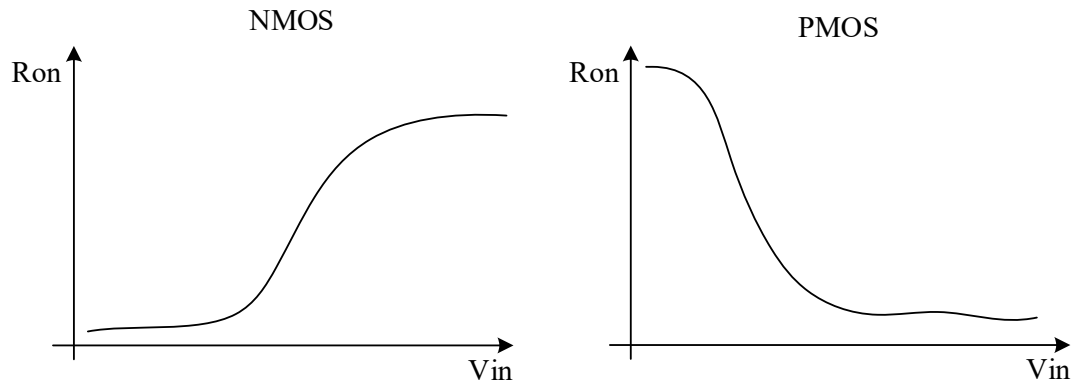
We want an ideal switch which has an infinite resistance when it open, an zero resistance when it closes. In fact, when CMOS switch open, the equivalent resistance is not 0, and the resistance value is affected by the input voltage. Consider an NMOS switch:



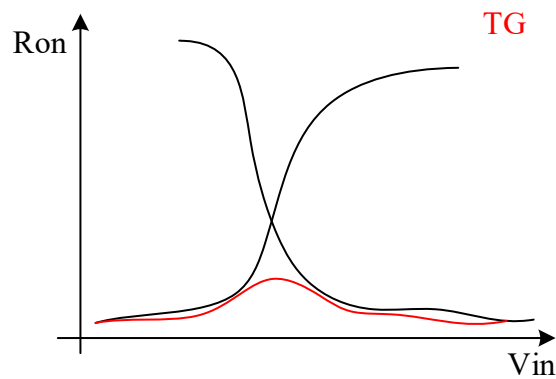
The current formula of NMOS in the deep linear region is:

$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} [(V_{DD} - V_{in}) - V_{th}]} = \frac{1}{k[V_{DD} - V_{in} - V_{th}]}$$

When the gate voltage of an NMOS switch is fixed at VDD and the input voltage gradually increases from 0, its on-resistance changes as follows: Initially, with a low input voltage, the NMOS is strongly on, and the resistance remains low and relatively stable. As the input voltage continues to rise, the gate-source voltage decreases, and the on-resistance begins to slowly increase. When the input voltage approaches the difference between VDD and the threshold voltage (VDD - Vth), the resistance enters a nonlinear, rapidly increasing region. Finally, when the input voltage exceeds this critical value, the NMOS enters the cutoff region, the on-resistance becomes extremely large, and the switch is effectively turned off. This process exhibits a distinct nonlinear characteristic, resulting in significant degradation of NMOS performance when transmitting high levels. We can roughly draw the resistance change curve:



The on resistance of a transmission gate (TG) varies noticeably with the input voltage V_{in} when V_{in} is near the low level, conduction is mainly provided by the NMOS, resulting in a small resistance; when V_{in} is near the high level, conduction is mainly provided by the PMOS, also yielding a small resistance. In the mid-level region, however, both NMOS and PMOS drive weakly, so their resistances are relatively large, causing the overall transmission resistance to reach its maximum. Therefore, the TG's on-resistance exhibits a “U-shaped” dependence on the input voltage—minimal at both ends and maximal in the middle.



In this experiment we will:

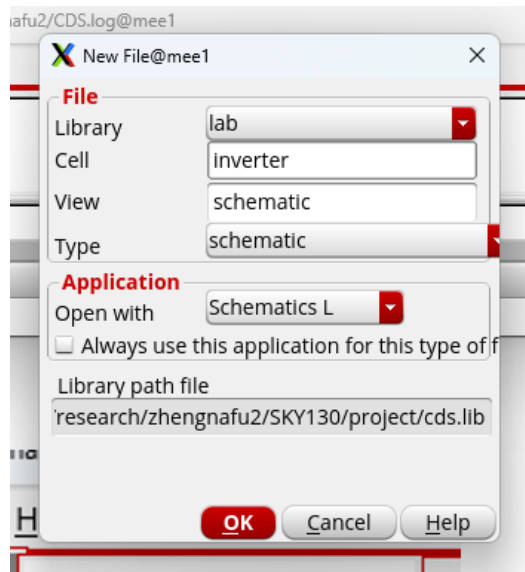
1. Build NMOS switch, PMOS switch, Transmission Gate schematic.
2. Build an inverter and its symbol.
3. Build testbench for each switch.
4. Simulate the resistance of each switch using transient analysis based on ADE L.

(transient analysis based on V_{in} at $V_{DD}/2$)

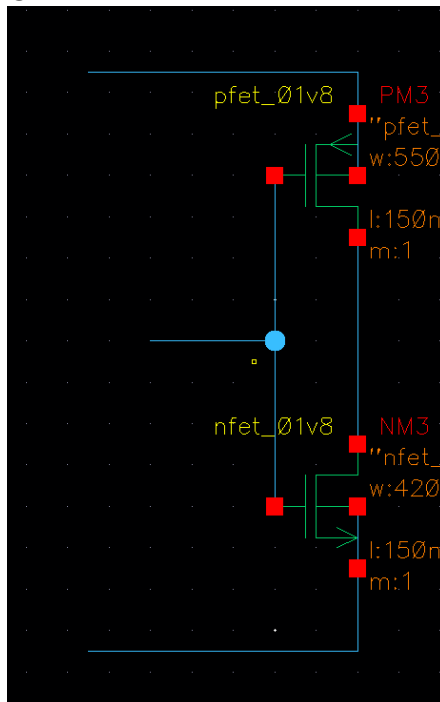
(Using AC or SP simulation to simulate resistance is a bonus for experimental exploration)

Creating an Inverter Cell

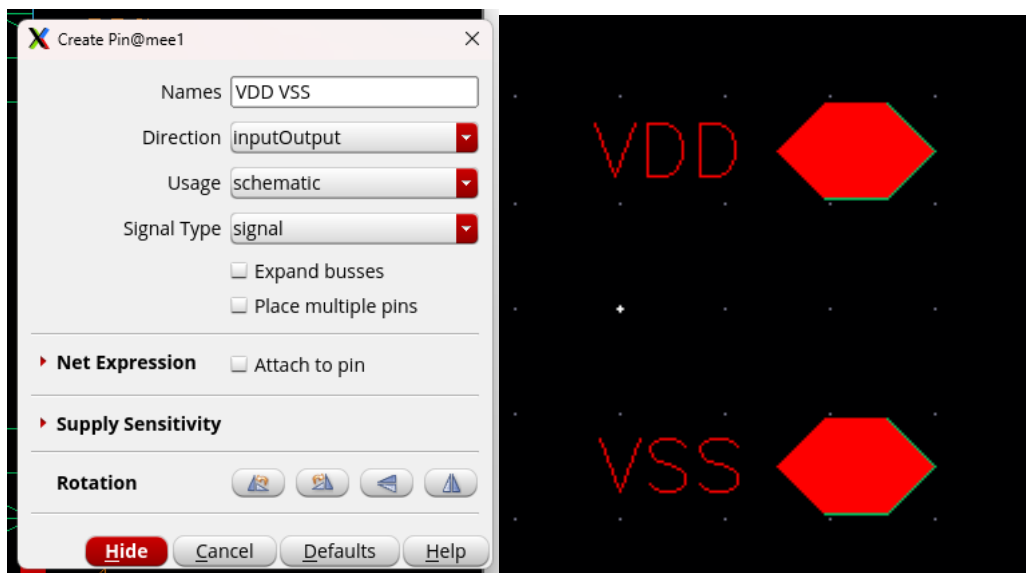
1. To create the inverted clock inputs for transmission gate, we need to build an inverter cell:



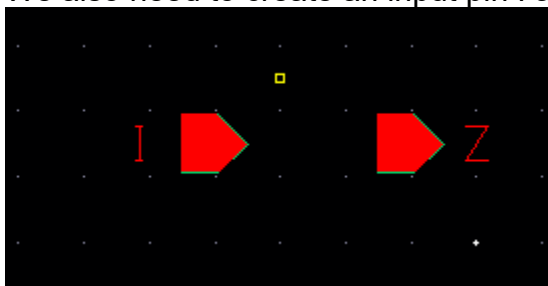
2. Create the inverter schematic below in this cell:



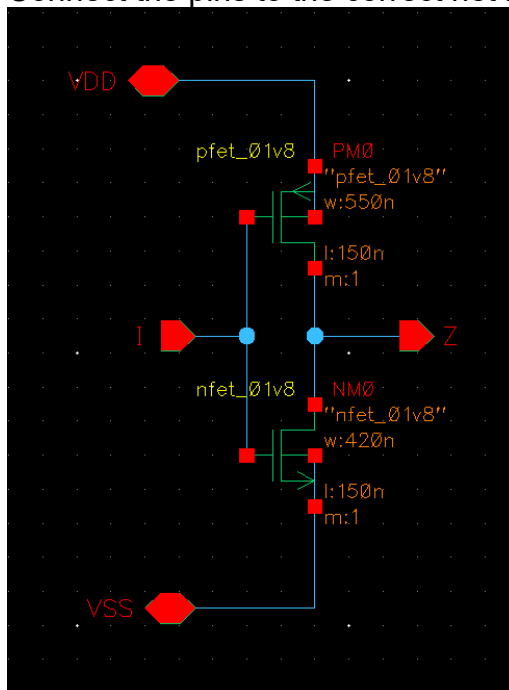
3. To create a symbol for the cell, we need to create pins for the inverter. First use shortcut **P** to create two pins named VDD and VSS. Attach them to the correct nets on the schematic.



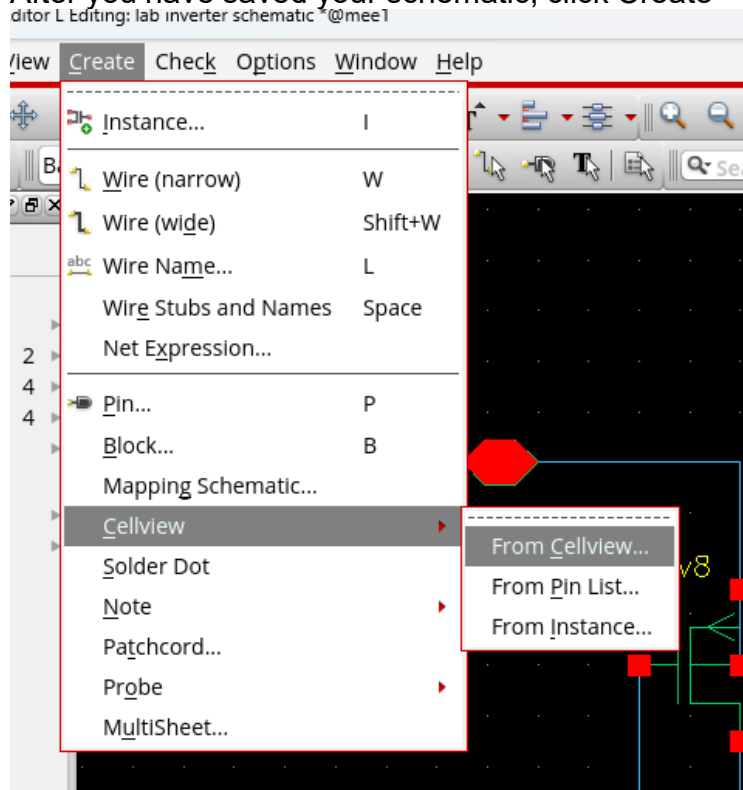
We also need to create an input pin I and an output pin Z.



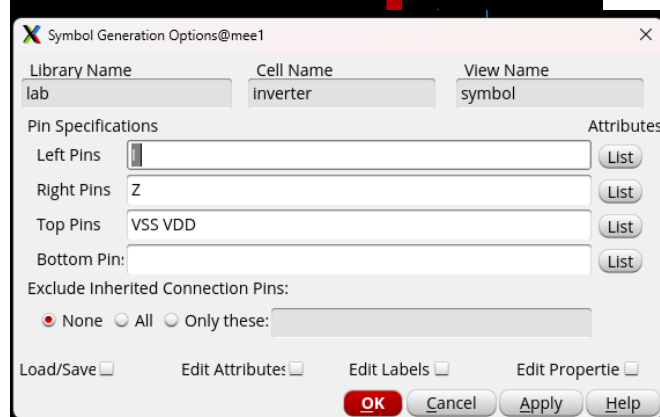
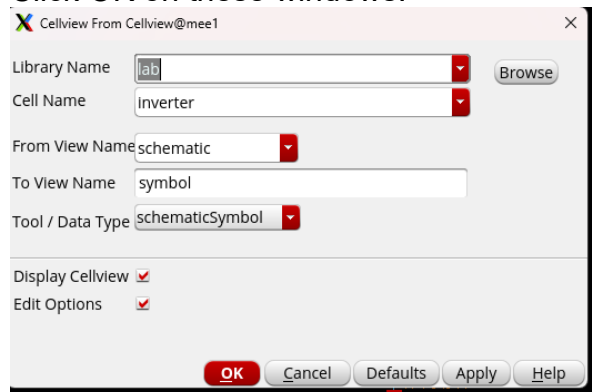
Connect the pins to the correct net like this:



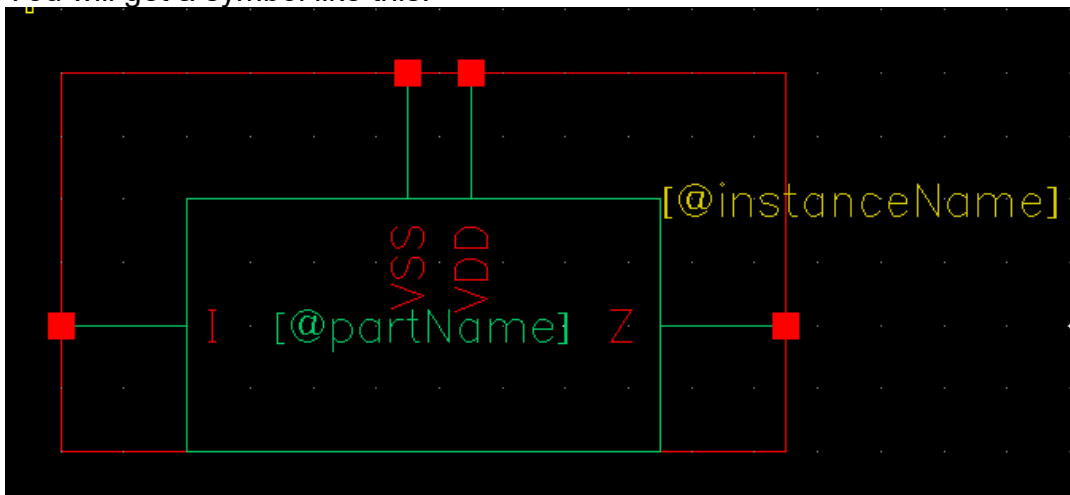
4. After you have saved your schematic, click Create -> Cellview -> from Cellview



Click OK on these windows:



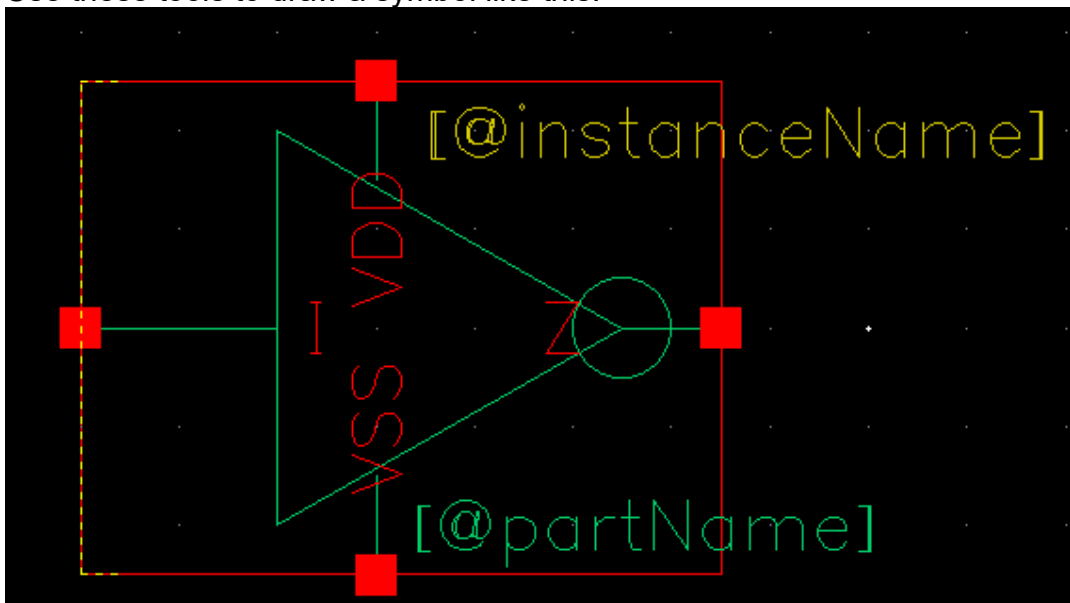
You will get a symbol like this:



On the toolbar are some drawing tools:



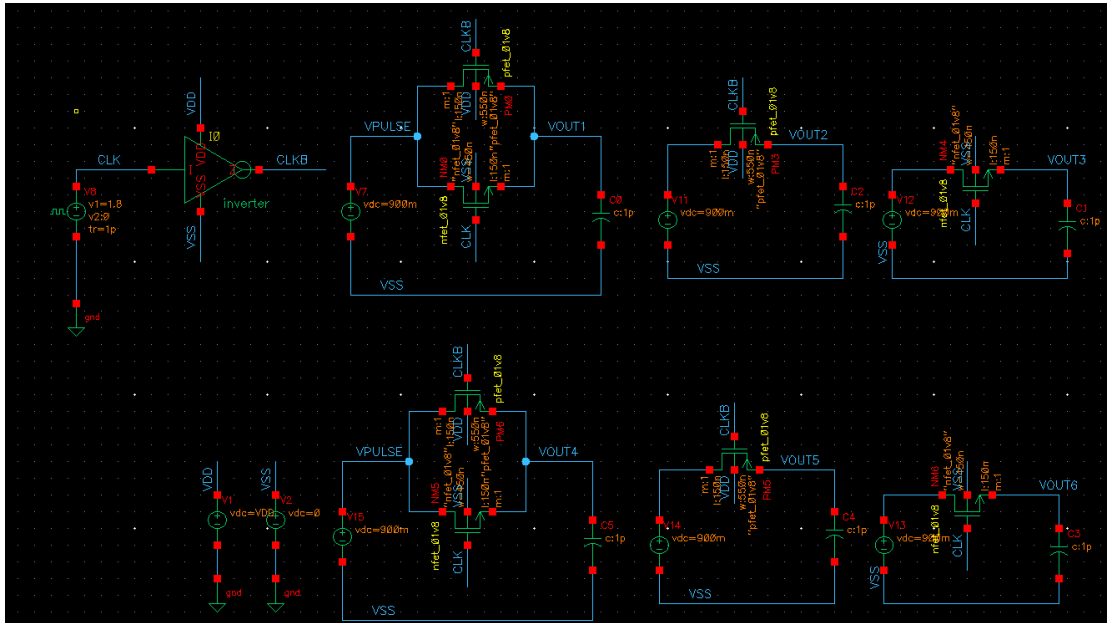
Use these tools to draw a symbol like this:



Now you can reference this inverter cell in your simulations.

Transient Simulation of MOS Switches

1. Create the schematic below for MOS transient simulations:



A few points to note

nfet and pfet: currently sized 550n/150n, 420n/150n repressively, you can change by yourself.

V0: cell vpulse from analogLib with the following settings

Property	Value	Display
Library Name	analogLib	off
Cell Name	vpulse	off
View Name	symbol	off
Instance Name	V0	off
Apply To: only current Instance		
Show ☐ system ☒ user ☒ CDF		
Browse Reset Instance Labels Display		
Add Delete Modify		
User Property	Master Value	Local Value
Ignore	TRUE	off
CDF Parameter Value Display		
Frequency name for 1/peri		off
Noise file name		off
Number of noise/freq pairs	0	off
DC voltage		off
AC magnitude		off
AC phase		off
XF magnitude		off
PAC magnitude		off
PAC phase		off
Voltage 1	1.8 V	off
Voltage 2	0 V	off
Period	2u s	off
Delay time		off
Rise time	1p s	off
Fall time	1p s	off
Pulse width	1u s	off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off
Type of rising & falling edge		off

OK

Cancel

Apply

Defaults

Previous

Next

Help

V3-8: Cell vdc from analogLib with 0.9V dc voltage

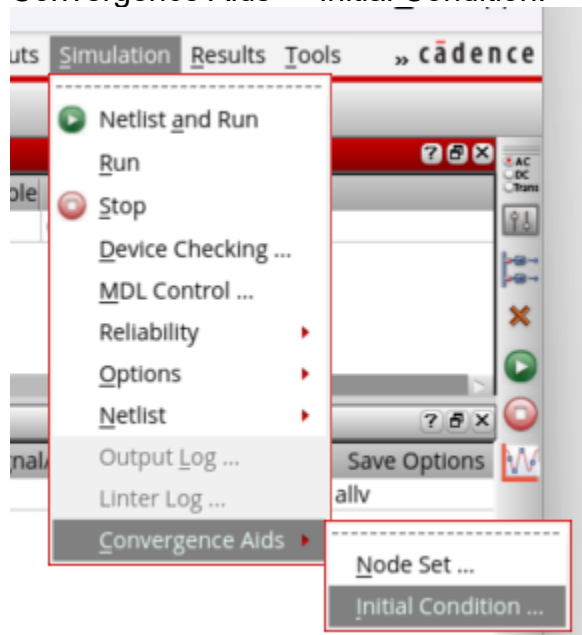
Apply To	only current ☒ instance ☒		
Show	☐ system ☒ user ☒ CDF		
Browse Reset Instance Labels Display			
Property	Value	Display	
Library Name	analogLib	off ☒	
Cell Name	vdc	off ☒	
View Name	symbol	off ☒	
Instance Name	V6	off ☒	
Add Delete Modify			
User Property	Master Value	Local Value	Display
lvignore	TRUE		off ☒
CDF Parameter Value Display			
Noise file name		off ☒	
Number of noise/freq pairs	0	off ☒	
DC voltage	900m V	off ☒	
AC magnitude		off ☒	
AC phase		off ☒	
XF magnitude		off ☒	
PAC magnitude		off ☒	
PAC phase		off ☒	
Temperature coefficient 1		off ☒	
Temperature coefficient 2		off ☒	
Nominal temperature		off ☒	
OK Cancel Apply Defaults Previous Next Help			

Capacitors: 1p capacitors from analogLib

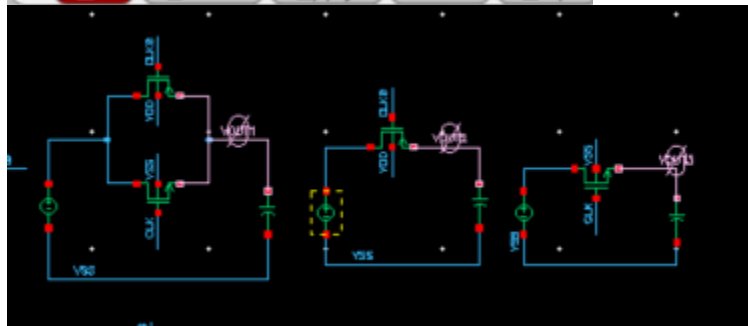
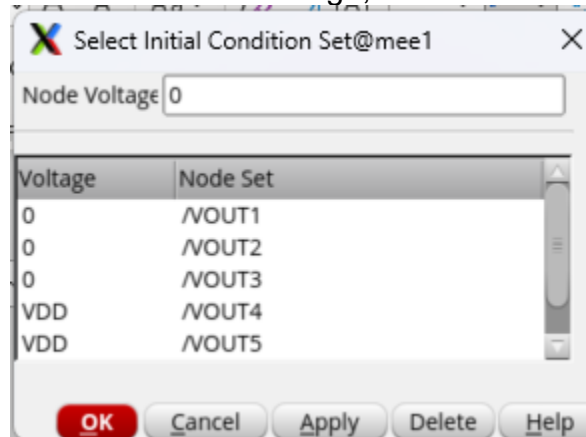
Apply To	only current ☒ instance ☒		
Show	☐ system ☒ user ☒ CDF		
Browse Reset Instance Labels Display			
Property	Value	Display	
Library Name	analogLib	off ☒	
Cell Name	cap	off ☒	
View Name	symbol	off ☒	
Instance Name	C0	off ☒	
Add Delete Modify			
CDF Parameter Value Display			
Model name		off ☒	
Capacitance	1p F	off ☒	
Width		off ☒	
Length		off ☒	
Multiplier		off ☒	
Scale factor		off ☒	
Temp rise from ambient		off ☒	
Initial condition		off ☒	
Temperature coefficient 1		off ☒	
Temperature coefficient 2		off ☒	
Number of Polynomial Coe	0	off ☒	
Capacitor Area		off ☒	
Capacitor Perimeter		off ☒	
OK Cancel Apply Defaults Previous Next Help			

2. ADE L Settings

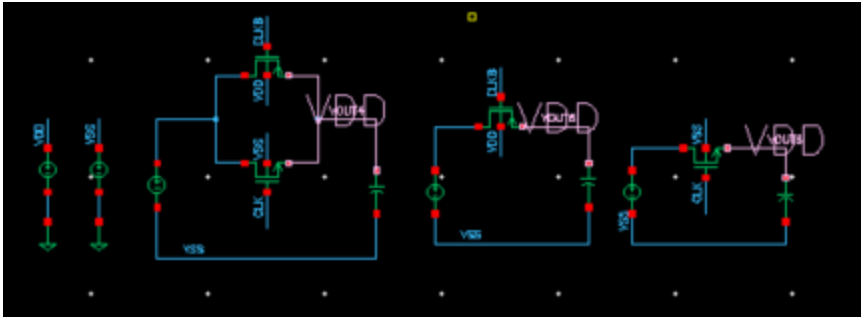
Initial Conditions: In this lab we simulate two initial conditions for each switch, one at VDD and one at 0. To set initial conditions, click Simulation -> Convergence Aids -> Initial Condition.



Enter 0 for Node Voltage, click VOUT1-3 on the schematic.



Then enter VDD and click on VOUT4-6



Design Variables:

Design Variables	
Name	Value
1 VDD	1.8

Analyses: Add a transient analysis with the below configuration

Analysis

☒ tran ☐ dc ☐ ac

☐ noise ☐ xf ☐ sens

☐ dcmatch ☐ acmatch ☐ stb

☐ pz ☐ lf ☐ sp

☐ envlp ☐ pss ☐ pac

☐ pstb ☐ pnoise ☐ pxf

☐ psp ☐ qpss ☐ qpac

☐ qpnoise ☐ qpxf ☐ qpss

☐ hb ☐ hbac ☐ hbstb

☐ hbnoise ☐ hbasp ☐ hbxf

Transient Analysis

Stop Time

Accuracy Defaults (errpreset)

☒ conservative ☐ moderate ☐ liberal

☐ Transient Noise

Dynamic Parameters ☐

Enable ☒

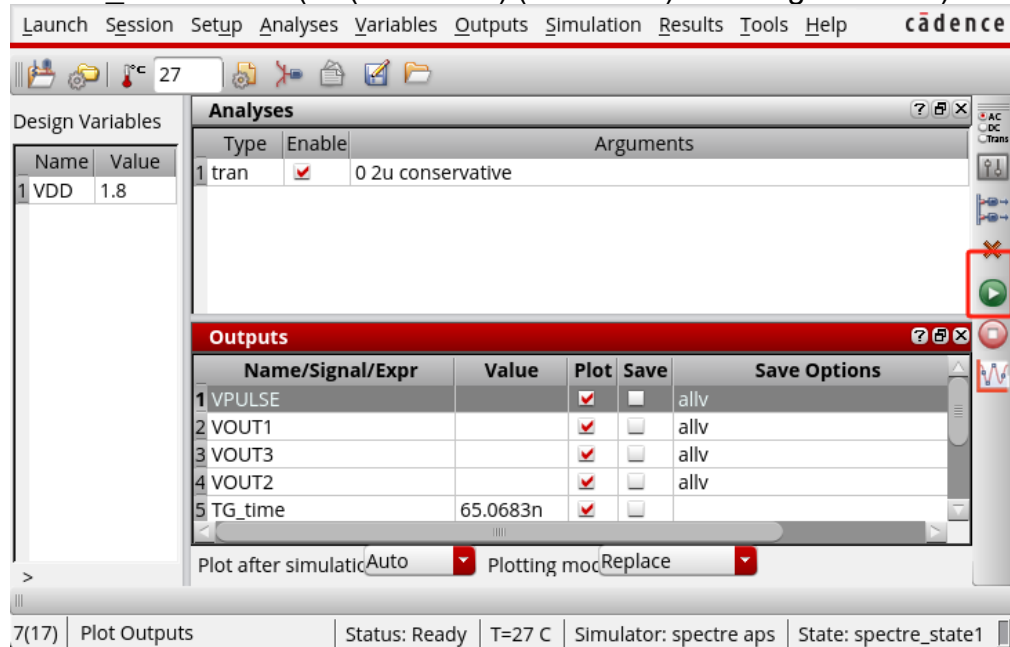
Options...

Outputs:

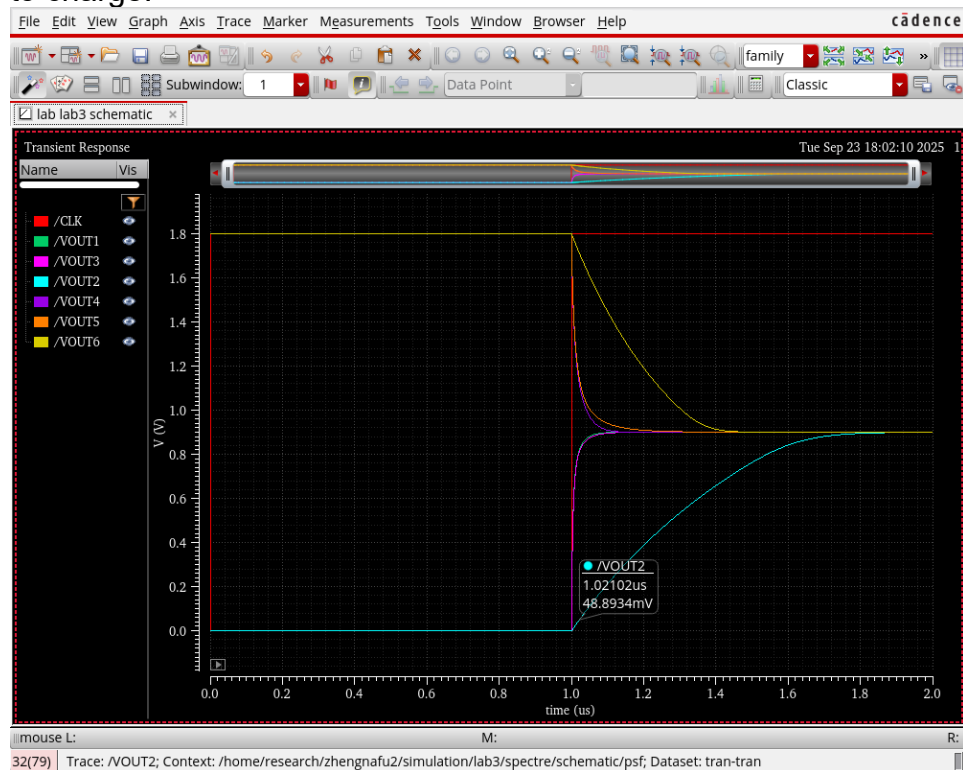
First use outputs -> to be plotted -> select on design to plot CLK and VOUT1-6, then add the other expressions

TG_time: cross(VT("/VOUT1") (0.9 * 0.99) 1 "rising" nil nil nil) - 1e-06

PMOS_time: cross(VT("/VOUT2")) (0.9 * 0.99) 1 "rising" nil nil nil) - 1e-06
 NMOS_time: cross(VT("/VOUT3")) (0.9 * 0.99) 1 "rising" nil nil nil) - 1e-06
 TG_time2: cross(VT("/VOUT4")) (0.9 * 1.01) 1 "falling" nil nil nil) - 1e-06
 PMOS_time2: cross(VT("/VOUT5")) (0.9 * 1.01) 1 "falling" nil nil nil) - 1e-06
 NMOS_time2: cross(VT("/VOUT6")) (0.9 * 1.01) 1 "falling" nil nil nil) - 1e-06



- Run the simulation, you will get the transient waveforms and the time needed to charge:



	Name/Signal/Expr	Value	Plot	Save	
1	CLK		☒	☐	allv
2	VOUT1		☒	☒	allv
3	VOUT3		☒	☒	allv
4	VOUT2		☒	☒	allv
5	TG_time	64.8233n	☒	☐	
6	PMOS_time	760.668n	☒	☐	
7	NMOS_time	80.4543n	☒	☐	
8	VOUT4		☒	☒	allv
9	VOUT5		☒	☒	allv
10	VOUT6		☒	☒	allv
11	TG_time2	99.9766n	☒	☐	
12	PMOS_time2	197.425n	☒	☐	
13	NMOS_time2	413.54n	☒	☐	

Tasks

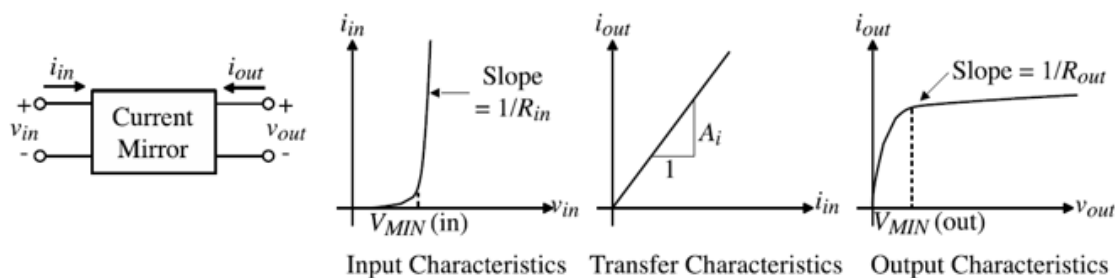
- Show your simulation waveform to TAs and save your schematic and waveform for your lab report.
- Lab1 Q5: Show your schematic and simulation waveform for three types of switches. Comment on the transient behavior of three types of switches and explain. (10 marks)
- Lab1 Q6: Start with a hand calculation, change the transistor size to reduce the charging time of TG within 10ns. (5 marks)

Lab 2: Current Mirror and Common Source

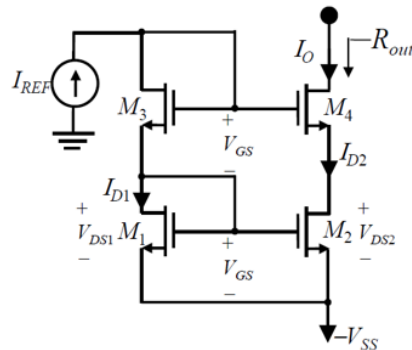
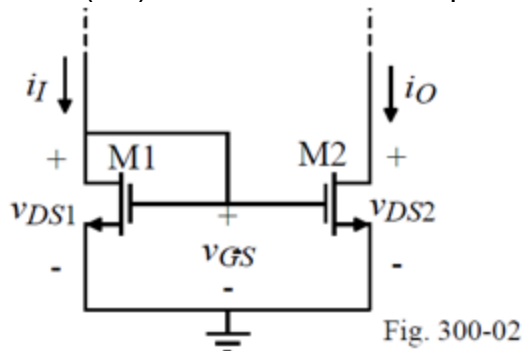
Lab 2.1 Current Mirrors

A current mirror replicates the input current of a current sink or current source as an output current. The output current may be identical to the input current or can be a scaled version of it.

For an ideal current source, the output resistance and the output voltage range are infinity. But for real transistors circuits, the minimum output voltage is limited and output resistance is not infinity.

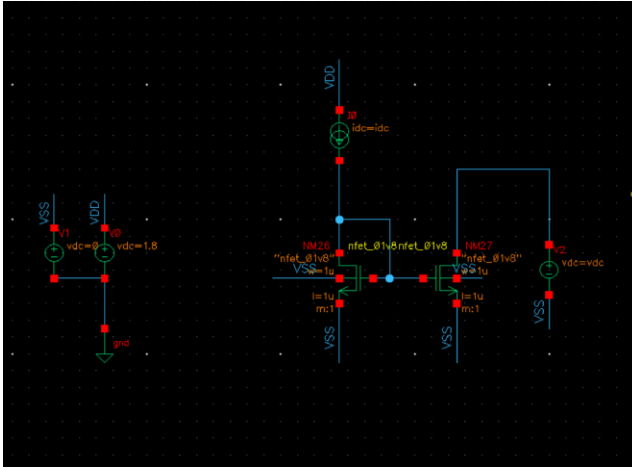


In this lab, we will simulate a simple current mirror (left) and a cascode current mirror (right) and measure the output characteristics of both circuits.



Measuring output resistance

1. Draw the schematic below for current mirror simulations:
V0 V1: Cell vdc from analogLib, set VSS to 0 and VDD to 1.8V
I0 I2: Cell idc from analogLib, set dc current as a design variable idc.
V2 V3: Cell vdc from analogLib, set dc current as a design variable vdc.
NMOS: Cell nfet_01v8 from sky130_fd_pr_main, set W and L to 1u.



2. ADE L Settings

Design Variables: Set i_{dc} at 1u and v_{dc} at 1.8

Analyses: Sweep V_{dc} from 0 to 1.8

Sweep Variable

☐ Temperature

☒ Design Variable Variable Name:

☐ Component Parameter

☐ Model Parameter

Sweep Range

☒ Start-Stop Start: Stop:

☐ Center-Span

Sweep Type

☒ Linear ☐ Step Size

☐ Number of Steps

Add Specific Points ☐

Add Points By File ☐

Add the below expressions as output, change the NMOS instance name in the expression with the name of current mirror output NMOS in your own schematic (can be viewed with Q):

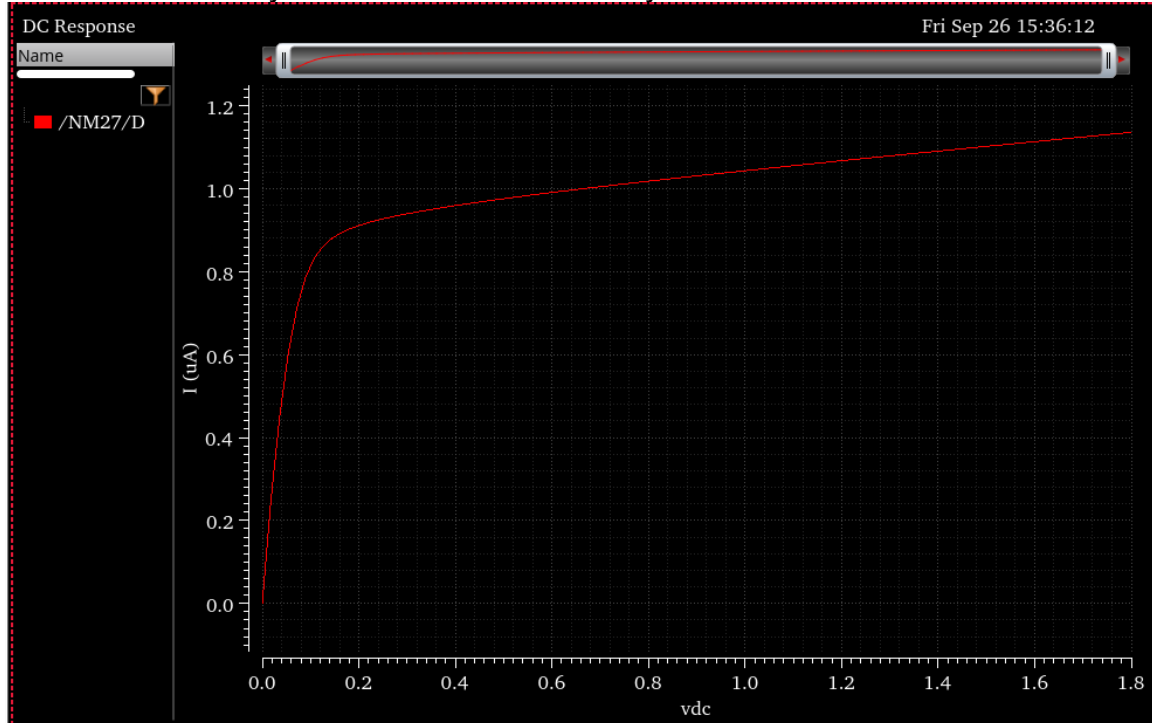
$ro_normal: (1 / \text{value}(\text{deriv}(\text{getData}("/\text{NM27/D}" ?\text{result 'dc'}) 1.6)))$

$OP_normal: OP("/\text{NM27}" \text{"region"})$

Also add the drain currents of the current mirror.

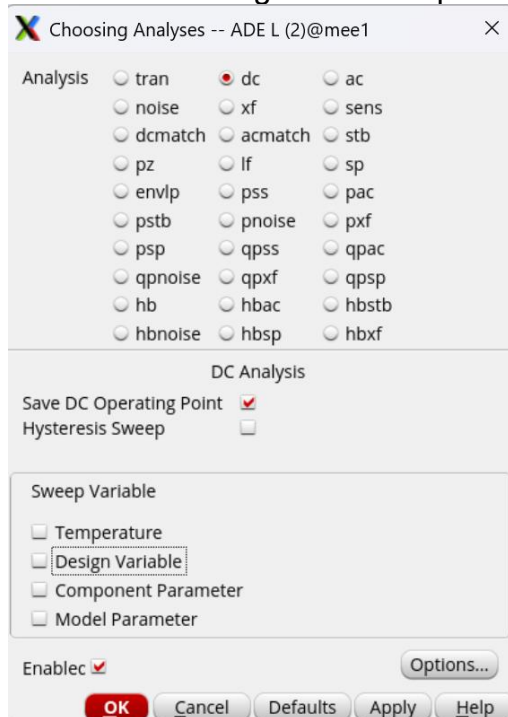
Outputs				
	Name/Signal/Expr	Value	Plot	Save
1	NM27/D		☒	☒
2	ro_normal	8.82635M	☒	☒
3	OP_normal	2	☒	☒

3. Run the simulation. You shall get the I_{out} vs V_{out} curve. Take a screenshot and save them on your server for further analysis.



Measuring minimum output voltage

1. To determine the minimum output voltage, we need to use parametric sweep and observe the operation regions of output NMOS.
Unselect the design variable option in dc analyses



- Only activate plot for OP_normal.

5 OP_normal	2	☒	☒
-------------	---	-------------------------------------	-------------------------------------

- In Tools -> Parametric Analyses, sweep vdc from 0 to 1 with 20 steps.

Parametric Analysis - spectre(1): test lab2 schematic @mee1

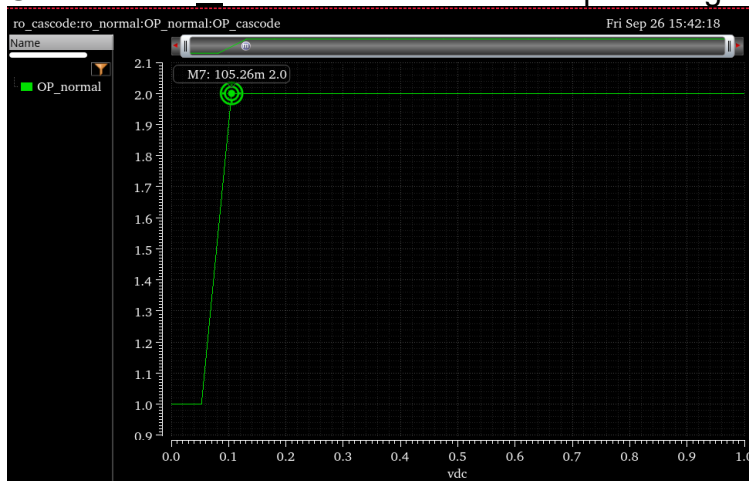
File Analysis Help

Ready

Run Mode: Sweeps & Ranges

Variable	Value	Sweep?	Range Type	From	To	Step Mode	Total Steps
vdc	1.8	☒	From/To	0	1.0	Linear	20

- Run the sweep, you will get the operation region vs Vout plot of the NMOS. In virtuoso, region 1 means triode region and region 2 means saturation region. Use shortcut **M** to mark the minimum output voltages.

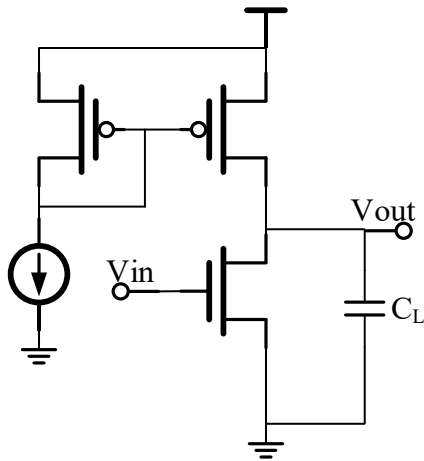


Tasks

- Show your simulation waveform to TAs and save your schematic and waveform for your lab report.
- Lab2 Q1: Adjust the size of the transistors to achieve output resistance > 20 Mohm. (5 marks)
- Lab2 Q2: How can you increase the output resistance to > 1 Gohm? (Hint: Use cascode). Find the rout and Vmin for two types of current mirrors. Compare simulation with theoretical calculations. (10 marks)

Lab 2.2 Common Source Amplifiers

This is the schematic diagram of the common source amplifier we are about to simulate:



The gain of a common-source amplifier is:

$$A_v = -g_m(r_o || R_D)$$

(Unit Gain Bandwidth) UGBW or Gain-Bandwidth Product, GBP :

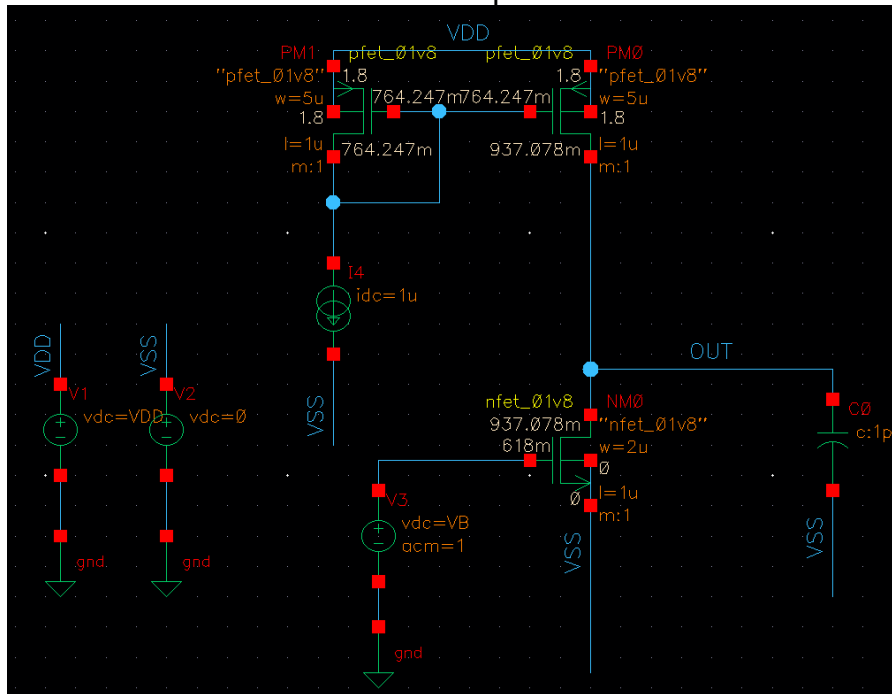
$$GBP = (g_m R_{drain}) \times \left(\frac{1}{2\pi R_{drain} C_{total}} \right) = \frac{g_m}{2\pi C_{total}}$$

In this lab we will:

1. Built CS amplifier testbench schematic.
2. Simulate and see the dc operation point of CS.
3. Simulate and draw the AC Gain plot of CS.

DC Simulation

1. First we need to create the CS amplifier schematic below:



pfet and nfet: use indicated size

capacitor: use 1p

Input voltage V3:

Property	Value	Display
Library Name	analogLib	off
Cell Name	vdc	off
View Name	symbol	off
Instance Name	V3	off

User Property	Master Value	Local Value	Display
Ignore	TRUE		off

CDF Parameter	Value	Display
Noise file name		off
Number of noise/freq pairs	0	off
DC voltage	VB V	off
AC magnitude	1 V	off
AC phase		off
XF magnitude		off
PAC magnitude		off
PAC phase		off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off

OK Cancel Apply Defaults Previous Next Help

Bias current I4:

Apply To: **only current** **Instance**

Show: ☐ system ☒ user ☒ CDF

Property Value Display

Property	Value	Display
Library Name	analogLib	off
Cell Name	Idc	off
View Name	symbol	off
Instance Name	I4	off

User Property Master Value Local Value Display

User Property	Master Value	Local Value	Display
Ivsignore	TRUE		off

CDF Parameter Value Display

CDF Parameter	Value	Display
Noise file name		off
Number of noise/freq pairs	0	off
DC current	1u A	off
AC magnitude		off
AC phase		off
Multiplier		off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off
XF magnitude		off
PAC magnitude		off
PAC phase		off

OK Cancel Apply Defaults Previous Next Help

2. ADE L Settings

Design Variables: Set VDD at 1.8 and VB at an initial value.

Name	Value
1 VB	600m
2 VDD	1.8

Analyses: Add a DC simulation sweeping VB from 0.3V to 0.7V.

Enable Save DC Operating Point.

Analysis

- ☒ tran ☒ dc ☐ ac
- ☐ noise ☐ xf ☐ sens
- ☐ dcmatch ☐ acmatch ☐ stb
- ☐ pz ☐ lf ☐ sp
- ☐ envlp ☐ pss ☐ pac
- ☐ pstb ☐ pnoise ☐ pxf
- ☐ psp ☐ qpss ☐ qpac
- ☐ qpnoise ☐ qpxf ☐ qpasp
- ☐ hb ☐ hbac ☐ hbstb
- ☐ hbnoise ☐ hbasp ☐ hbxf

DC Analysis

Save DC Operating Point ☒

Hysteresis Sweep ☐

Sweep Variable

☐ Temperature ☒ Design Variable Variable Name: **VB**

☐ Component Parameter ☐ Model Parameter

Sweep Range

☒ Start-Stop Start: **300m** Stop: **700m**

☐ Center-Span

Sweep Type

Automatic

Add Specific Points ☐

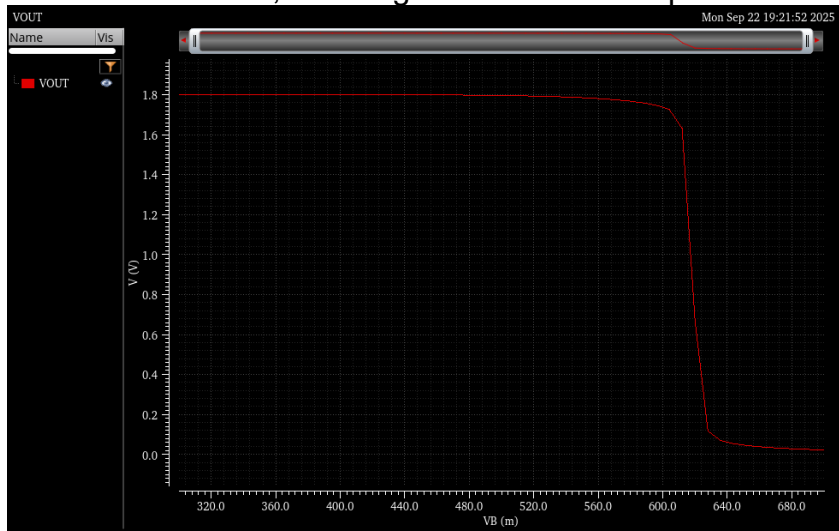
Add Points By File ☐

Enable ☒ Options...

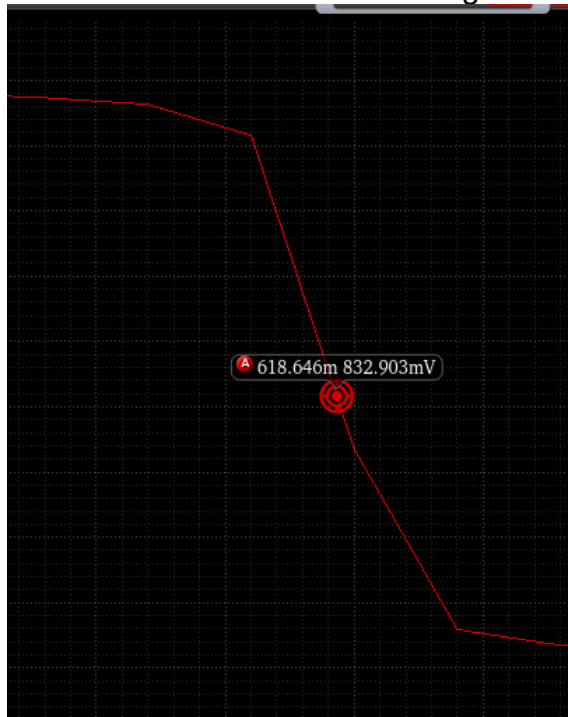
OK Cancel Defaults Apply Help

Outputs: Select OUT as the output in DC simulation

3. Run the simulation, we will get the OUT vs VB plot:



From the curve we can locate a good DC operation point.

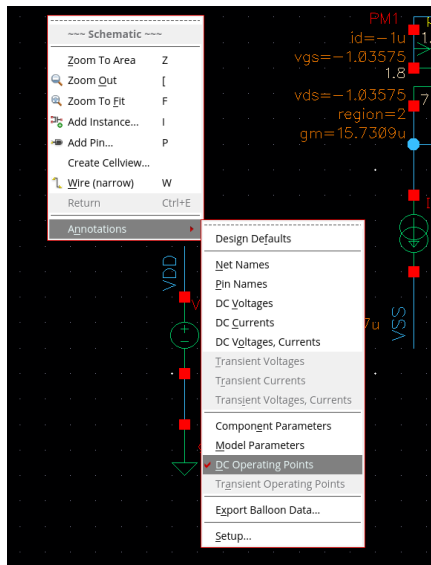


Update in ADE L and simulate again.

Design Variables	
Name	Value
1 VB	618m
2 VDD	1.8

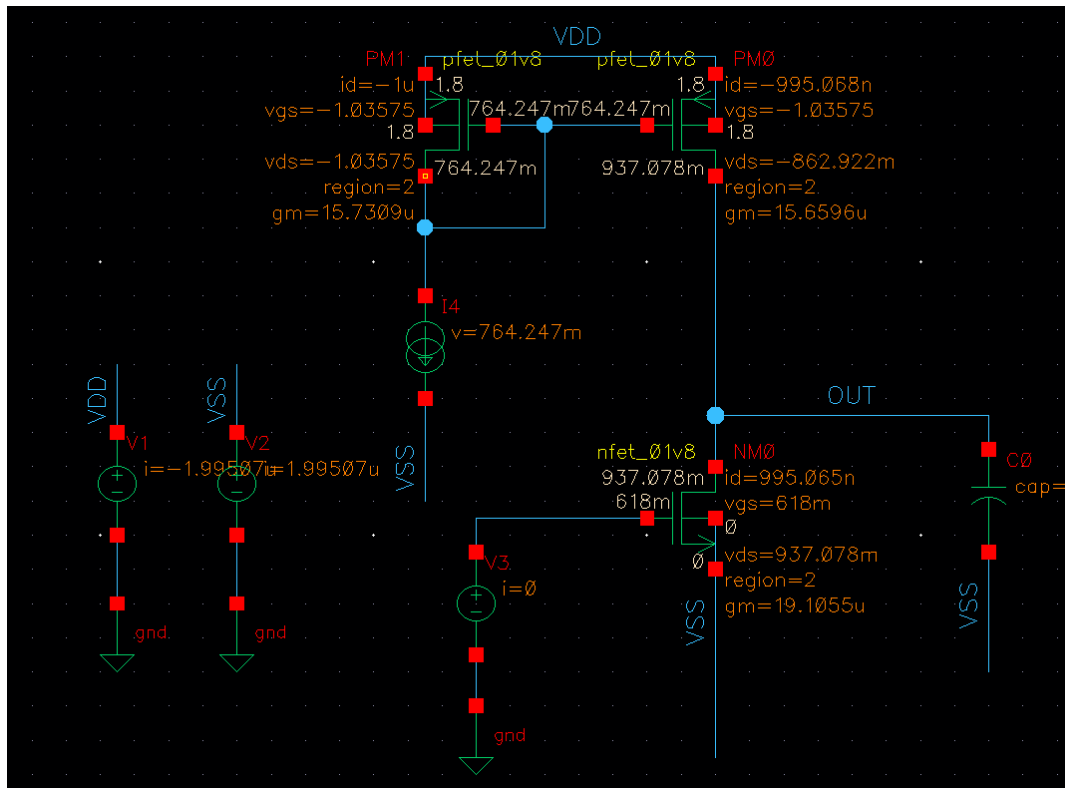
4. Check the DC operation Points

After we have run a DC simulation, we can observe its DC operation point on the schematic by right click -> Annotations -> DC Operating Points:

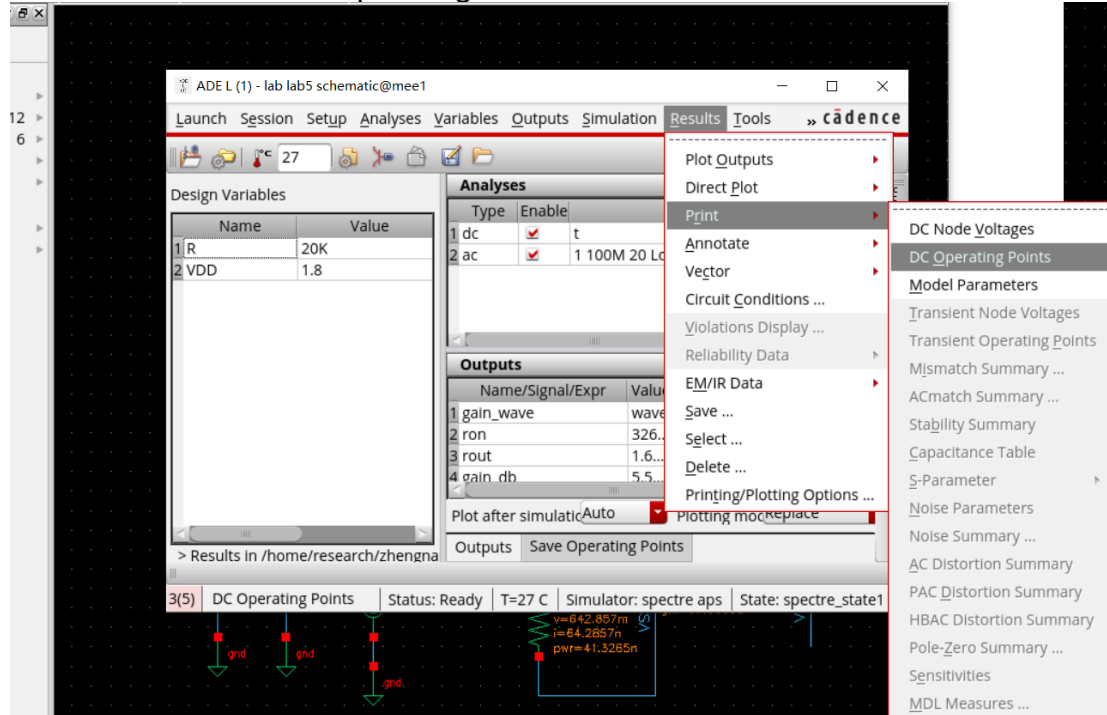


You will find the information of I, V, ID, VGS, VDS, region shown around the device. VGS stand for the voltage between G and S. VDS stand for the voltage between G and S.

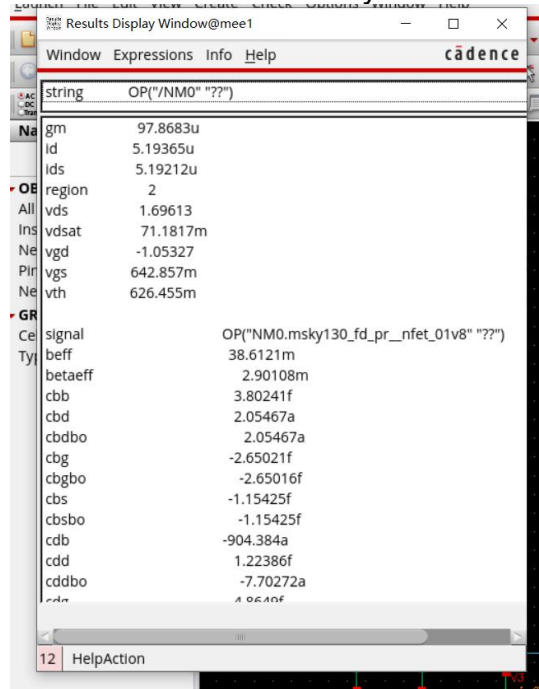
Region stand for the working region of MOSFET, 0 is the cut-off region, 1 is the linear region, 2 is the saturation region, and 3 is the subthreshold region.



If you want to observe the DC parameters of a single transistor, you can click Results -> Print -> DC Operating Points in ADE L.



Then click on the device you want to check on the schematic:



You can check the datasheet to figure out the meaning of parameter. MOSFET models are becoming increasingly complex in the deep submicron era. A typical MOSFET requires numerous parameters to define its operating state. We only need to focus on the most critical parameters.

AC Simulation

- Next, we will run AC simulation to simulate the AC transfer characteristics of the CS amplifier. We will use the same schematic as DC but a different ADE L settings.

Analyses: Add a AC simulation from 1Hz to 100MHz.

Analysis

☐ tran ☐ dc ☒ ac

☐ noise ☐ xf ☐ sens

☐ dcmatch ☐ acmatch ☐ stb

☐ pz ☐ lf ☐ sp

☐ envlp ☐ pss ☐ pac

☐ pstb ☐ pnoise ☐ pxf

☐ psp ☐ qpss ☐ qpac

☐ qpnoise ☐ qpxf ☐ qpssp

☐ hb ☐ hbac ☐ hbstb

☐ hbnoise ☐ hbasp ☐ hbxf

AC Analysis

Sweep Variable

☒ Frequency

☐ Design Variable

☐ Temperature

☐ Component Parameter

☐ Model Parameter

☐ None

Sweep Range

☒ Start-Stop Start Stop

☐ Center-Span

Sweep Type

☒ Points Per Decade

☐ Number of Steps

Logarithmic ☒

Add Specific Points ☐

Add Points By File ☐

Specialized Analyses

None ☒

Enable ☒

Options...

OK Cancel Defaults Apply Help

Outputs: Add OUT from schematic.

gain_wave Expression: db(vfreq('ac "/OUT"))

ron Expression: OP("NM0.msky130_fd_pr__nfet_01v8" "ron")

rout Expression: OP("NM0.msky130_fd_pr__nfet_01v8" "rout")

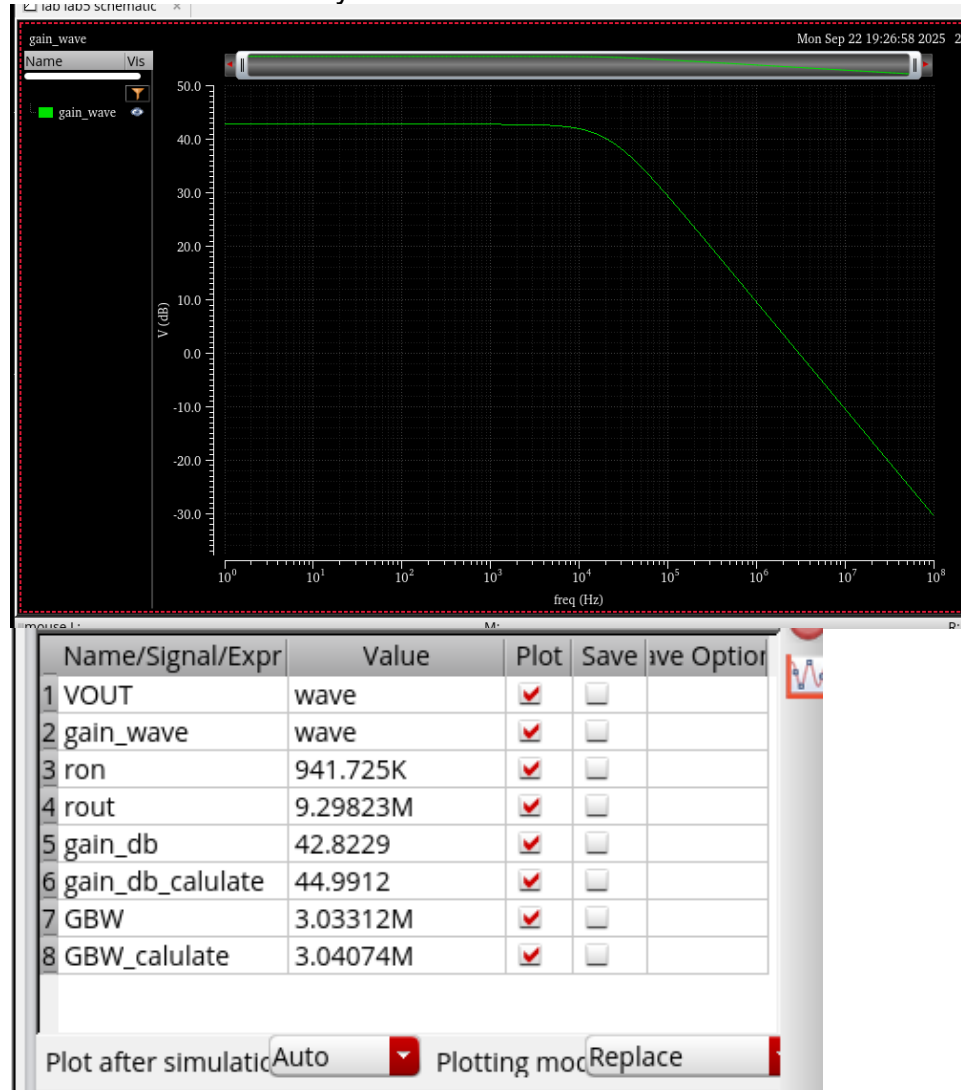
gain_db Expression: ymax(db(vfreq('ac "/OUT")))

gain_db_calulate Expression: dB20((rout * OP("/NM0" "gm")))

GBW Expression: cross(db(vfreq('ac "/OUT")) "0" 1 "falling" nil nil)

GBW_calulate Expression: (OP("/NM0" "gm") / (2 * pi * 1e-12))

Run the simulation. The gain waveform shows how gain varies with frequency. R_{on} represents the transconductance resistance. R_{out} represents the equivalent output resistance. $gain_db$ represents the actual maximum gain obtained through simulation. $gain_cal$ represents the gain calculated by looking up g_m and r_{out}/R_D , which are very close. GBW represents the unity-gain bandwidth obtained by simulation, and GBW_cal represents the unity-gain bandwidth calculated by G_m/CL .



- You may modify the MOSFET width-to-length ratio or current bias based on the below formula:

$$A_v = -g_m(r_o || R_D)$$

$$GBP = (g_m R_{drain}) \times \left(\frac{1}{2\pi R_{drain} C_{total}} \right) = \frac{g_m}{2\pi C_{total}}$$

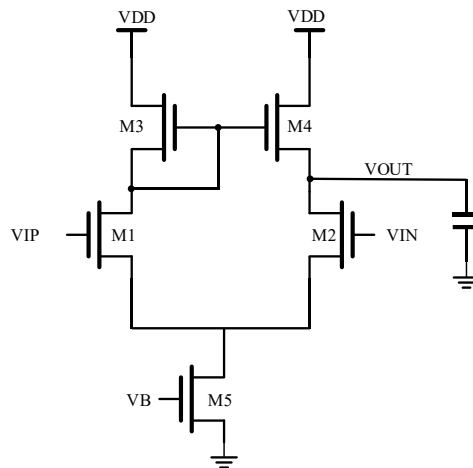
Tasks

- Show your simulation waveform to TAs and save your schematic and waveform for your lab report.
- Lab2 Q4: Now redesign the amplifier and try to increase (a) gain, (b) bandwidth and (c) gain bandwidth product by at least a factor of 2 while minimizing power dissipation. (these 3 separate experiments) (20 marks)
- Lab2 Q5: Explain the meaning of the calculator expressions used in this lab. (Optional)
- Lab2 Q6: Why the simulation gain and BW differ from calculations? (Optional)

Lab 3: Differential Amplifier Design

Lab 3.1 5T OTA Design

The schematic below shows the 5T OTA we will simulate in this lab. The input differential pair Q1 and Q2 converts input differential voltage into differential current. The current mirror Q3 and Q4 converts the differential current into single-ended voltage output. And the tail current source Q5 provides a constant bias current to set the DC operation point.



The unity gain bandwidth and voltage gain of 5T OTA is given by:

$$GBW = \frac{g_{m1}}{2\pi C_L}$$

$$A_{v0} = g_{m2} \cdot (r_{o2} \parallel r_{o4})$$

Design Specifications:

AC gain > 50 V/V

GBW > 10 MHz

ICMR better than 0.8V-1.3V

AC Simulation

Our simulation begins with an AC simulation to measure the AC transfer characteristics of the amplifier.

1. Draw the schematic below

V0: Cell vsin from analogLib, set AC magnitude to vac V.

V9: Cell vdc from analogLib, set DC voltage to vcm V.

V2 V3: VDD and VSS.

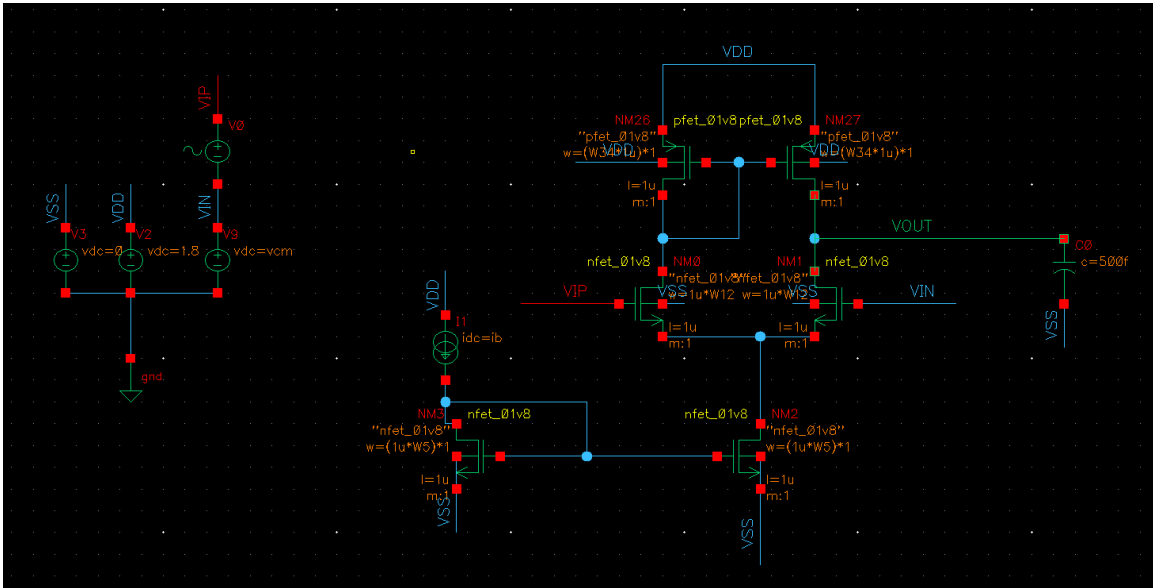
I1: Cell idc from analogLib, set dc current to ib A.

C0: Cell cap from analogLib, set capacitance to 500f F.

Top PMOS: pfet_01v8 from sky130_fd_pr_main with L = 1u, W = W34 * 1u

Middle NMOS: nfet_01v8 from sky130_fd_pr_main with L = 1u, W = W12 * 1u

Bottom NMOS: nfet_01v8 from sky130_fd_pr_main with L = 1u, W = W5 * 1u



2. ADE L Settings

Design Variables:

Name	Value
1 W34	10
2 W12	500m
3 W5	20
4 vac	10m
5 ib	5u
6 vcm	1

Analyses: Add an AC analyses from 1 Hz to 50 MHz

Choosing Analyses -- ADE L (1)@mee1

Analysis

☐ tran ☐ dc ☒ ac

☐ noise ☐ xf ☐ sens

☐ dcmatch ☐ acmatch ☐ stb

☐ pz ☐ lf ☐ sp

☐ envlp ☐ pss ☐ pac

☐ pstb ☐ pnoise ☐ pxf

☐ psp ☐ qpss ☐ qpac

☐ qpnoise ☐ qpxf ☐ qpsp

☐ hb ☐ hbac ☐ hbstb

☐ hbnoise ☐ hbasp ☐ hbxf

AC Analysis

Sweep Variable

☒ Frequency

☐ Design Variable

☐ Temperature

☐ Component Parameter

☐ Model Parameter

☐ None

Sweep Range

☒ Start-Stop Start Stop

☐ Center-Span

Sweep Type

Outputs:

GBW: $\text{cross}(\text{dB20}((\text{getData}("/\text{VOUT}" \text{ ?result 'ac' } / 0.01))) "0" 1 "either" \text{nil nil nil})$

GainAv: $\text{ymax}(\text{mag}((\text{getData}("/\text{VOUT}" \text{ ?result 'ac' } / 0.01)))$

GainDB: $\text{ymax}(\text{dB20}((\text{getData}("/\text{VOUT}" \text{ ?result 'ac' } / 0.01)))$

GainDB_wave: $\text{dB20}((\text{getData}("/\text{VOUT}" \text{ ?result 'ac' } / 0.01)))$

Phase_margin: $(180 + \text{value}(\text{phaseDegUnwrapped}(\text{vfreq}('ac "/\text{VOUT}')) \text{ GBW}))$

Phase_wave: $\text{phaseDegUnwrapped}(\text{VF}("/\text{VOUT}"))$

VDIFF: $(\text{getData}("/\text{VOUT}" \text{ ?result 'dc' }) - \text{getData}("/\text{VIP}" \text{ ?result 'dc'}))$

VICMR_max: $\text{cross}((\text{getData}("/\text{VOUT}" \text{ ?result 'dc' }) - \text{getData}("/\text{VIP}" \text{ ?result 'dc'})) -0.01 1 "either" \text{nil nil nil})$

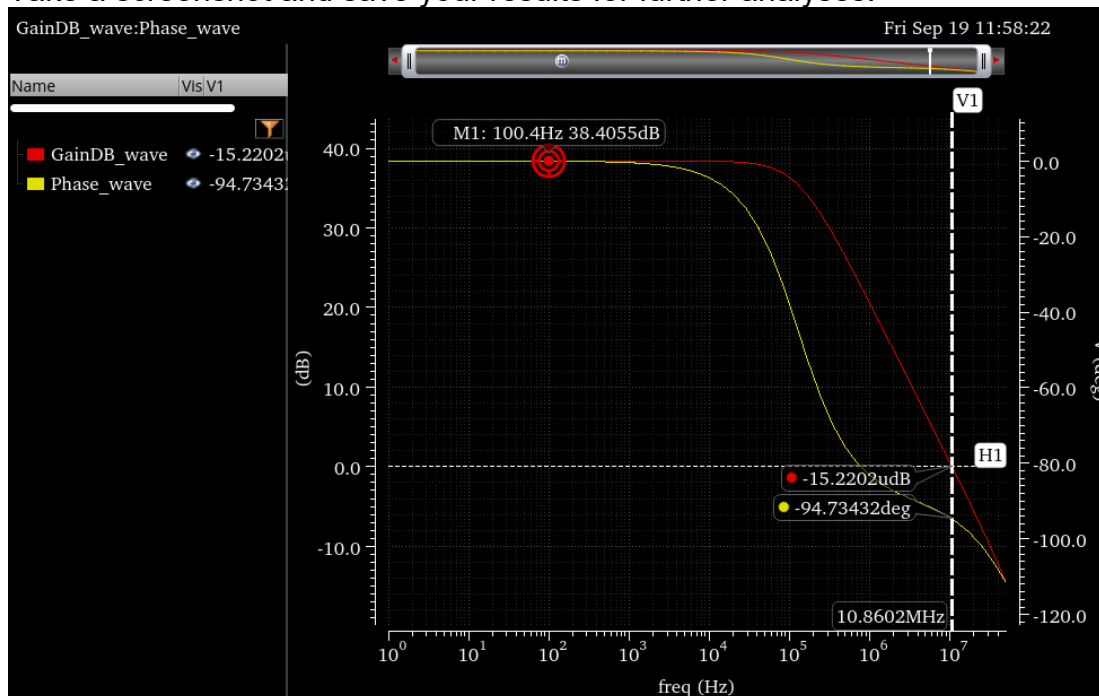
VICMR_min: $\text{cross}(\text{OS}("/\text{NM2}" \text{ "region"}) 1.5 1 "either" \text{nil nil nil})$

OP_DOWN: $\text{OS}("/\text{NM2}" \text{ "region"})$

VIP and VOUT: Add from schematic

Name/Signal/Expr	Value
1 GBW	
2 GainAv	
3 GainDB	
4 GainDB_wave	
5 Phase_margin	
6 Phase_wave	
7 VDIFF	
8 VICMR_max	1.36812
9 VICMR_min	738m
10 VIP	
11 VOUT	
12 OP_DOWN	wave

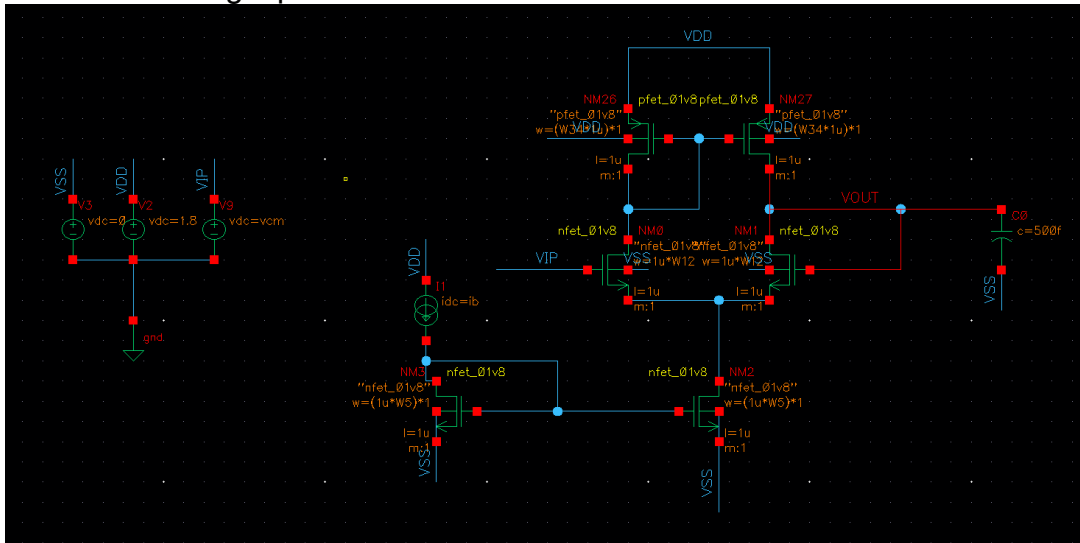
- Run the simulation and you will get the transfer characteristics of the 5T OTA. Take a screenshot and save your results for further analyses.



DC Simulation

Then we will configure the OTA as a voltage follower and sweep the common mode voltage input to determine its common-mode input range.

1. Modify your schematic as below. Short the inverting input and output. Connect the non-inverting input to the DC source.



2. ADE L configurations:

Analyses: Create a DC analyses sweeping vcm from 0 to 1.8V

DC Analysis

Save DC Operating Point ☒

Hysteresis Sweep ☐

Sweep Variable

☐ Temperature

☒ Design Variable Variable Name:

☐ Component Parameter

☐ Model Parameter

Sweep Range

☒ Start-Stop Start: Stop:

☐ Center-Span

Sweep Type

☒ Linear

☐ Step Size

☒ Number of Steps

Add Specific Points ☐

Add Points By File ☐

Outputs: Enable the DC outputs:

7	VDIFF	☒	☒	
8	VICMR_max	☒	☒	
9	VICMR_min	☒	☒	
10	VIP	☒	☒	allv
11	VOUT	☒	☒	allv

- Run the simulation, you will get the input common-mode range and the voltage follower I/O curve:

The left plot shows the operation region of the bottom transistor NM2. Here the value 1 means the triode region and the value 2 means the saturation region. From this plot we can observe the minimum V_{cm} needed to keep NM2 in saturation.

The right plot shows the DC input and output for a buffer connection. By observing the difference between them, we can find the maximum V_{cm} .

Take a screenshot and save your results for further analyses.

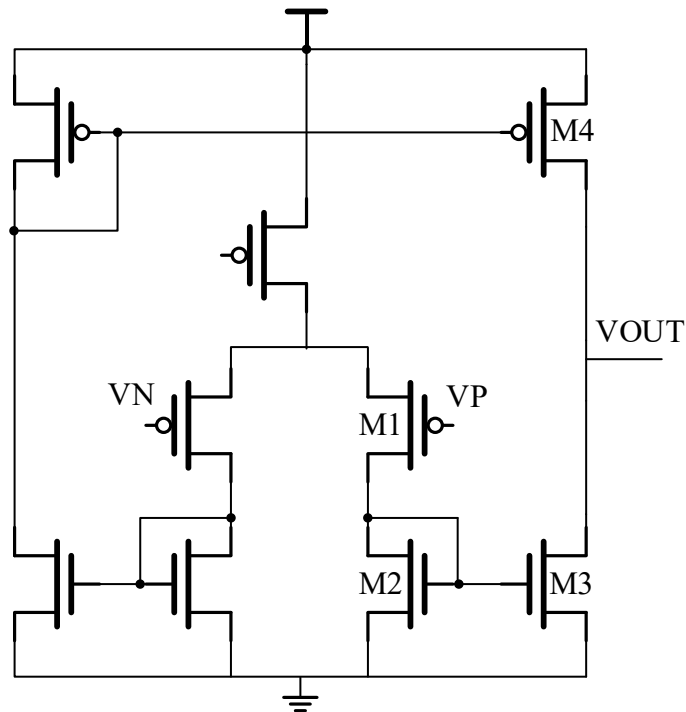


Tasks

- Show your simulation waveform to TAs and save your schematic and waveform for your lab report.
- Lab3 Q1: Adjust the size of transistors to satisfy the design requirements. (AC gain 5 marks, GBW 5 marks, ICMR 10 marks)
Please inform your simulation with a hand design. (10 marks)

Lab 3.2 9T/11T/13T OTA Design

This is the schematic diagram of the 9T differential amplifier we are about to build.



$$\left\{ \begin{array}{l} A_v = \frac{g_{m1}}{g_{m2}} g_{m3} (r_{on3} // r_{on4}) \\ GBP = \frac{g_{m1}}{CL} \end{array} \right.$$

In this lab we will

1. Build 9T/11T/13T differential amplifier and their testbench schematic.
2. Simulate and see the dc operation point of the amplifier.
3. Simulate and plot the AC gain of amplifier.

Requirements:

GBW>5MHz

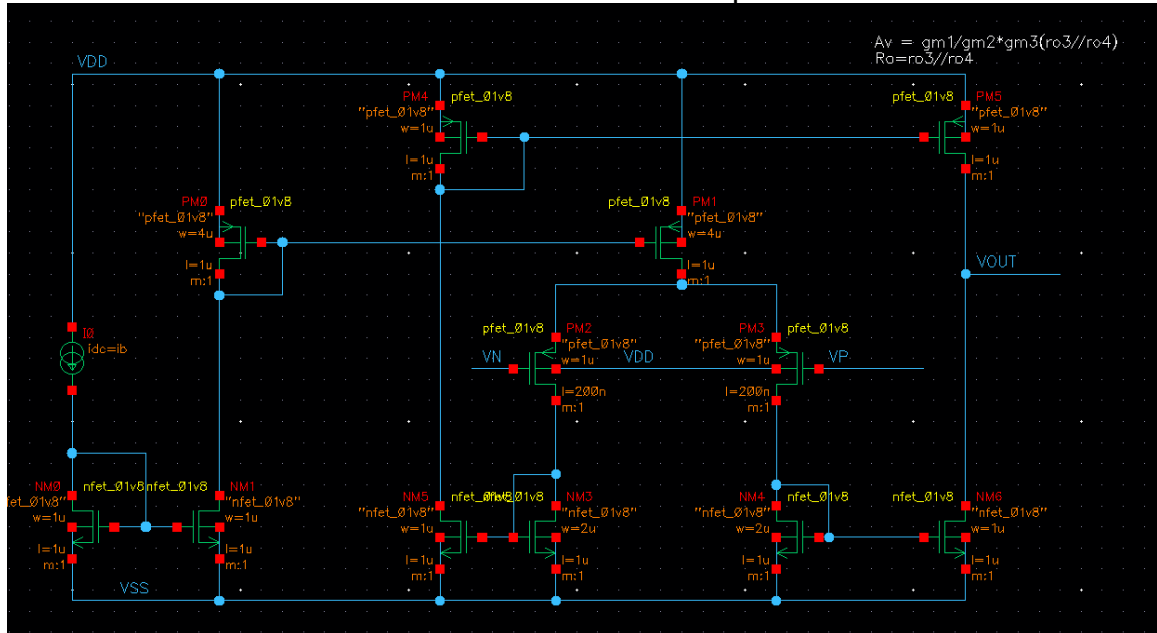
Gain>30dB

Phase_margin>60

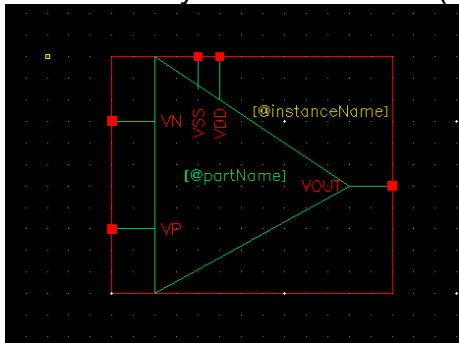
IMCR better than (300mV, 800mV)

DC Simulation

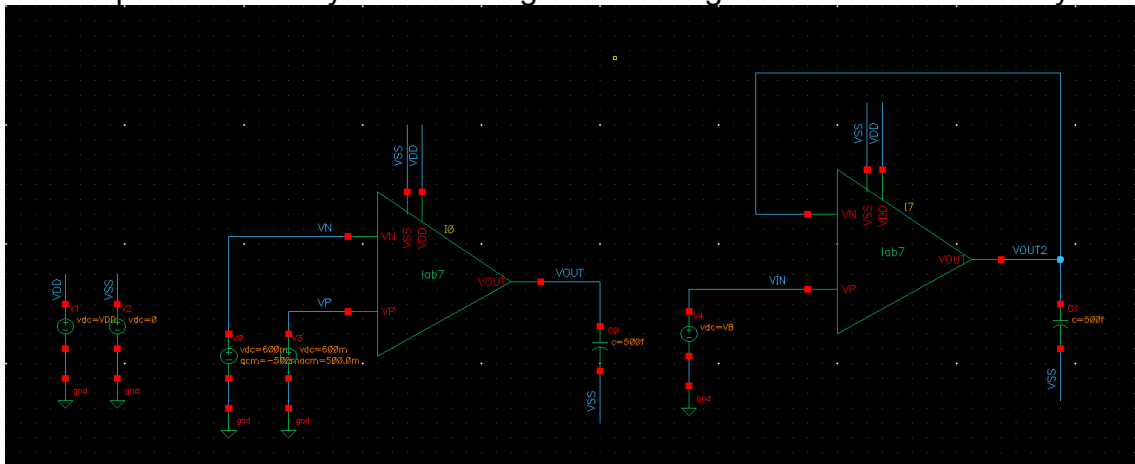
1. Build the schematic below for the 9T differential amplifier:



Create the symbol below for it (Recap Lab1.3):

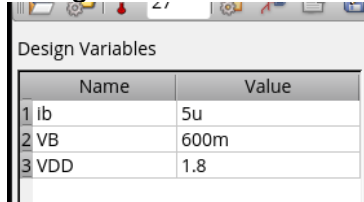


Create a new cell for testbench, draw the below testbench schematic. The left side amp is for AC analysis and the right side voltage follower is for DC analysis.



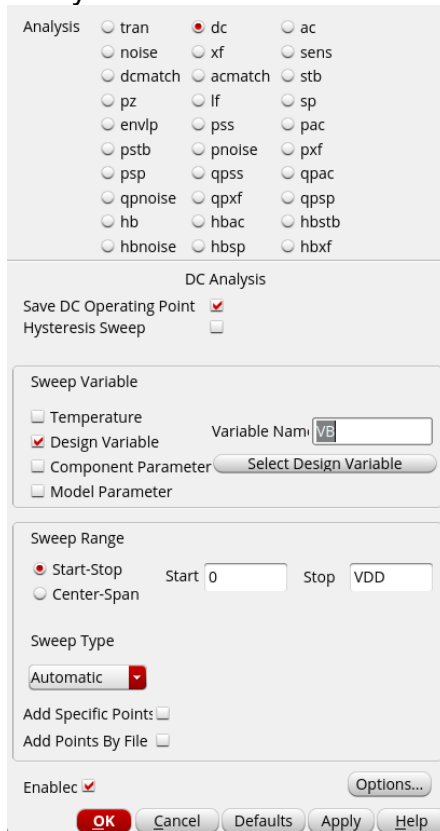
2. ADE L Settings

Design Variables:



	Name	Value
1	ib	5u
2	VB	600m
3	VDD	1.8

Analyses:



Analysis

☐ tran ☒ dc ☐ ac

☐ noise ☐ xf ☐ sens

☐ dcmatch ☐ acmatch ☐ stb

☐ pz ☐ lf ☐ sp

☐ envlp ☐ pss ☐ pac

☐ pstb ☐ pnoise ☐ pxf

☐ psp ☐ qpss ☐ qpac

☐ qpnoise ☐ qpxf ☐ qpasp

☐ hb ☐ hbac ☐ hbstb

☐ hbnoise ☐ hbasp ☐ hbxf

DC Analysis

Save DC Operating Point ☒

Hysteresis Sweep ☐

Sweep Variable

☐ Temperature

☒ Design Variable Variable Name:

☐ Component Parameter

☐ Model Parameter

Sweep Range

☒ Start-Stop Start: Stop:

☐ Center-Span

Sweep Type

Add Specific Points ☐

Add Points By File ☐

Enable ☒

Outputs:

First add VOUT2 and VIN from schematic.

OPM1: OS("/I7/PM1" "region")

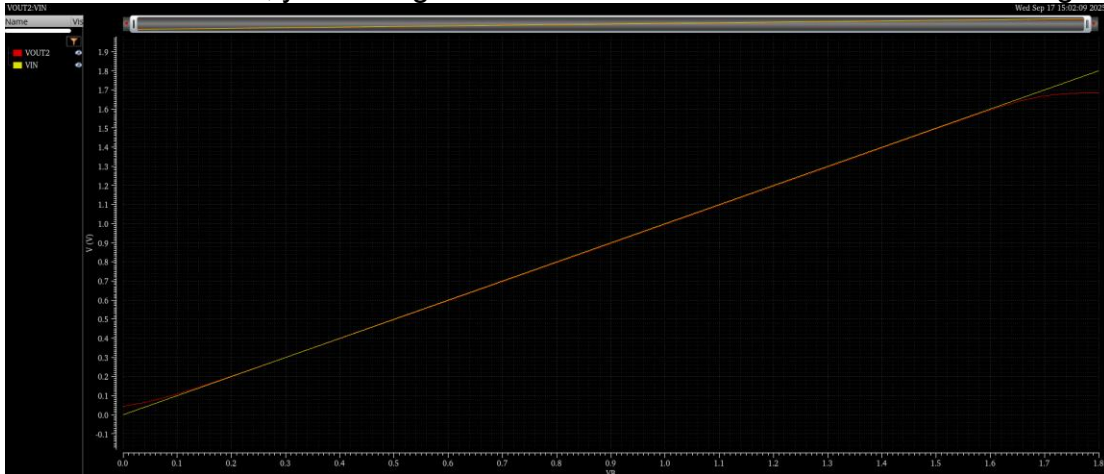
ONM6: OS("/I7/NM6" "region")

ICMR_H: cross(OS("/I7/PM1" "region") 1.1 1 "falling" nil nil nil)

ICMR_L: cross(OS("/I7/NM6" "region") 1.1 1 "rising" nil nil nil)

Outputs				
Name/Signal/Expr	Value	Plot	Save	Save Options
1 gain_wave	wave	☒	☐	
2 phase_wave	wave	☒	☐	
3 GBW	2.35906M	☒	☐	
4 gain_dB	37.634	☒	☐	
5 phasemargin	89.4848	☒	☐	
6 ICMR_H	716.4m	☒	☒	
7 ICMR_L	75.6m	☒	☒	

3. Run the simulation, you shall get the VIN vs VOUT2 curve and the ICMR ranges.



4. When adjusting the DC operation points, we should make sure that the MOSFETS operates in saturation region (region 2). Recap Lab2.2 to view the DC operation points in Cadence.

Hint: you can use shortcut E to descend into the amplifier schematic and ctrl + E to ascend.

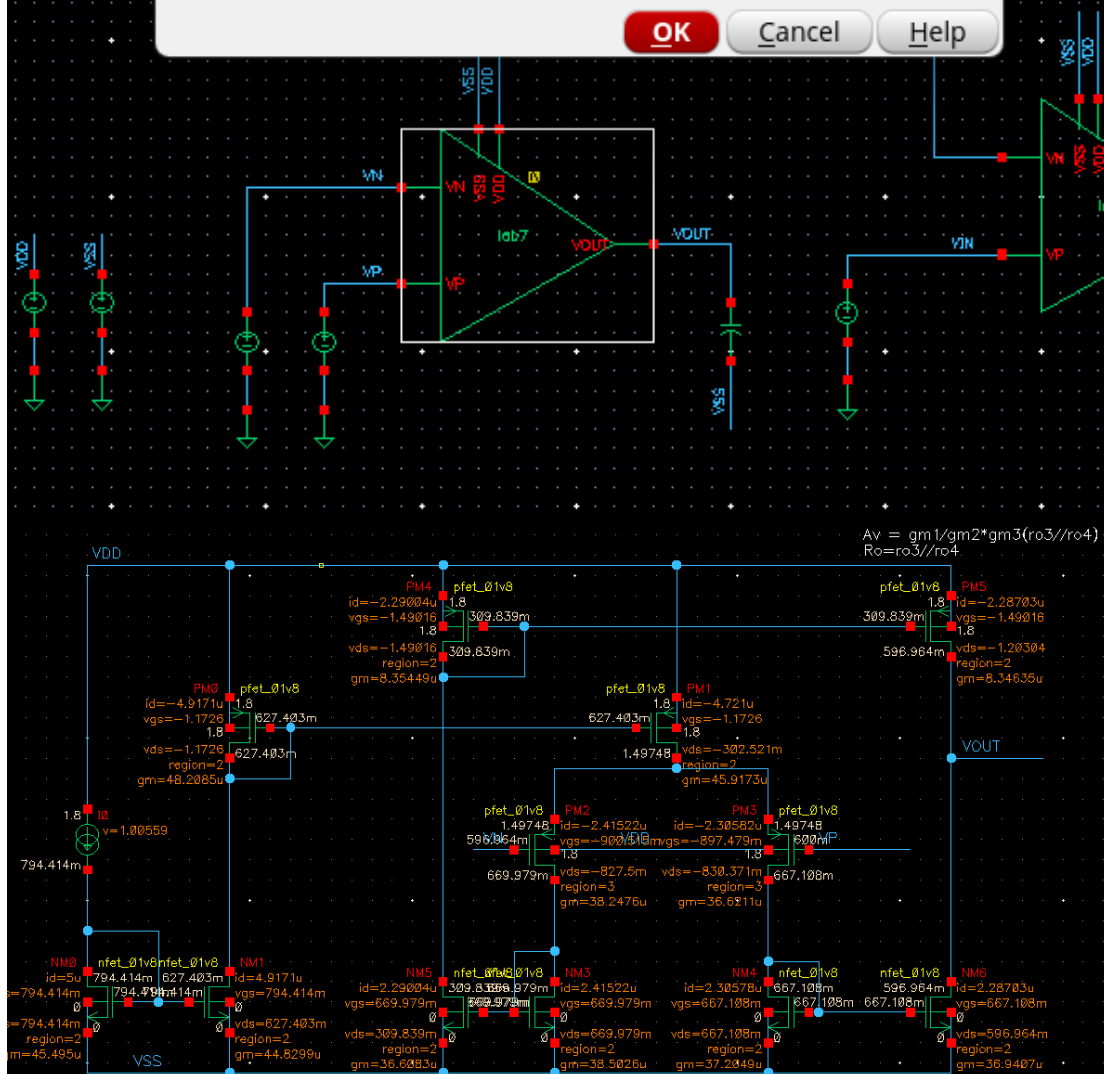
Descend@mee1
×

View
schematic

Open for
☐ edit
☒ read
☐ auto

Open in
☒ new tab
☐ current tab
☐ new window

OK
Cancel
Help



Results Display Window@mee1		
Window Expressions Info Help cadence		
	string	OP("/NM0" "?")
Na	gm	97.8683u
	ld	5.19365u
	lds	5.19212u
• OE	region	2
All	vds	1.69613
Ins	vdsat	71.1817m
Ne	vgd	-1.05327
Pir	vgs	642.857m
Ne	vth	626.455m
• GR		
Ce	signal	OP("/NM0.msky130_fd_pr__nfet_01v8" "?")
Ty	beff	38.6121m
	betaeff	2.90108m
	cbb	3.80241f
	cbd	2.05467a
	cbdbo	2.05467a
	cbg	-2.65021f
	cbgbo	-2.65016f
	cbs	-1.15425f
	cbsbo	-1.15425f
	cdb	-904.384a
	cdd	1.22386f
	cddbo	-7.70272a
	cdn	1.9640f
12 HelpAction		

AC Simulation

- Next, we will plot the AC characteristics of the amplifier. We will use the same schematic with different ADE L settings.

Analyses: AC analysis from 1Hz to 100MHz

Analysis: ☐ tran ☐ dc ☒ ac
☐ noise ☐ xf ☐ sens
☐ dcmatch ☐ acmatch ☐ stb
☐ pz ☐ lf ☐ sp
☐ envlp ☐ pss ☐ pac
☐ pstb ☐ pnoise ☐ pxf
☐ psp ☐ qpss ☐ qpac
☐ qpnoise ☐ qpxf ☐ qpssp
☐ hb ☐ hbac ☐ hbstb
☐ hbnoise ☐ hbasp ☐ hbx

AC Analysis

Sweep Variable
☒ Frequency
☐ Design Variable
☐ Temperature
☐ Component Parameter
☐ Model Parameter
☐ None

Sweep Range
☒ Start-Stop Start: 1 Stop: 100M
☐ Center-Span

Sweep Type
Logarithmic ☒ Points Per Decade: 20
☐ Number of Steps

Add Specific Points: ☐
Add Points By File: ☐

Specialized Analyses
None

Enabled: ☒ Options...

OK Cancel Defaults Apply Help

Outputs:

First add VOUT from the schematic.

```
gain_wave:db(vfreq('ac "/VOUT"))
```

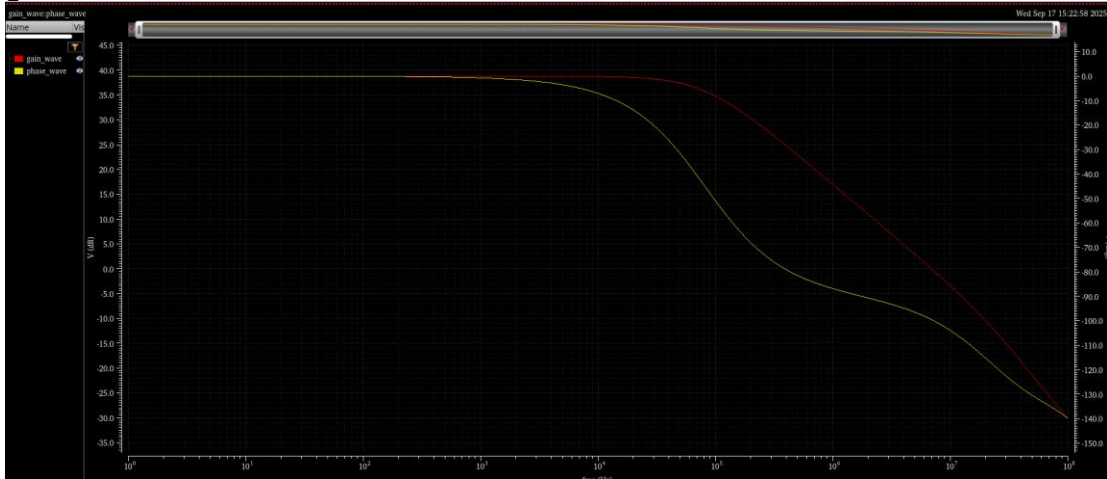
```
phase_wave: phaseDegUnwrapped(vfreq('ac "/VOUT"))
```

```
GBW: cross(db(vfreq('ac "/VOUT")) "0" 1 "either" nil nil nil)
```

```
phasemargin: (180 + value(phaseDegUnwrapped(vfreq('ac "/VOUT")) GBW))
```

	Name/Signal/Expr	Value	Plot
1	gain_wave	wave	☒
2	phase_wave	wave	☒
3	GBW	6.94142M	☒
4	gain_dB	38.7758	☒
5	phasemargin	80.4759	☒

The gain waveform shows how the gain changes with frequency. The phase waveform shows how the phase changes with frequency. We know that the difference between the phase at the frequency corresponding to zero gain and the 180° reverse phase is the amplifier phase margin. When designing an operational amplifier, it is necessary to ensure that the phase margin is at least greater than 60° .

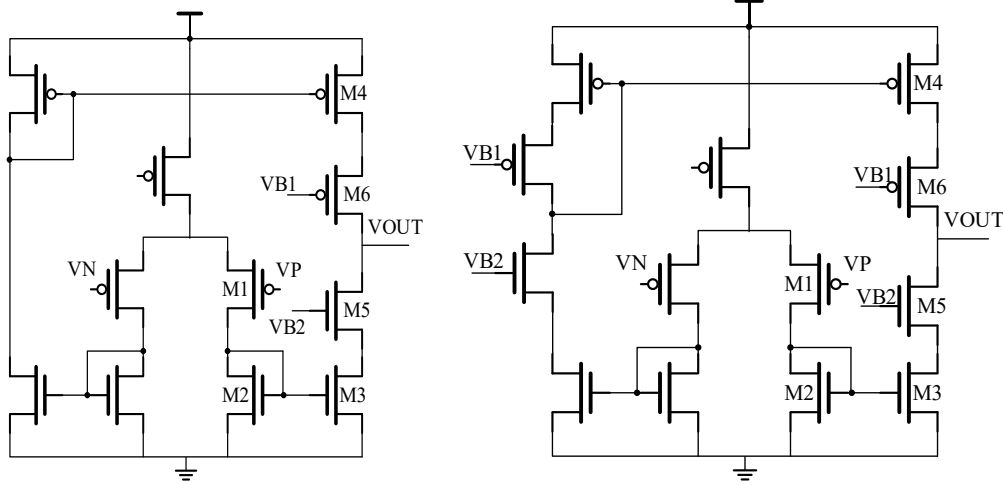


Tasks

- **Lab3 Q3: Adjust the size of transistors to satisfy the design requirements. Please inform your simulation with a hand design. (20 Marks)**
- **Lab3 Q4: Explain the meaning of the calculator expressions used in this lab. (Optional)**

Advanced Exercises

Try to build the schematic diagram of 11T and 13T and simulate related indicators.



Tips from TAs:

Although CMOS analog integrated circuits can now be manufactured with smaller transistor sizes, larger transistor sizes are typically used in analog integrated circuits to minimize channel modulation effects. Bias and load transistors typically use MOSFETs with $L=1\mu\text{m}$ and $W\geq 1\mu\text{m}$ to minimize channel modulation effects. Input transistors typically use $L=500\text{nm}$ or 200nm and $W\geq 2\mu\text{m}$ to maximize transconductance.

We encourage you to use current mirrors to generate bias voltages, but in this experiment, you can directly use the DC power supply VDC to generate the appropriate bias voltages for VB1, VB2.