

EE3220 System on Chip Design

Lecture Note 13

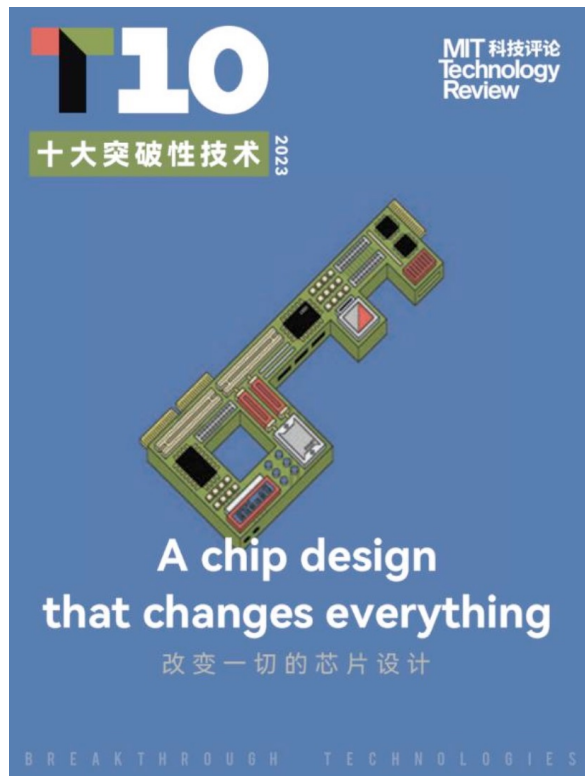
Intro to RISC-V

Review

- Lecture 1: Course Overview
- Lecture 2: Intro to Modern Microprocessor (CPU Architecture)
- Lecture 3: Embedded System Software (Software Architecture)
- Lecture 4: ARM Cortex-M4 (ARM Hardware)
- Lecture 5: From C to ARM Assembly (C Language, ARM Firmware)
- Lecture 6: Team Based Learning (USB Firmware)
- Lecture 7: AAPCS (ARM Firmware)
- Lecture 8: Exceptions & Interrupts (ARM Firmware)
- Lecture 9: Intro to HDL & FPGA Design (HDL Design)
- Lecture 10: FPGA based SoC (FPGA based SoC)
- Lecture 11: Integrating SoC Components (SoC Integration)
- Lecture 12: Team Based Learning (Wi-Fi SoC)
- **Lecture 13: Intro to RISC-V (RISC-V, Course Review)**

MIT Technology Review

10 Technology Breakthroughs in 2023



CREATING NEW POSSIBILITIES



Open RISC-V Architecture Standard
10s of Billion of RISC-V Cores Already Deployed

Overview

- WHAT is RISC-V?
- WHY RISC-V?
- WHO are Key Players?
- Roadmap in China
- Current Challenges

Overview

- **WHAT** is RISC-V?
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WHAT is RISC-V?

The
definition
of open
computing
is RISC-V



- RISC-V is the **FIFTH GENERATION RISC ISA** from UC Berkeley.
- RISC-V is an open, **ROYALTY-FREE**, extensible CPU architecture.
- Chip designers can quickly create new **CUSTOMIZED ARCHITECTURES** for their target applications.
- Customized architectures are supported by **WORLDWIDE RISC-V HW/SW ECOSYSTEM**.

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WHY RISC-V?

**OPEN
STANDARD**

**MODULAR
DESIGN**

**CUSTOMIZED
INSTRUCTIONS**

**AGILE
DESIGN FLOW**

Value Proposition: Open Standard

TECHNOLOGY

Arm to make its own prototype chips to boost post-IPO business

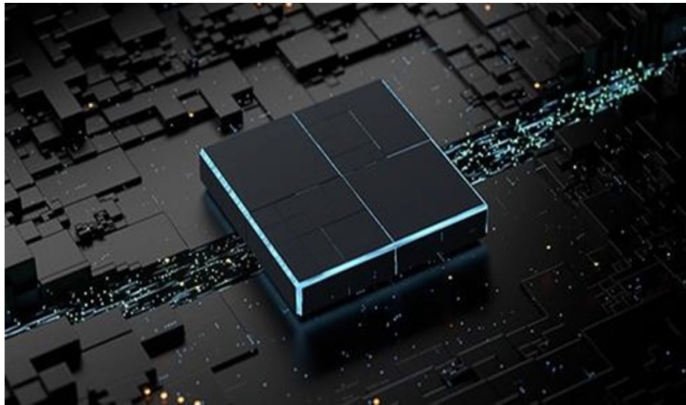


Photo Credit: Source: arm.com

Team TC | 24 Apr, 2023



- Architecture no longer controlled by ARM.
- No royalty payments.
- Do not need to compete with ARM's own chips using ARM's architecture.

Value Proposition: Custom Instructions

RISC-V may encompass both RISC and
CUSTOM SIMD/CISC instructions

RISC is efficient
for **GENERAL
PURPOSE
APPLICATIONS**

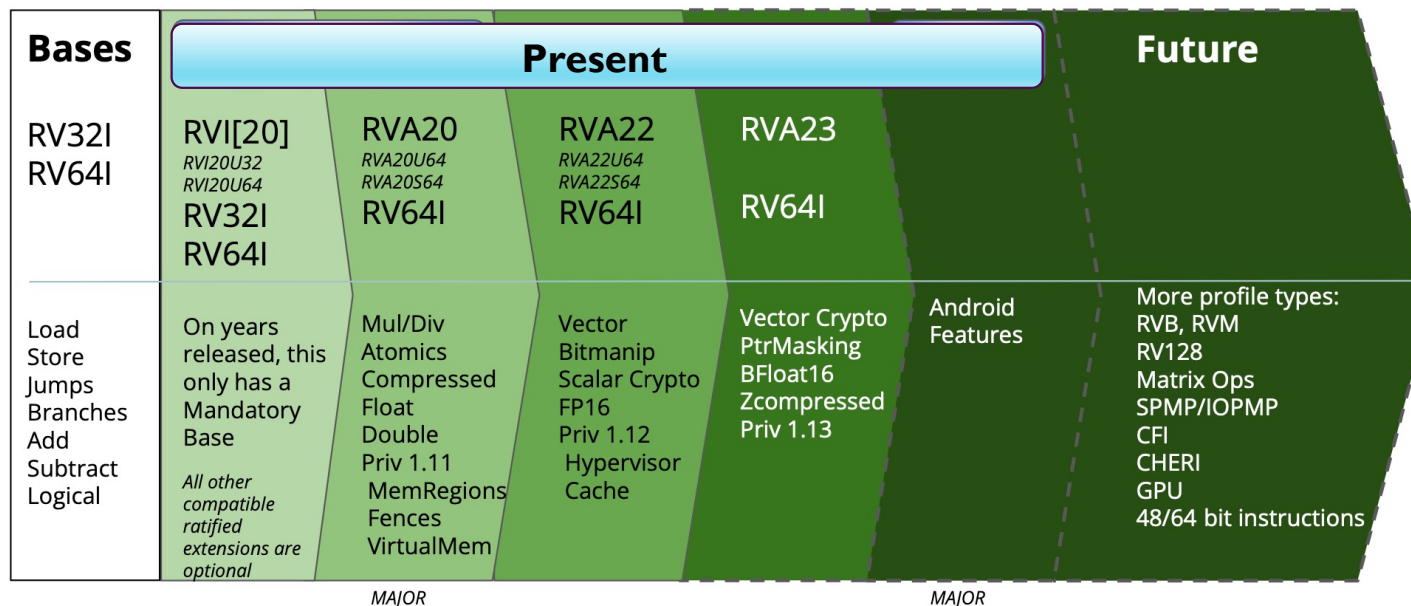
**BASIC
RISC
INSTRUCTIONS**

**CUSTOM
SIMD/CISC
INSTRUCTIONS**

SIMD/CISC is
efficient for
**DOMAIN SPECIFIC
APPLICATIONS**, like
DSP and Machine
Learning

Note: RISC-V instructions are mostly 32-bit instructions,
but RISC-V can also support 16-bit compressed
instructions , and 48-bit to 96-bit extended instructions

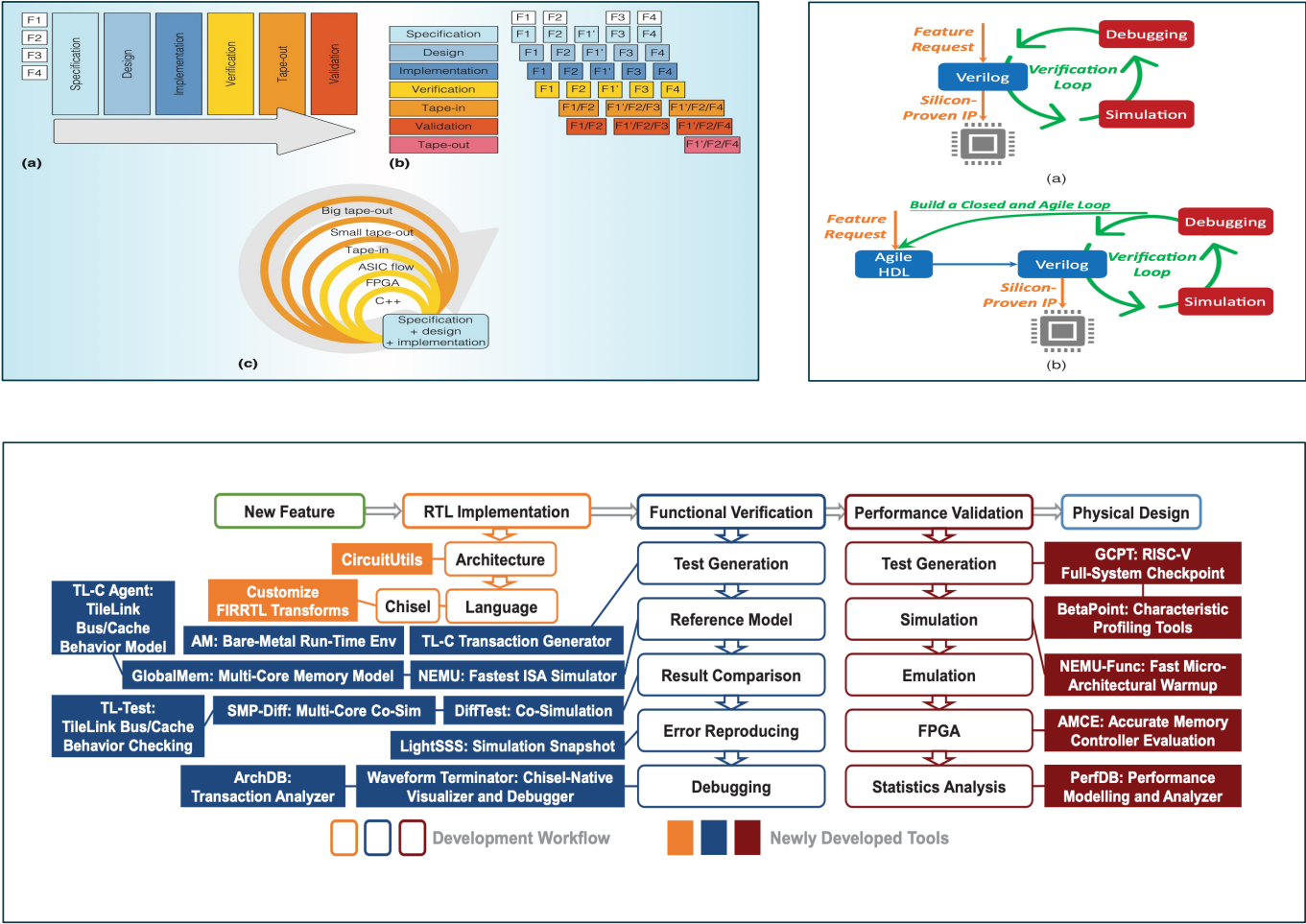
Value Proposition: Modular Design



- Only a subset of extensions are listed above and it is not an exhaustive list
- Some extensions may be optional or non-profile in one profile and be mandatory in another

Each **PROFILE**, which is tailored for each application **SCENARIO** (IoT or smartphone or server), can support many optional **EXTENSIONS** (such as floating-point or hypervisor/cache instructions).

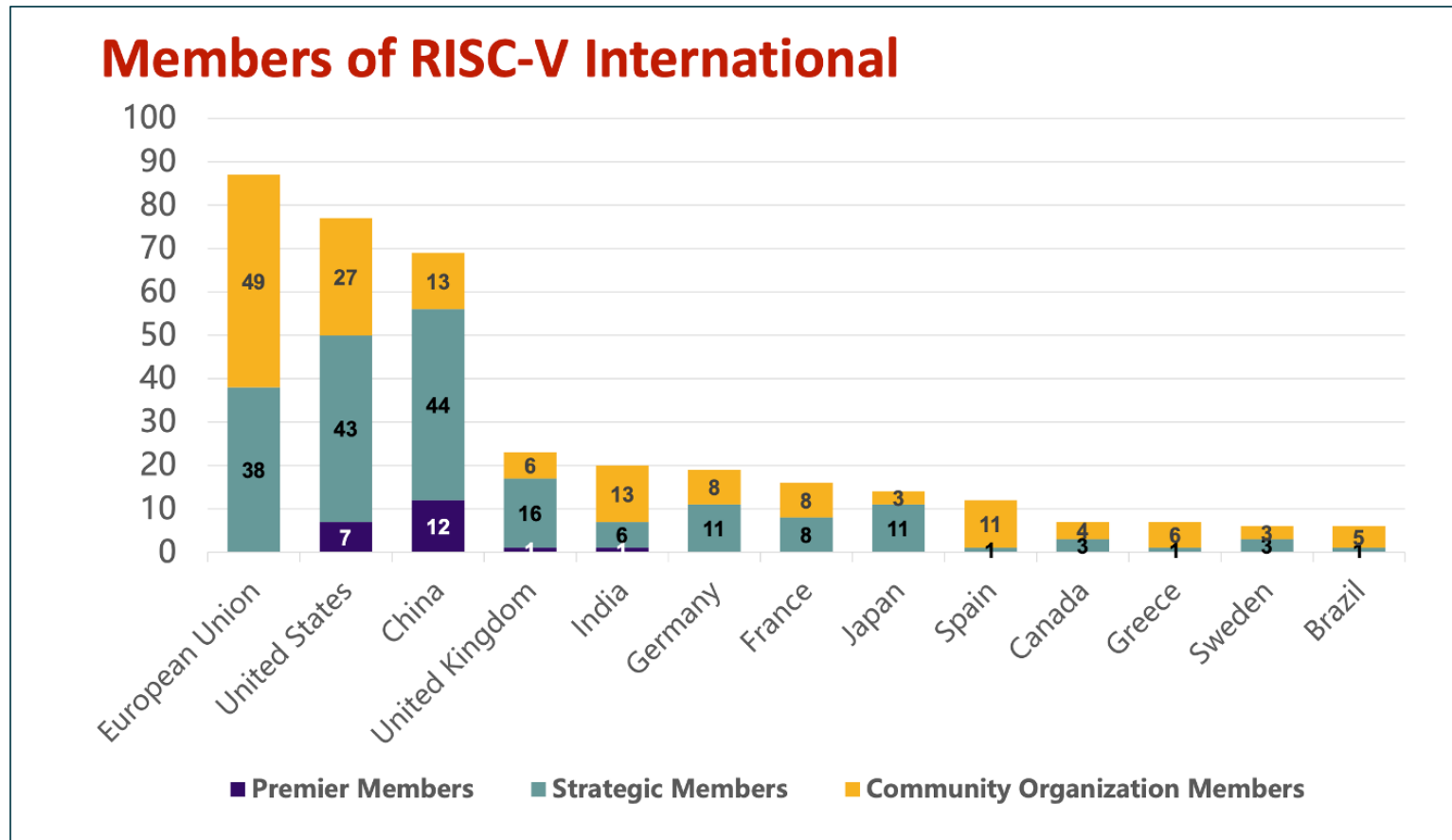
Value Proposition: Agile Design Flow



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Key Players: Geographical Distribution



Key Players: Applications in USA, Europe

AI / HPC SERVERS

EUROHPC JU allocates €270M to make HPC RISC-V chips.

INTEL creates \$1B fund to create RISC-V market.

AUTOMOTIVES

QUALCOMM, **NXP**, **INFINEON**, **NORDIC SEMICONDUCTOR** and **BOSCH** will form a new company to make automotive RISC-V chips.

LOW POWER IOT

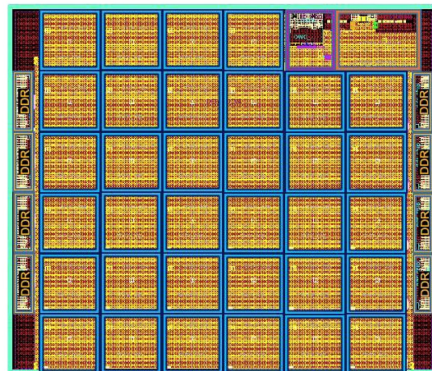
EUROPEAN PROCESSOR INITIATIVE to develop lower power RISC-V chips.

MICROCHIP won \$50M to develop high reliability RISC-V chips for space missions.

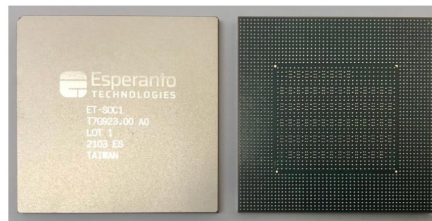
PHONES

GOOGLE announced in the 2022 RISC-V Summit that it will officially support RISC-V on Android.

Key Players: High Performance Computing (HPC)

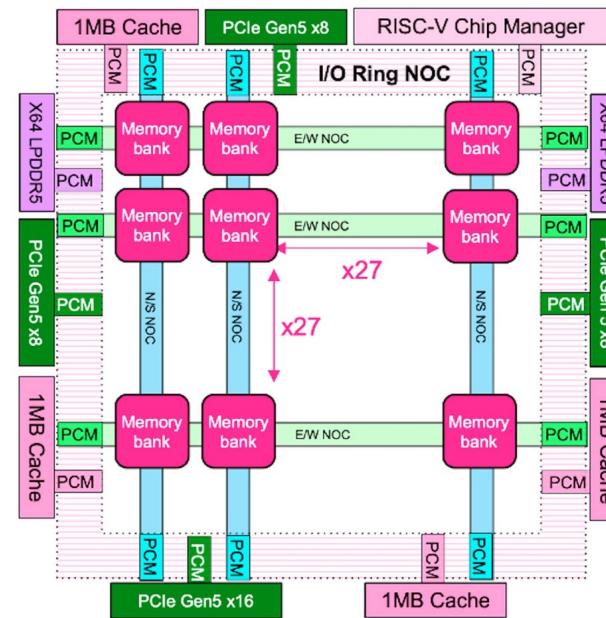


ET-SoC-1 Die Plot



ET-SoC-1 Package

Esperanto's Tensor Processor
1000+ RISC-V Cores
(Mountain View, CA)



Untether AI's SpeedAI240 Processor
1456 RISC-V Cores
(Toronto, ON)

IP Providers: USA, Europe

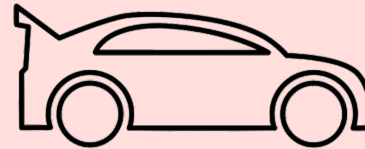
 SiFive	 codasip [®]	 ANDES TECHNOLOGY	 Ri vos
 Imagination	 XMOS	 VENTANA MICRO	 rydev
Akeana	 tenstorrent	 MIPS TECHNOLOGIES	CAST

Key Players: Applications in China

AI / HPC SERVERS



AUTOMOTIVES



IOT



PHONES



IP Providers: China

CAS



T-HEAD



ALLWINNERS



NUCLEI



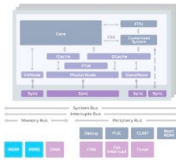
RIOS



THUNDERSOFT



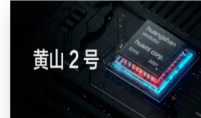
UC TECHIP



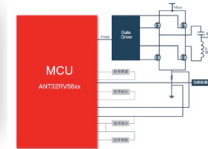
GIGADEVICE



ZEPP



CMSEMICON



STARFIVE



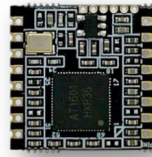
FISILINK



MCH



TIMESINTELLI



JEEJIO



CAMBRICON



XITC



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Roadmap in China

The China RISC-V Alliance (CRVA) founded in 2018 is driving Open-Source Chip Ecosystem (OSCE):

- Develop Silicon-Proven **OPEN-SOURCE RISC-V CORES**. (3-5 years)
- Build **OPEN-SOURCE SOC**s using **OPEN-SOURCE EDA TOOLS**. (5-7 years)
- Build **OPEN-SOURCE HARDWARE** automatically using **OPEN-SOURCE EDA TOOLS**. (10-15 years)



2030 “三步走” 规划

- **第一步：开源SoC**——用3-5年为社区提供经过流片验证的高质量RISC-V开源核、开源SoC设计
 - RISC-V处理器核IP、外围IP等
- **第二步：用开源工具链构建开源SoC**——用5-7年逐步构建一套基于开源EDA工具链、开源IP、开源工艺库的开源SoC芯片设计流程
 - 将商业版工具、IP逐渐替换为开源版
 - 实现本科生用全开源工具开发开源芯片，带着自己芯片毕业
- **第三步：用开源工具链自动化构建开源硬件**——用10-15年开发更智能、更自动化的开源工具，提高设计验证效率
 - 形成开源芯片生态，降低芯片开发门槛

Roadmap in China: Open-Source RISC-V Cores

- Chinese Academy of Sciences: Xiangshan RISC-V (香山)
 - HIGH-PERFORMANCE, OPEN-SOURCE RISC-V CPU Project
- Tools
 - Toolchains: GCC/LLVM
 - Simulator: Verilator, FireSim
 - OS: Linux
- Xiangshan v1 (28nm) 雁栖湖 (2021)
 - SPEC CPU2006: 7.01 at 1GHz
- Xiangshan v2 (24nm) 南湖 (2023)
 - SPEC CPU2006: 20 at 2GHz
- Xiangshan v3 (7nm) 昆明湖 (2025)
 - SPEC CPU2006: 45 at 3GHz

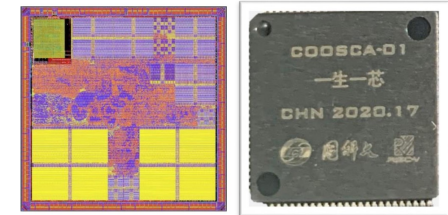
Roadmap in China: Open-Source Platform & EDA Tools

HPC Platform	PerfXLab
Operating System	Linux
IDE	
Compiler	TeraPines 兆松科技
Simulator	 T-HEAD
EDA Tools	OpenLane

Roadmap in China: One Student One Chip

- OSOC launched in 2019
 - Train **EACH UNDERGRADUATE** to design their **OWN CHIP**.

BATCH	START	# SCHOOLS	# ENROLLMENTS
1	AUG 2019	1	5
2	AUG 2020	5	11
3	JUL 2021	168	760
4	FEB 2022	328	1753
5	AUG 2022	335	1689



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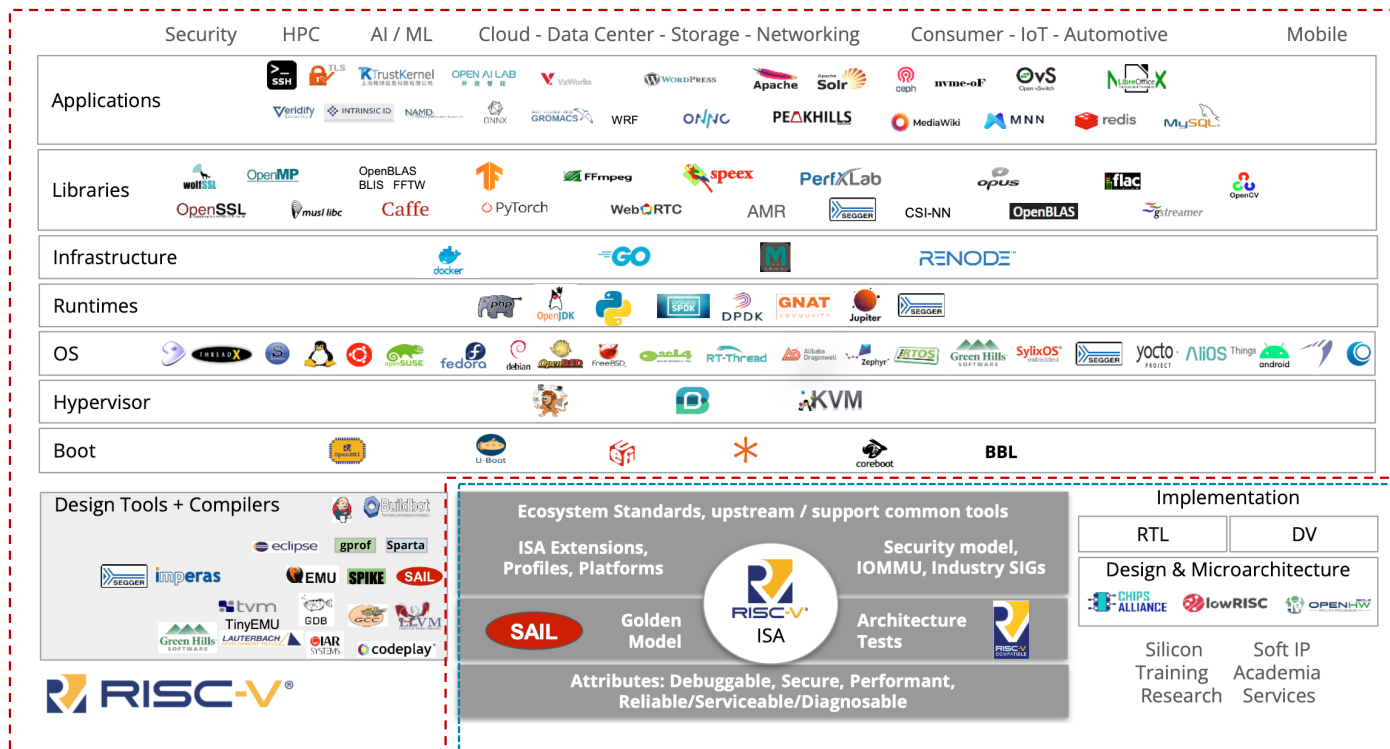
Current Challenges

RISC-V International identifies
SOFTWARE ECOSYSTEM as **#1 PRIORITY**.

RISC-V software ecosystem currently
lags behind ARM's or x86's, as it is
harder to support such **FLEXIBLE &
FRAGMENTED DESIGN**.

Current Challenges

Software ecosystem is more complex



Hardware ecosystem is more straightforward