

EE3220: Test 2-Answer (Total of 55 marks)

Question 1.(i)

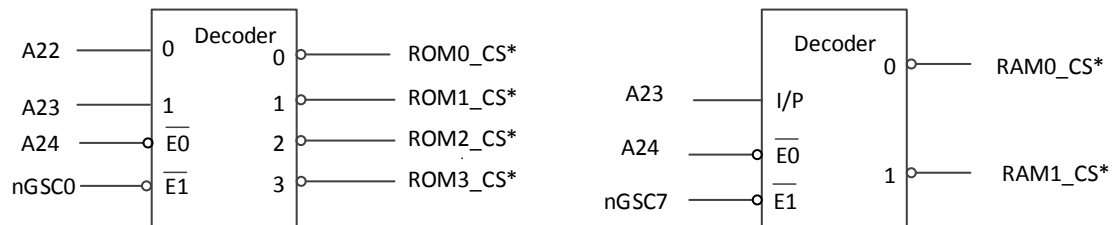
No. of ROM chips required: $16\text{M}/2\text{M} = 8$

No. of RAM chips required: $16\text{M}/4\text{M} = 4$

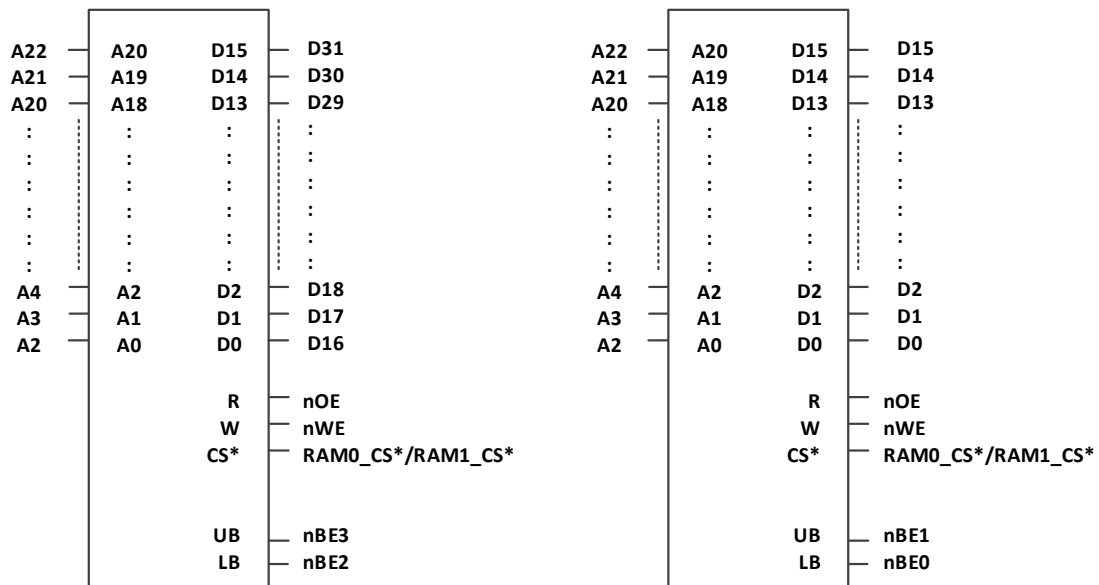
(ii)

		Address lines																
Device	nGCS	24	23	22	21	20	19	18	17	16	...	07	06	05	04	03	02	01
ROM0	0(000)	0	0	0	X	X	X	X	X	X	...	X	X	X	X	X	X	X
ROM1	0(000)	0	0	1	X	X	X	X	X	X	...	X	X	X	X	X	X	X
ROM2	0(000)	0	1	0	X	X	X	X	X	X	...	X	X	X	X	X	X	X
ROM3	0(000)	0	1	1	X	X	X	X	X	X	...	X	X	X	X	X	X	X
RAM0_0	7(111)	0	0	X	X	X	X	X	X	X	...	X	X	X	X	X	X	-
RAM0_1	7(111)	0	1	X	X	X	X	X	X	X	...	X	X	X	X	X	X	-

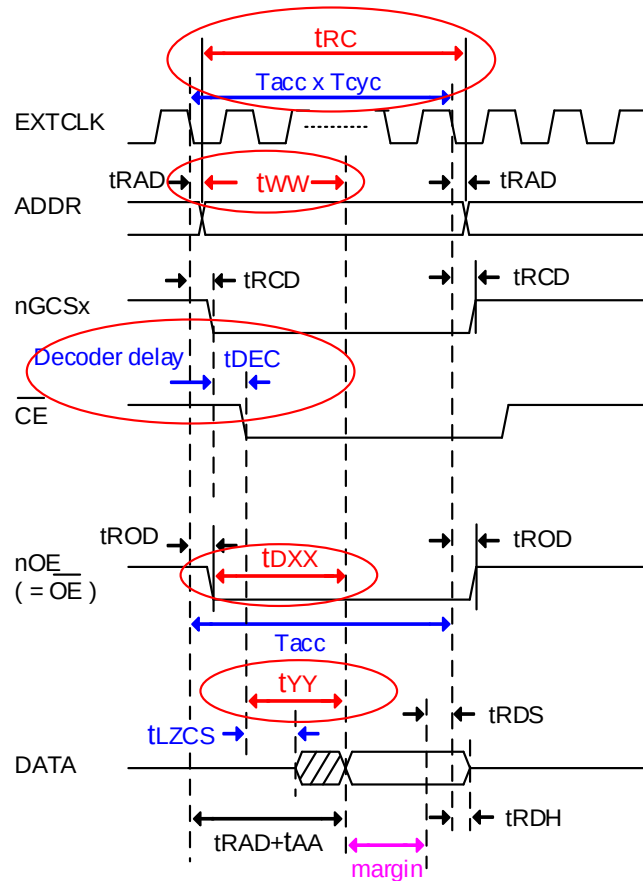
(iii)



(iv)



Question 2



READ CYCLE:

$$t_{RAD} + t_{WW} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$\text{i.e., } T_{acc} \geq (t_{RAD} + t_{WW} + t_{RDS}) / t_{cyc}$$

CPU running at 50 MHz ($t_{cyc} = 20$ ns):

$$T_{acc_{min}} \geq (12 + 150 + 1) / 20 \geq 8.15 = 9$$

Condition checking (i):

$$(i) \ t_{RCD} + t_{DEC} + t_{YY} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$11 + 50 + 150 + 1 = 212 \Rightarrow 212 / 20 = 10.6$$

$$\text{i.e., } T_{acc} = 11$$

Condition checking (ii):

$$(ii) \ t_{ROD} + t_{DXX} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$11 + 70 + 1 = 82 \Rightarrow 82 / 20 = 4.1$$

Final $T_{acc} = 11$

Question 3

$$t_{cyc} = 1/50\text{MHz} = 20\text{ns}$$

$$t_{RCD} = 35\text{ns} \Rightarrow 35/20 = 1.75 = 2 \Rightarrow 00$$

$$\text{SCAN (9-bit: CA0-CA8)} = 01 \Rightarrow 01$$

$$\text{Bankcon6(7)} = 1\ 1xxx\ xxxx\ xxxx\ 0001$$

$$T_{rp} = 30\text{ ns} \Rightarrow 30/20 = 1.5 \Rightarrow 00$$

$$T_{rc} = 80\text{ns} \Rightarrow 80/20 = 4 \Rightarrow 00$$

$$\text{Refresh: cycle} = 64\text{ms}/4096 = 15.625\text{ us}$$

$$\text{Resresh count} = 2^{11} + 1 - 50 \times 15.625 = 1267.75 \Rightarrow 1268 = 100\ 1111\ 0100$$

$$\text{REFRESH} = 1000\ 0000\ 0000\ 0100\ 1111\ 0100 = 80004F4$$

