

Question 1

Sketch the cross-section of an enhancement-type n-channel MOSFET (NMOS). Label the terminals. Indicate the channel length (L). Indicate the half-pitch that corresponds to a technology node.

Do the same for the p-channel MOSFET (PMOS).

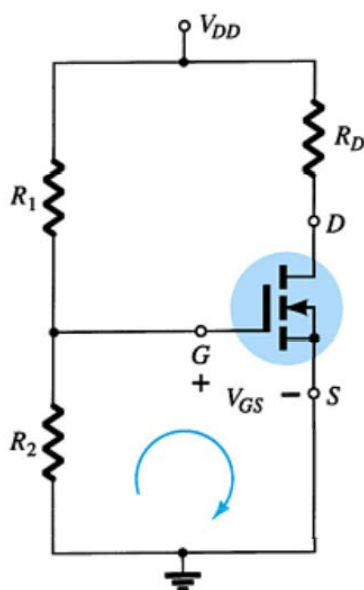
Explain why we may justifiably assume that the gate current of a MOSFET is always zero.

Question 2

Write down the conditions for the three operating modes of an NMOS with respect to V_{GS} and V_{GD} .

Question 3

Refer to the following circuit for this question. Given: $V_{th} = 0.8V$, $K = 1.2mA/V^2$, $V_{DD} = 5V$ and $R_D = 2k\Omega$.



- Determine the state of the MOSFET when $R_1 = 9R_2$ and find V_{GS} , I_D and V_{DS} .
- Determine the state of the MOSFET when $3R_1 = 7R_2$ and find V_{GS} , I_D and V_{DS} .
- Determine the state of the MOSFET when $4R_1 = R_2$ and find V_{GS} , I_D and V_{DS} .

Question 4

An NMOS has the following parameters: $W/L = 5$, $t_{ox} = 10nm$, $V_{th} = 0.35V$.

- Determine the oxide capacitance per unit area, C_{ox} .
- Determine the conductance parameter, K_n .
- Sketch the transfer characteristic (I_D vs V_{GS}) by determining the respective values of I_D when V_{GS} is increased from 0 to 0.9V in steps of 0.1V. Assume the NMOS does not change between triode and saturation modes.
- Sketch the drain characteristic (I_D vs V_{DS}) for V_{GS} of 0.7V and 0.9V by determining the respective values of I_D when V_{DS} is increased from 0 to 0.9V in steps of 0.1V.

Assume the values of carrier mobility provided in the reference sheet.

Question 5

A PMOS has the same parameters as the NMOS described in the previous question and V_{th} is of the same magnitude.

- Determine the conductance parameter, K_p .
- Sketch the transfer characteristic (I_D vs V_{GS}) by determining the respective values of I_D when V_{GS} is decreased from 0 to -0.9V in steps of 0.1V. Assume the NMOS does not change between triode and saturation modes.
- Sketch the drain characteristic (I_D vs V_{DS}) for V_{GS} of -0.7V and -0.9V by determining the respective values of I_D when V_{DS} is decreased from 0 to -0.9V in steps of 0.1V.
- Account for the difference in the magnitude of I_D observed in the transfer and drain characteristics between the NMOS and PMOS.

Assume the values of carrier mobility provided in the reference sheet.

Question 6

A matched pair of NMOS and PMOS have $K_n = K_p = 1.2\text{mA/V}^2$ and $V_{th} = 0.4\text{V}$, and are used to implement a CMOS inverter that requires a supply voltage of $V_{DD} = 1.8\text{V}$. The NMOS has $L = 0.18\mu\text{m}$.

- Find the gate capacitance (C_{gate}) for the NMOS.
- Find the maximum value of I_D . See answers for hints if you are stuck.
- Hence, find an estimate of the switching time delay (τ).
- Find the total power dissipated in the CMOS inverter.

Question 7

Assuming constant field scaling, derive the scaling factors for C_{gate} , C_{ox} , K , and I_D . Hence, derive the scaling factors for the switching delay time and power dissipated per transistor. Use your results on scaling factors to explain the performance benefits of CMOS downscaling.

Question 8

Explain why the static power dissipation in a CMOS inverter is zero.

Numerical Answers

Question 3:

- a) Cut-off mode, $V_{GS} = 0.5V$, $I_D = 0A$, $V_{DS} = 5V$
- b) Saturation mode, $V_{GS} = 1.5V$, $I_D = 0.588mA$, $V_{DS} = 3.824V$ (Note: $V_{GD} < 0$)
- c) Triode mode, $V_{GS} = 4V$, $V_{DS} = 0.32V$, $I_D = 2.34mA$ (Note: $V_{GD} > V_{th}$)

Note: For the triode mode solution, you need to solve a quadratic equation.

Question 4: $C_{ox} = 3.453 \times 10^{-3} \text{ F/m}$, $K_n = 1.04mA/V^2$

$V_{DS} (V)$		0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
$I_D (mA)$	$V_{GS} = 0.7V$	0	0.062	0.106	0.124	0.127	0.127	0.127	0.127	0.127	0.127
	$V_{GS} = 0.9V$	0	0.104	0.186	0.249	0.290	0.311	0.313	0.313	0.313	0.313

Question 5: $K_p = 0.345mA/V^2$

Values of I_D will reduce to a third of the values relative to the NMOS.

Question 6:

- a) $C_{gate} = 0.648fF$
- b) Hint: I_D reaches its maximum in a matched CMOS inverter when $V_{in} = V_{GS(NMOS)} = V_{DD}/2 = 0.9V$.

Hence maximum $I_D = 0.3mA$

- c) Switching time delay = 3.9ps
- d) Power dissipated in CMOS inverter = 0.54mW