

EE3220 System-on-Chip Design

Quiz #1 Results

Summary

- Average: 42.2 / 60 (70.3%)
- Highest: 57 (95%)
- Standard Deviation: 7.76 / 60 (12.9%)
- Above Average: DOING FINE
- Below 30/60: TIME TO CATCH UP

Some Important Concepts (A)

- $Performance \propto \frac{1}{Execution\ Time} = \frac{Clock\ Frequency \times IPC}{Instruction\ \#}$
- IPC = Number of Instructions executed Per Cycle
 - Simple Non-Pipelined Processors can achieve 1 clock per cycle at low clock speed.
 - Simple Pipelined Processors cannot achieve 1 clock per cycle even at low clock speed due to control hazards and data hazard.
 - Pipelining improves performance with **HIGHER CLOCK FREQUENCY** not higher IPC.
- Superscalar Processors can achieve >1 clocks per cycle
 - Superscalar Processors issue and execute multiple instructions per cycle.
 - Superscalar Processor improves performance with **HIGHER IPC**.
 - This IPC increase is not related to Pipelining.

Some Important Concepts (B)

- Moore's Law
 - Moore's Law has been valid up until 15 years ago
 - For a long time, Smaller Feature Sizes (Same Design):
 - **LOWER UNIT COST, BETTER PERFORMANCE (CLOCK SPEED), LOWER POWER**
- Deep Submicron Era
 - Feature Size cannot keep going smaller, when approaching **MOLECULAR DIMENSIONS**
 - It's increasing more **DIFFICULT** and **EXPENSIVE** to adopt smaller feature size.
 - Smaller Feature Sizes (Same Design) may gain better unit cost or performance.
 - Smaller Feature Sizes still provide **LOWER POWER** and allow **BIGGER DESIGN**

Important Concepts (C)

- Debounce Delay
 - Typically, 5 – 50ms
- Signal sampled when someone presses the Push Button **ONCE**

