EE3220 System on Chip Design

Lecture Note 8

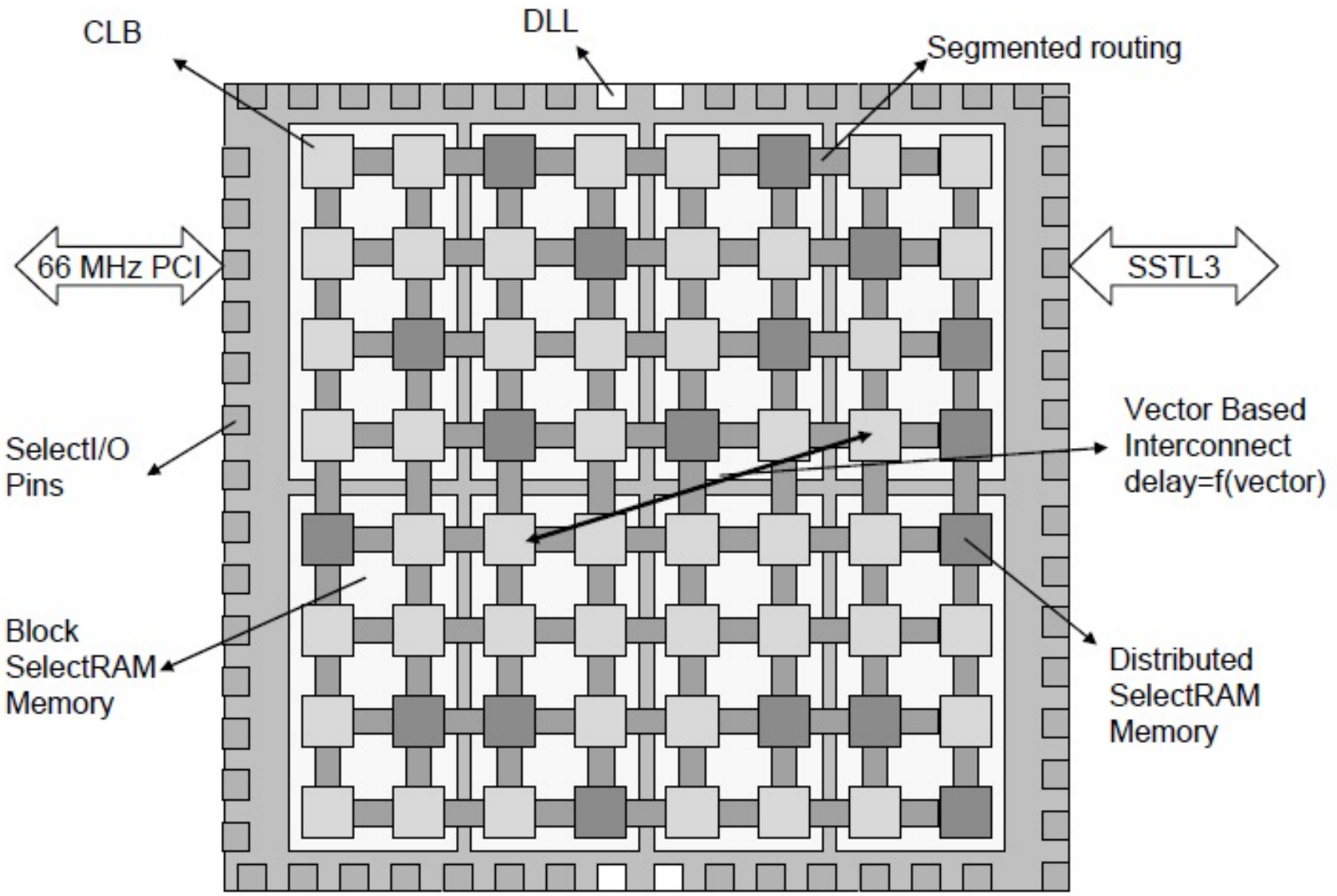
FPGA System-on-Chip & ARM Processor

CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Overview

- FPGA Overview
- FPGA + ARM Processor
  - FPGA Electronic Design Automation Platform – Vivado & Vitis AI
  - Multi-processor System-on-Chip (MPSoC)
  - Building Blocks of a Generic Microcontroller
  - PicoBlaze vs. MicroBlaze
- Zynq SoC (AP SoC)
- Zynq SoC Processing System (PS)
- Processor Peripherals
- Clock, Reset, and Debug Features
- AXI Interfaces
- Summary

Recall: FPGA Chip Overview



CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

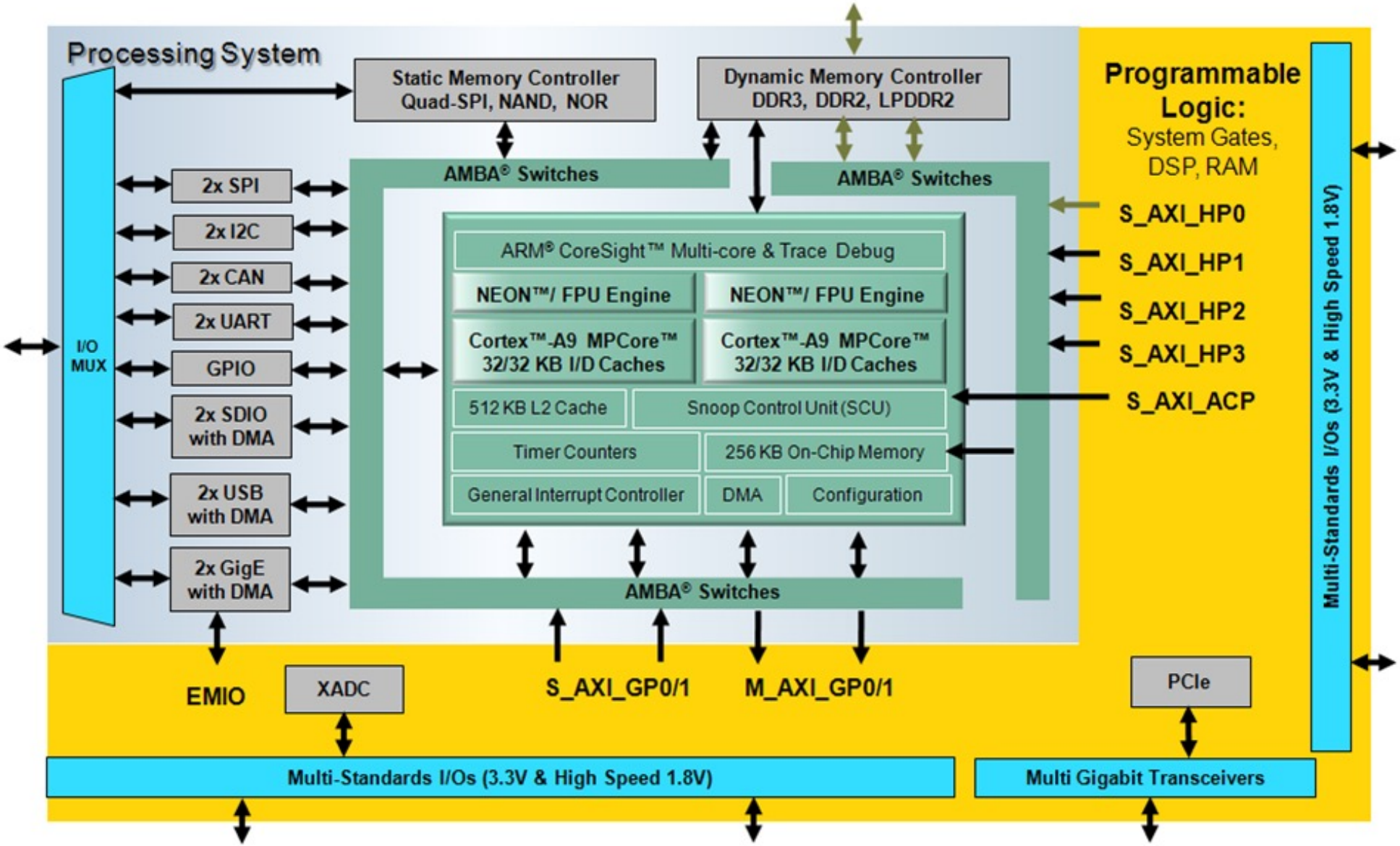
MPSoC – Xilinx Zynq

Zynq® UltraScale+™ MPSoCs: CG Devices

		Device Name[1]	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
Processing System (PS)	Application Processor Unit	Processor Core	**Dual-core** ARM® Cortex™-A53 MPCore™ up to 1.3GHz						
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB						
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore up to 533MHz						
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core						
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC						
		Static Memory Interfaces	NAND, 2x Quad-SPI						
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet						
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains						
		Security	RSA, AES, and SHA						
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor						
PS to PL Interface			12 x 32/64/128b AXI Ports						
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256	469	504	600
		CLB Flip-Flops (K)	94	141	176	234	429	461	548
		CLB LUTs (K)	47	71	88	117	215	230	274
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1
		UltraRAM (Mb)	-	-	13.5	18.0	-	27.0	-
	Clocking	Clock Management Tiles (CMTs)	3	3	4	4	4	8	4
	Integrated IP	DSP Slices	240	360	728	1,248	1,973	1,728	2,520
		PCI Express® Gen 3x16 / Gen4x8	-	-	2	2	-	2	-
		150G Interlaken	-	-	-	-	-	-	-
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-
		AMS - System Monitor	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	16	16	24	24	24
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-
	Speed Grades	Extended[2]	-1 -2 -2L						
		Industrial	-1 -1L -2						

CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

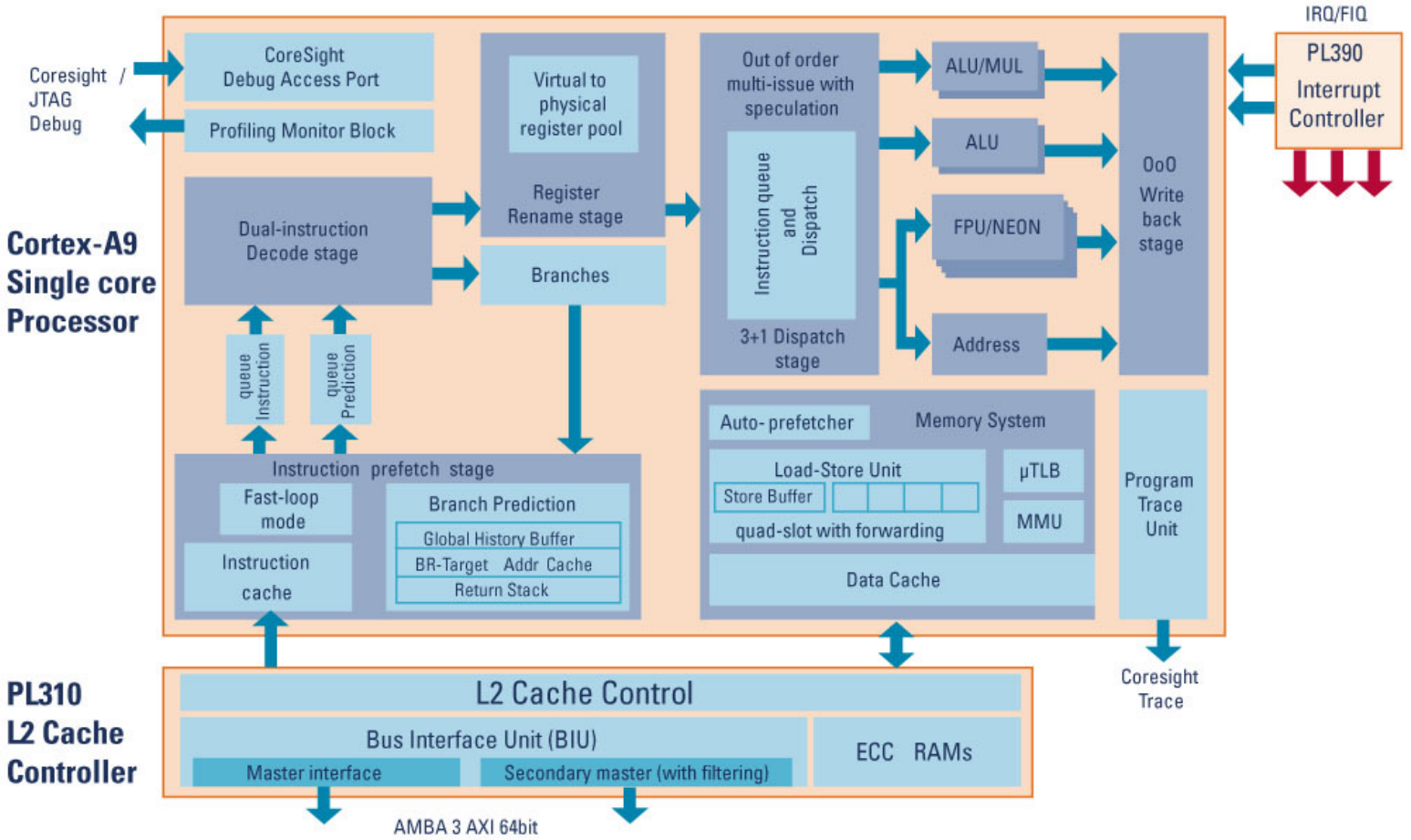
Zynq-7000 SoC Block Diagram - FPGA + ARM Processor



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

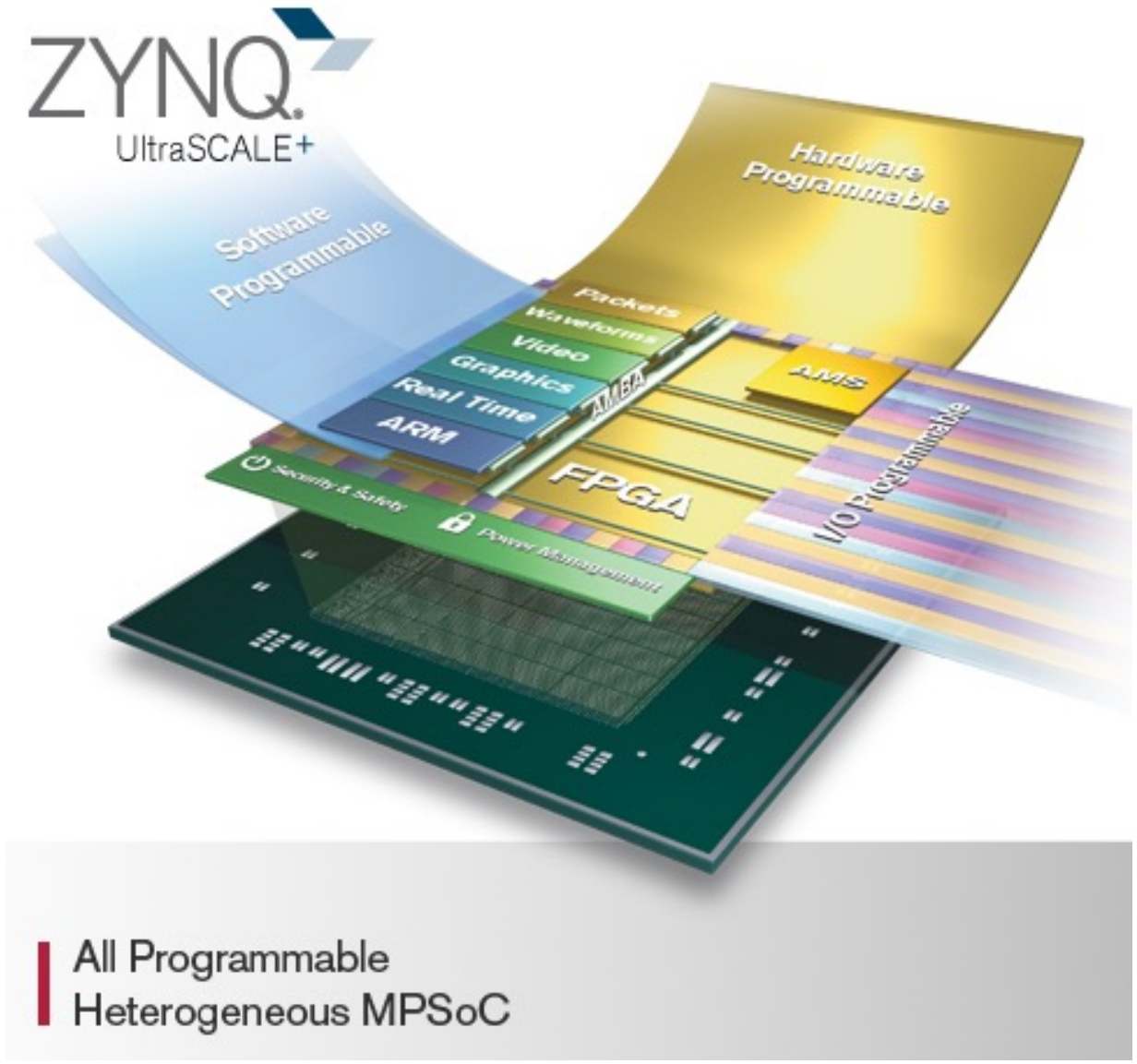
ARM Cortex-A9 Processor Micro-Architecture

- Instruction pipeline supports out-of-order instruction issue and completion
- Register renaming to enable execution speculation
- Non-blocking memory system with load-store forwarding
- Fast loop mode in instruction pre-fetch to lower power consumption



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Multi-processor System-on-Chip (MPSoC)



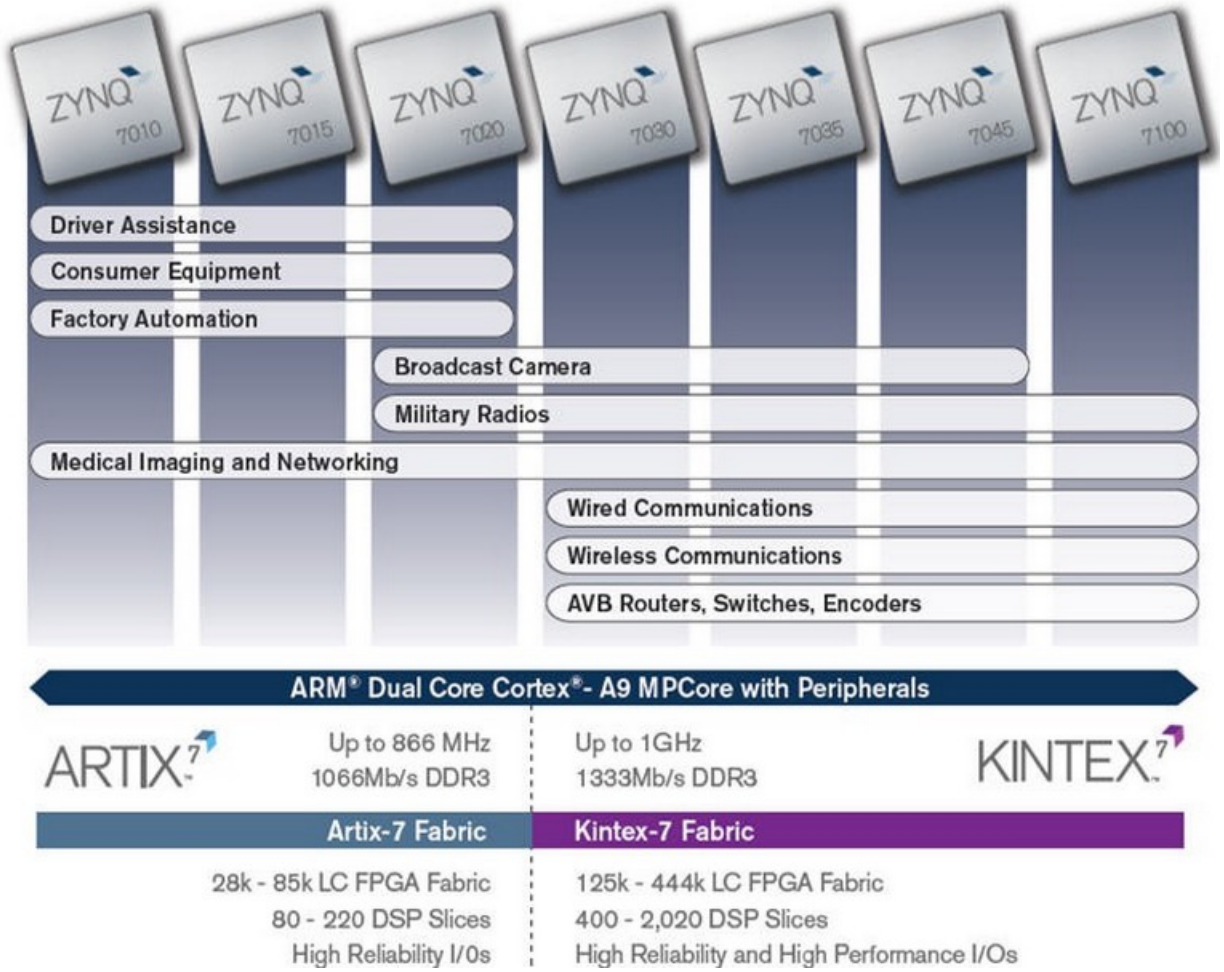
CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Embedded Design Architecture in Zynq

- Embedded design with Zynq is based on:
  - Processor and peripherals
  - Dual ARM® Cortex™ -A9 processors of Zynq-7000 SoC
  - AXI interconnect
  - AXI component peripherals
  - Reset, clocking, debug ports
  - Software platform for processing system
  - Bare Metal Applications or OS's (e.g. Linux, FreeRTOS)
  - C language support
  - Processor services
  - C drivers for hardware
  - User application
  - Interrupt service routines (optional)

The PS and the PL

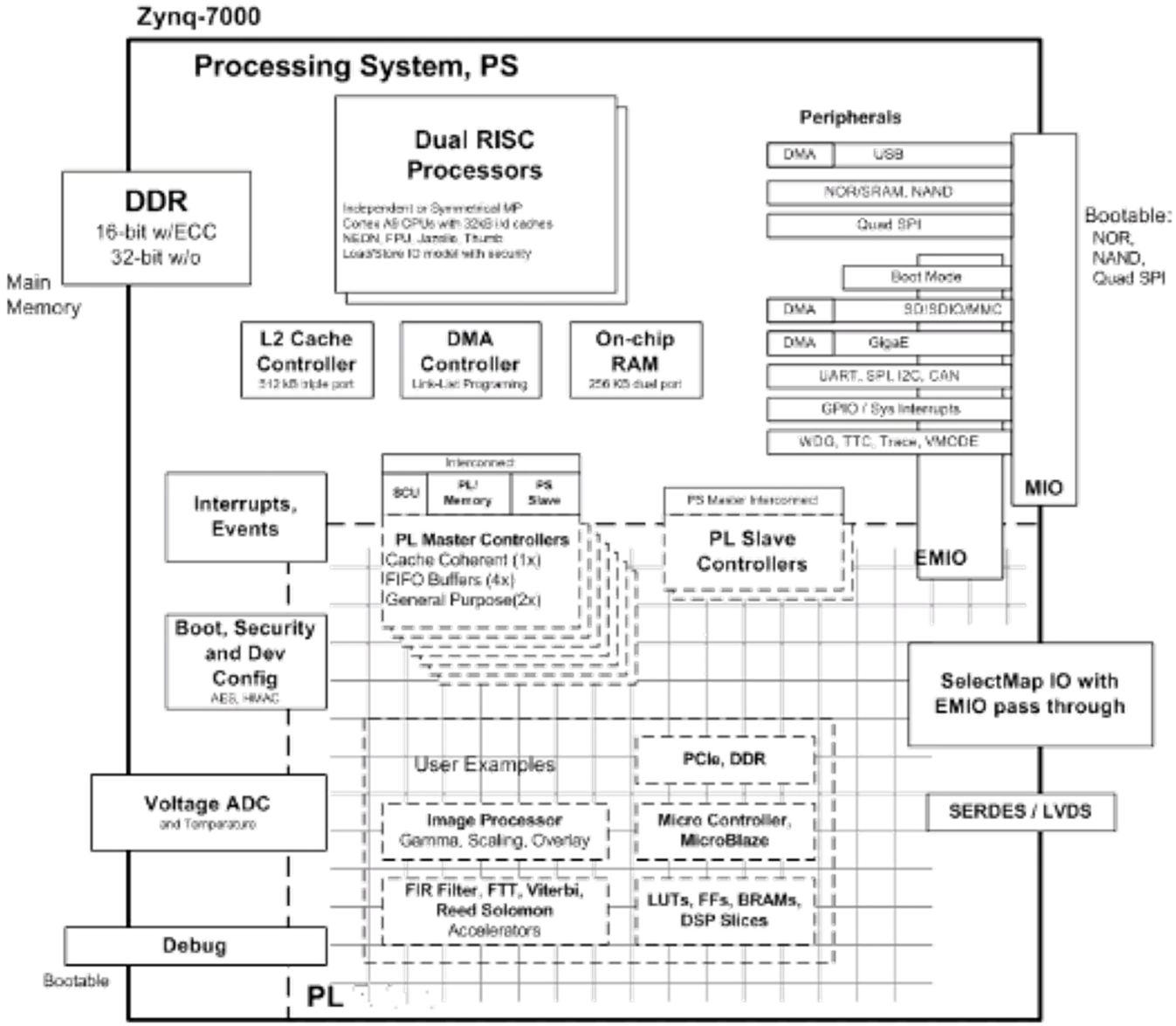
- The Zynq-7000 SoC architecture consists of two major sections
  - PS: Processing system
  - Dual ARM Cortex-A9 processor based
  - Single core versions available
  - Multiple peripherals
  - Hard silicon core
  - PL: Programmable logic
  - Uses the same 7 series programmable logic
  - Artix™-based devices: Z-7010, Z-7015 and Z-7020 (high-range I/O banks only)
  - Kintex™-based devices: Z-7030, Z-7035, Z-7045, and Z-7100 (mix of high-range and high-performance I/O banks)



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

PS Components

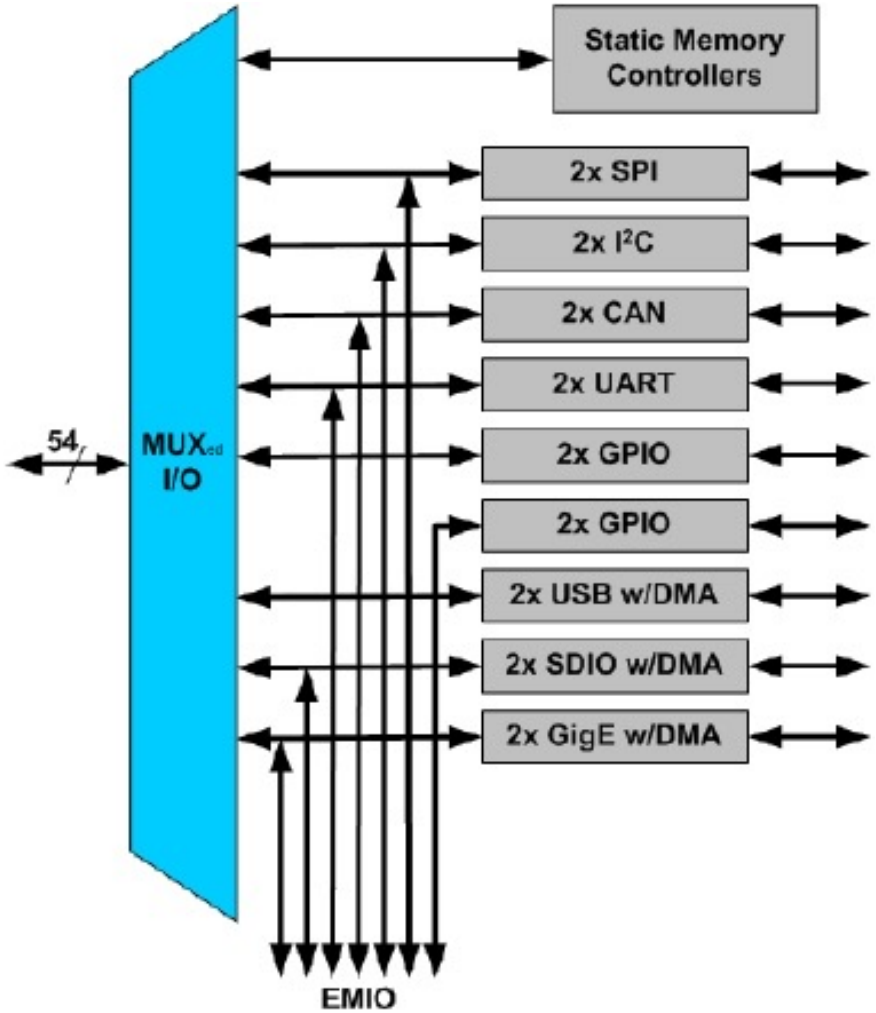
- The Zynq SoC processing system consists of the following blocks
  - Application processing unit (APU)
  - I/O peripherals (IOP)
  - Multiplexed I/O (MIO), extended multiplexed I/O (EMIO)
  - Memory interfaces
  - PS interconnect
  - DMA, Timers
  - Public and private
  - General interrupt controller (GIC)
  - On-chip memory (OCM): ROM and RAM
  - Debug controller: CoreSight



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Zynq Architecture Built-in Peripherals

- Two USB 2.0 OTG/Device/Host
- Two Tri- Mode GigE (10/100/1000)
- Two SD/SDIO interfaces
  - Memory, I/O and combo cards
- Two CAN 2.0Bs, SPIs , I2Cs, UARTs
- Four GPIO 32bit Blocks
  - 54 available through MIO; other available through EMIO
- Multiplexed Input/Output (MIO)
  - Multiplexed pinout of peripherals and static memories
- Extended MIO
  - Maps PS peripheral ports to the PL



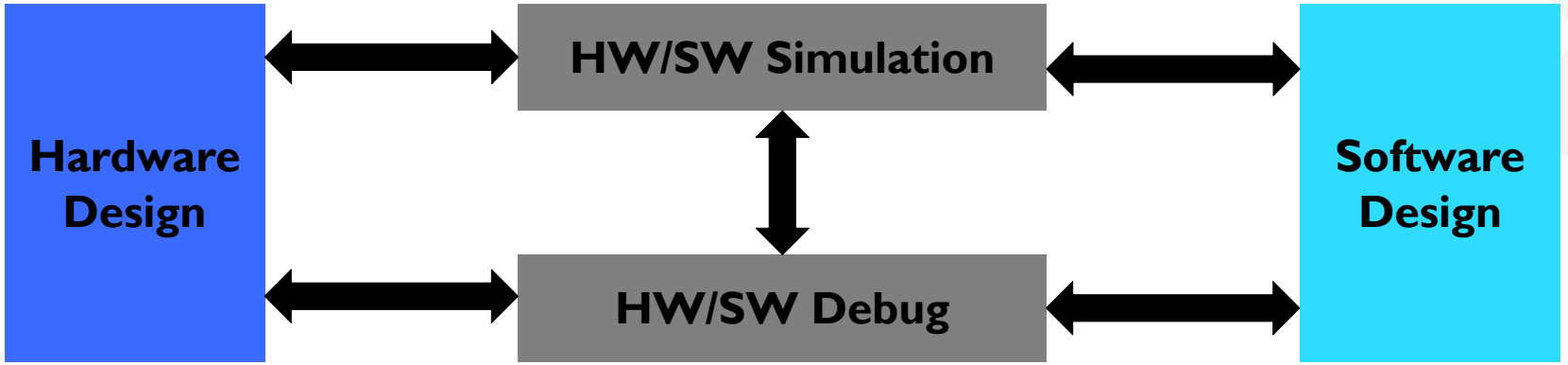
CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Xilinx Vivado

- What are Vivado, IP Integrator and SDK?
  - Vivado is the tool suite for Xilinx FPGA design and includes capability for embedded system design
  - IP Integrator, is part of Vivado and allows system level design of the hardware part of an Embedded system
  - Integrated into Vivado
  - Vivado includes all the tools, IP, and documentation that are required for designing systems with the Zynq-7000 SoC hard core and/or Xilinx MicroBlaze soft core processor
  - Vivado + IPI replaces ISE/EDK
  - SDK is an Eclipse-based software design environment
  - Enables the integration of hardware and software components
  - Links from Vivado
- Vivado is the overall project manager and is used for developing non-embedded hardware and instantiating embedded systems
  - Vivado/IP Integrator flow is recommended for developing Zynq embedded systems

Vivado Components

- Vivado/IP Integrator
  - Design environment for configuration of PS, and hardware design for PL
  - Hardware Platform (xml)
  - Platform, software, and peripheral simulation
  - Vivado logic analyzer integration
- Software Development Kit (SDK)
  - Project workspace
  - Hardware platform definition
  - Board Support Package (BSP)
  - Software application
  - Software debugging



CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Embedded System Tools: Hardware

- Hardware and software development tools
  - IP Integrator
  - IP Packager
  - Hardware netlist generation
  - Simulation model generation
  - Xilinx Microprocessor Debugger (XMD)
  - Hardware debugging using Vivado logic analyzer

Embedded System Tools: Software

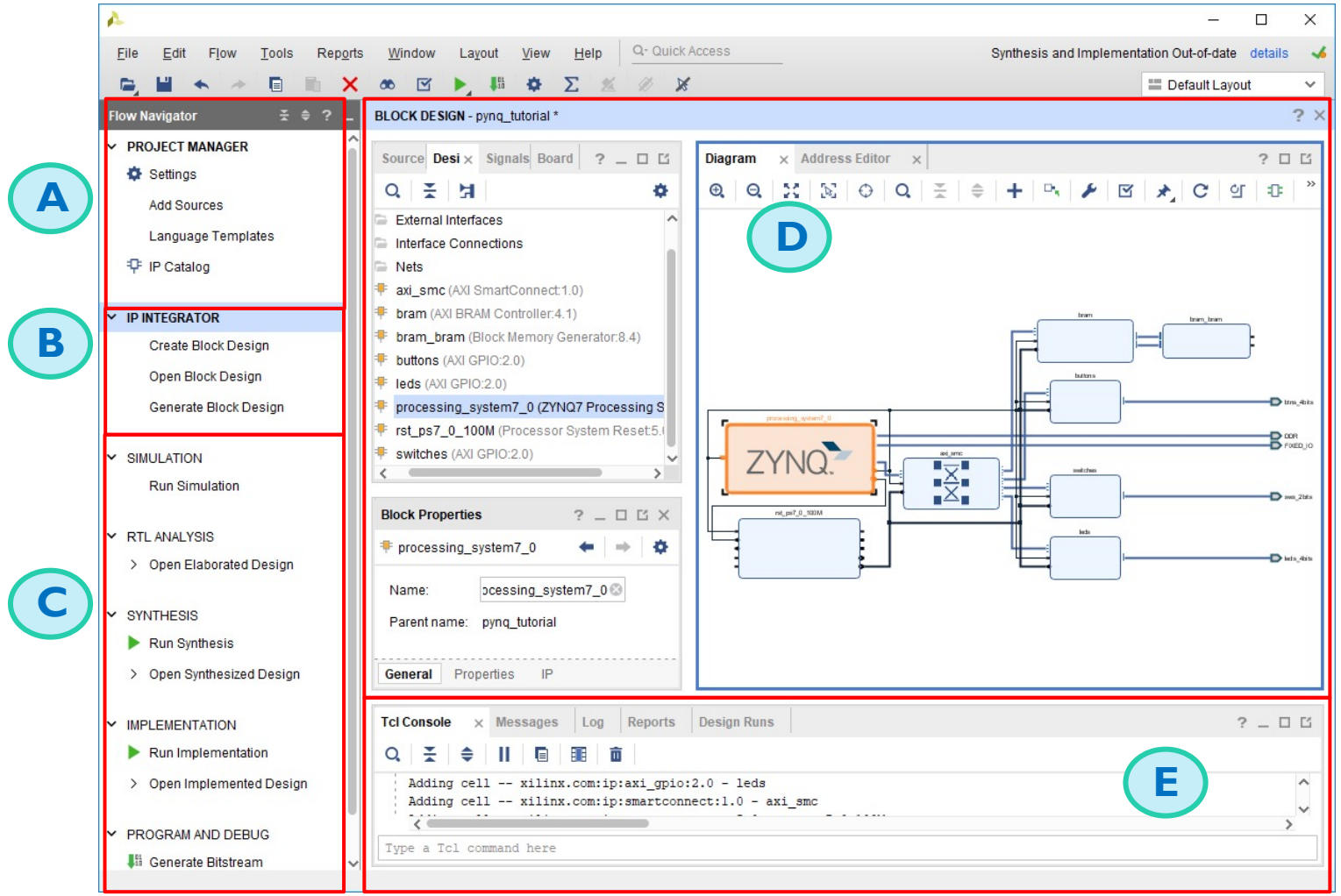
- Eclipse IDE-based Software Development Kit (SDK)
  - Board support package creation
  - GNU software development tools
  - C/C++ compiler for the MicroBlaze and ARM Cortex-A9 processors (gcc)
  - Debugger for the MicroBlaze and ARM Cortex-A9 processors (gdb)
  - TCF framework – multicore debug
- Board support packages (BSPs)
  - Stand-alone BSP
  - Free basic device drivers and utilities from Xilinx
  - NOT an RTOS

CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Vivado View

- Customizable panels

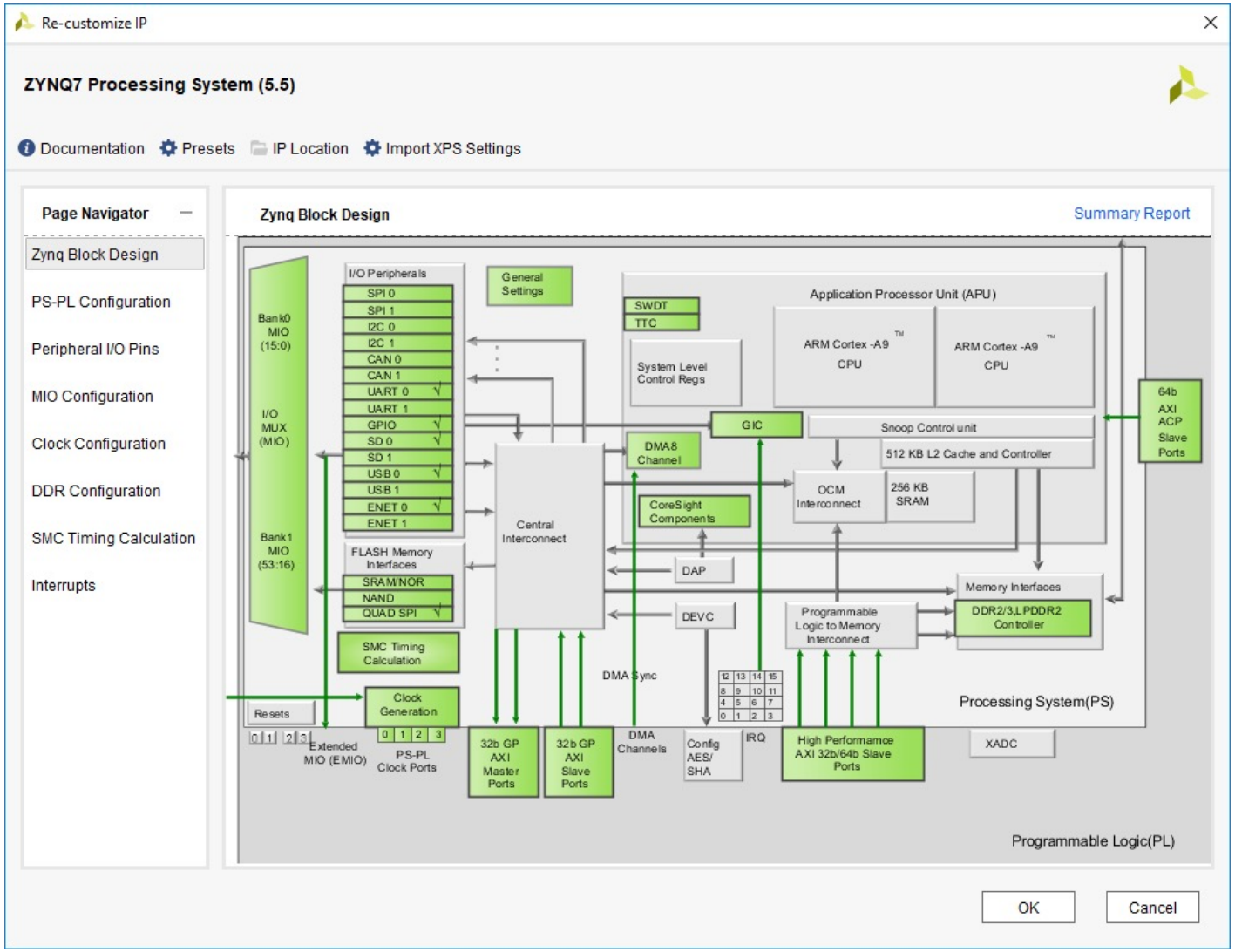
- A: Project Management
- B: IP Integrator
- C: FPGA Flow
- D: Project view/Preview Panel
- E: Console, Messages, Logs



CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Zynq Customization Processing System

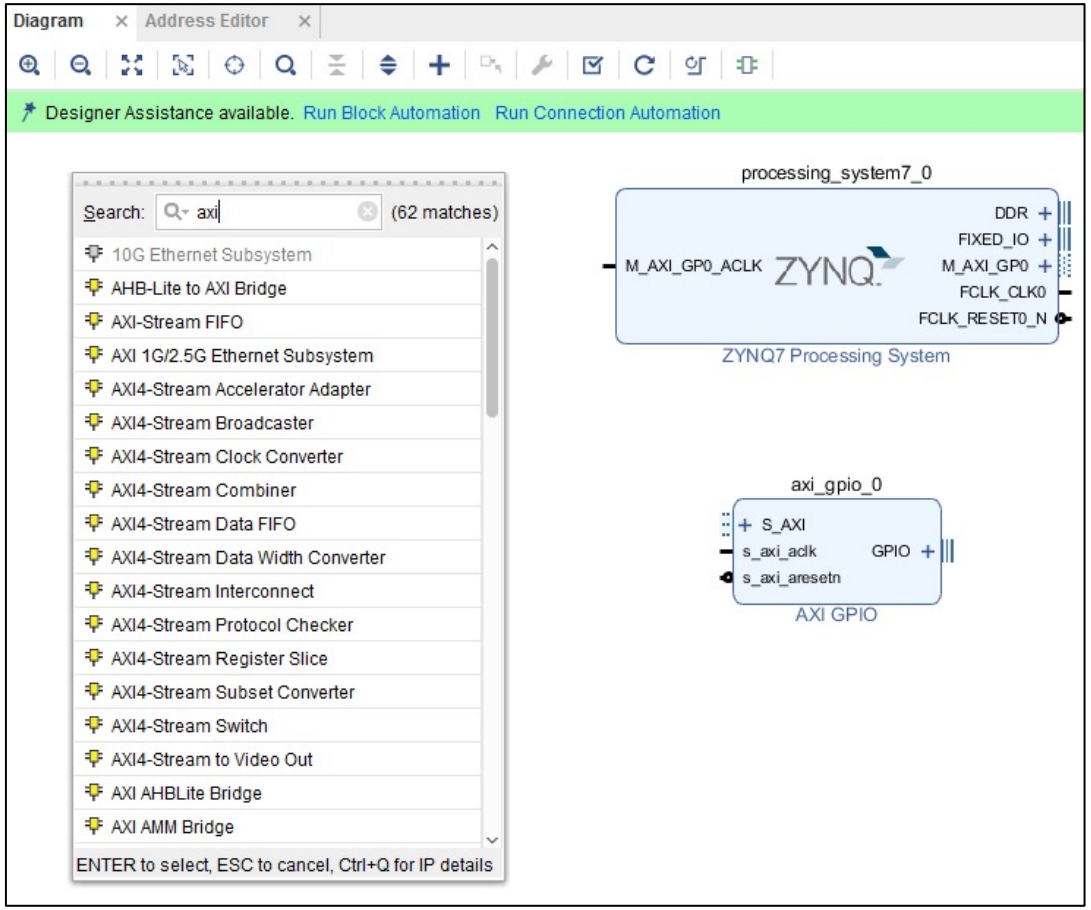
- Zynq Block Design
- PS-PL Interface Configuration
- Peripheral I/O Pins
- MIO Configuration/Table View
- Clock Configuration
- DDR Configuration
- SMC Timing Calculation
- Interrupts



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Integrator Block Diagram

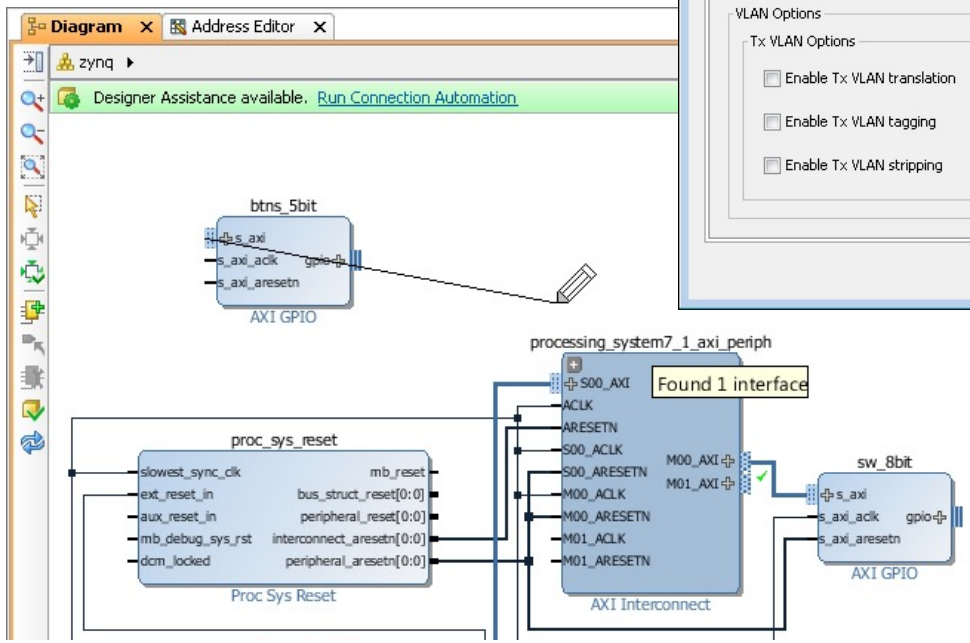
- IP Integrator Block Diagram opens a blank canvas
- IP can be added from the IP catalog
- Drag and drop interface
- Intelligent Design environment
  - Design Assistance
  - Connection automation
  - Highlights valid connections
  - Group, create hierarchal blocks
- Can create and import custom IP using IP Packager

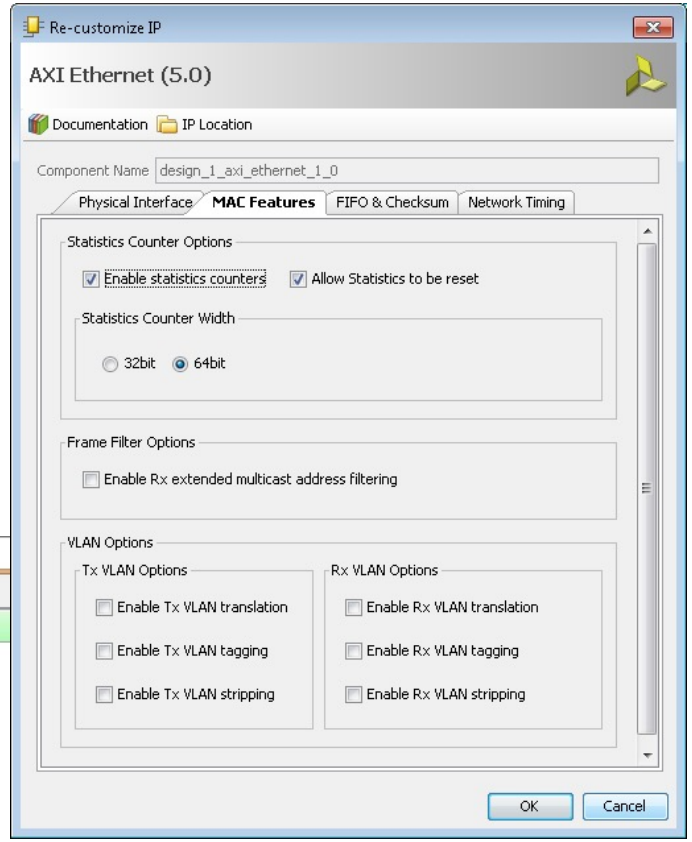


CityU Department of Electrical Engineering 香港城市大學 City University of Hong Kong

Configuring Hardware in IP Integrator

- Double click blocks to access configuration options
- Drag pointer to make connections
  - Highlights valid connections
- Connection Automation
  - Automatically connect recognised interfaces
- Automatically Redraw system

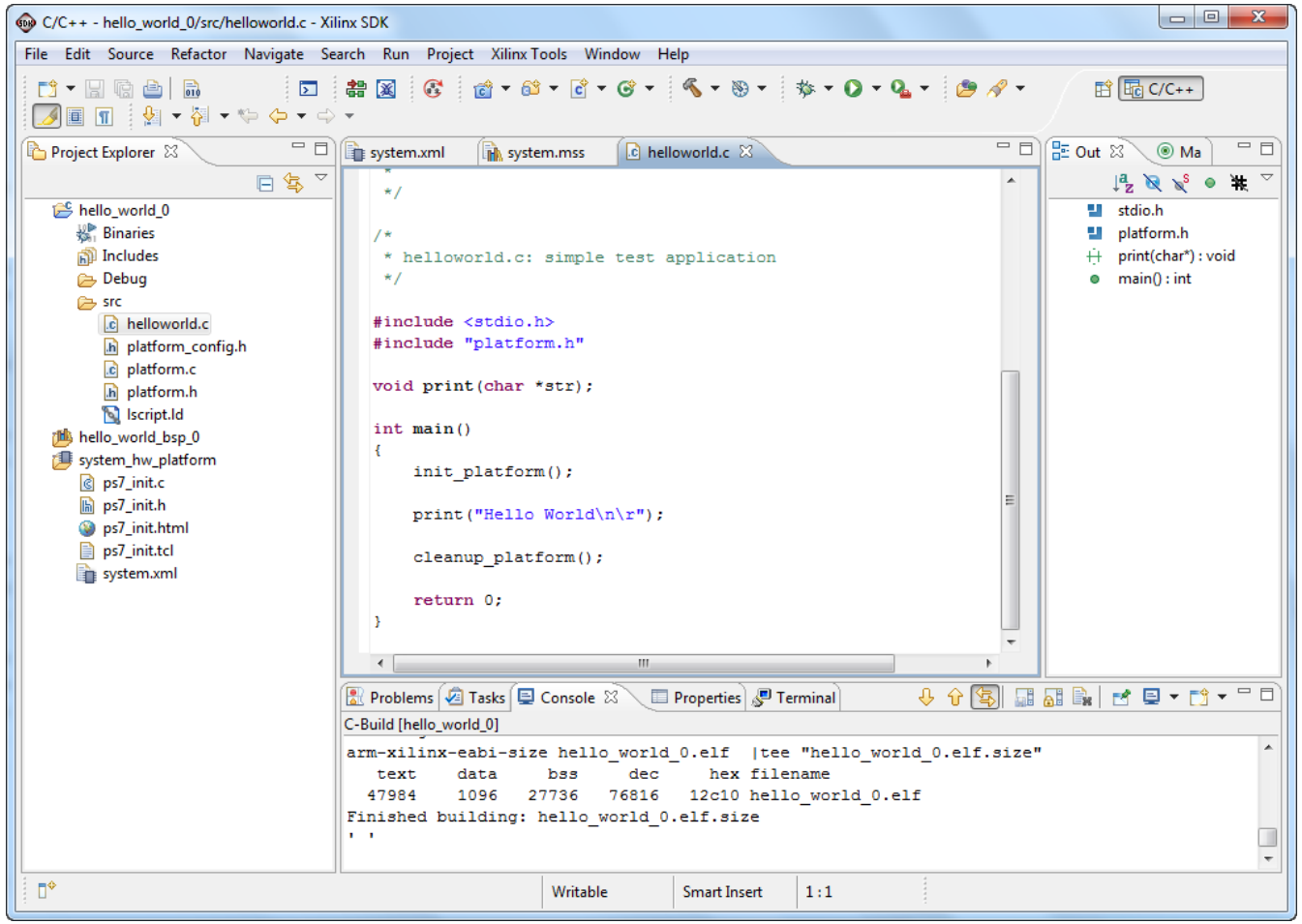




CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Software Development Flow

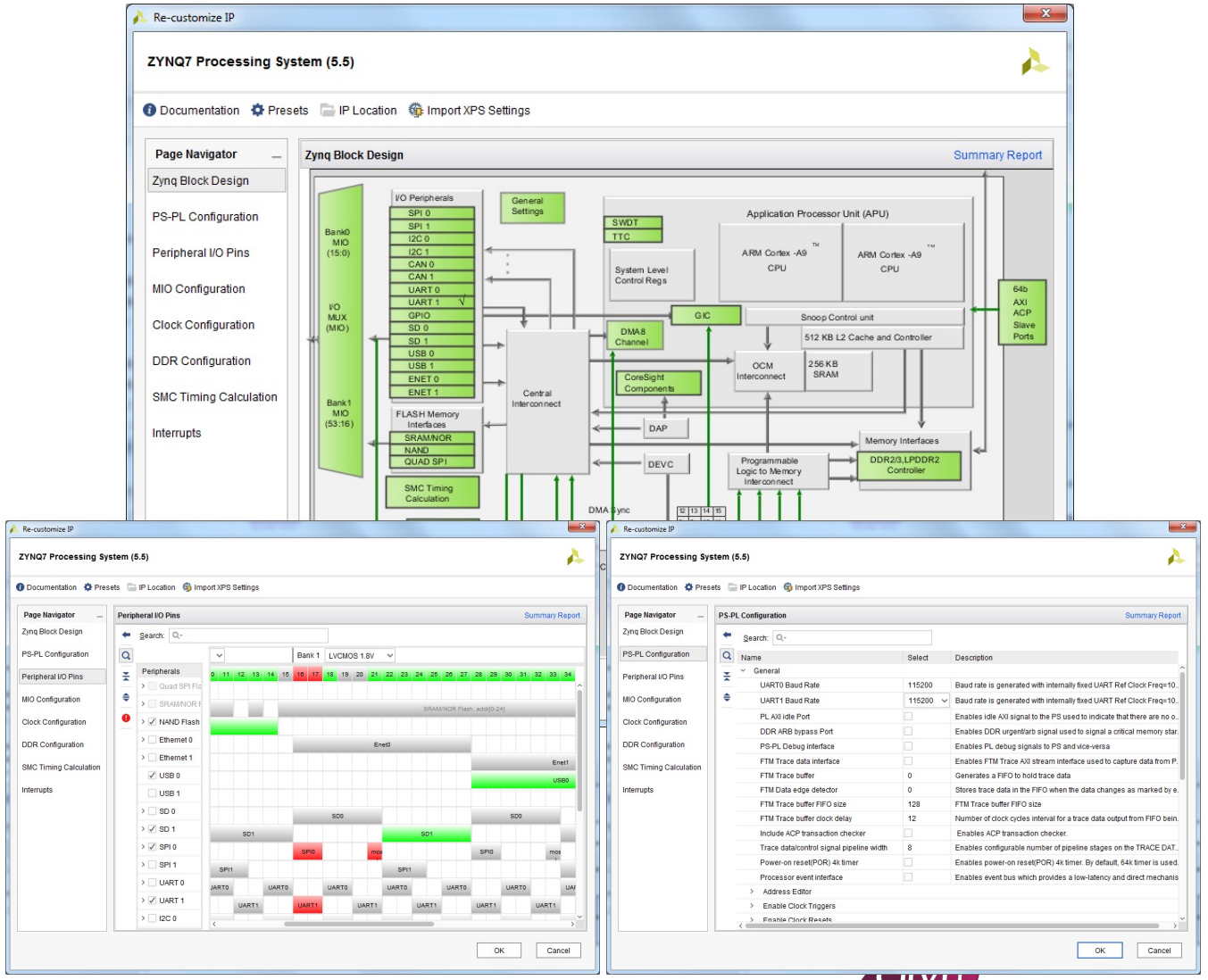
- Create hardware platform project
  - Automatically performed when SDK tool is launched from Vivado project
- Create BSP
  - System software, board support package
- Create software application
- Create linker script
- Build project
  - compile, assemble, link output file *<app_project>.elf*



CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Zynq Configuration GUI

- Provides a graphical view of the PS to configure
  - ARM cores
  - I/O peripherals
  - DDR controller
  - Memory systems
- I/O partitioning between dedicated PS pins and programmable logic I/O
- PS is configured via a set of memory-mapped configuration registers



香港城市大學
City University of Hong Kong

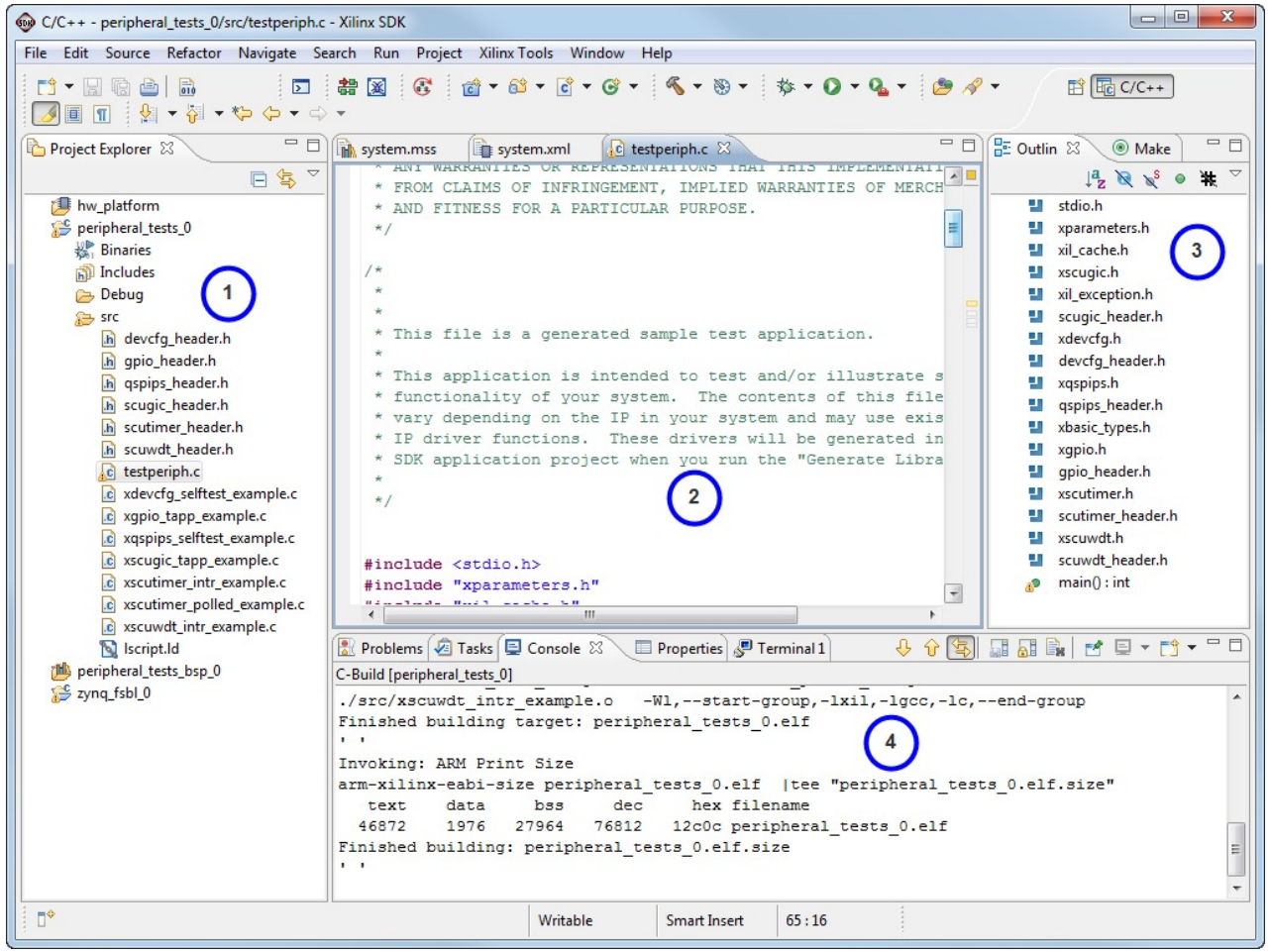
Software Development Kit (SDK)

- Full-featured software design environment
- Separate tool from Vivado – can install standalone for SW teams
- Based on popular Eclipse open-source IDE
- Used for software applications only; hardware design and modifications are done in Vivado
- Well-integrated environment for seamless debugging of embedded targets
- Sophisticated software design environment with many options and features with support for
  - Multiple processors
  - Multiple software platforms
  - Multiple software applications
- Fully Featured C/C++ code editor and error navigator



SDK Workbench Views

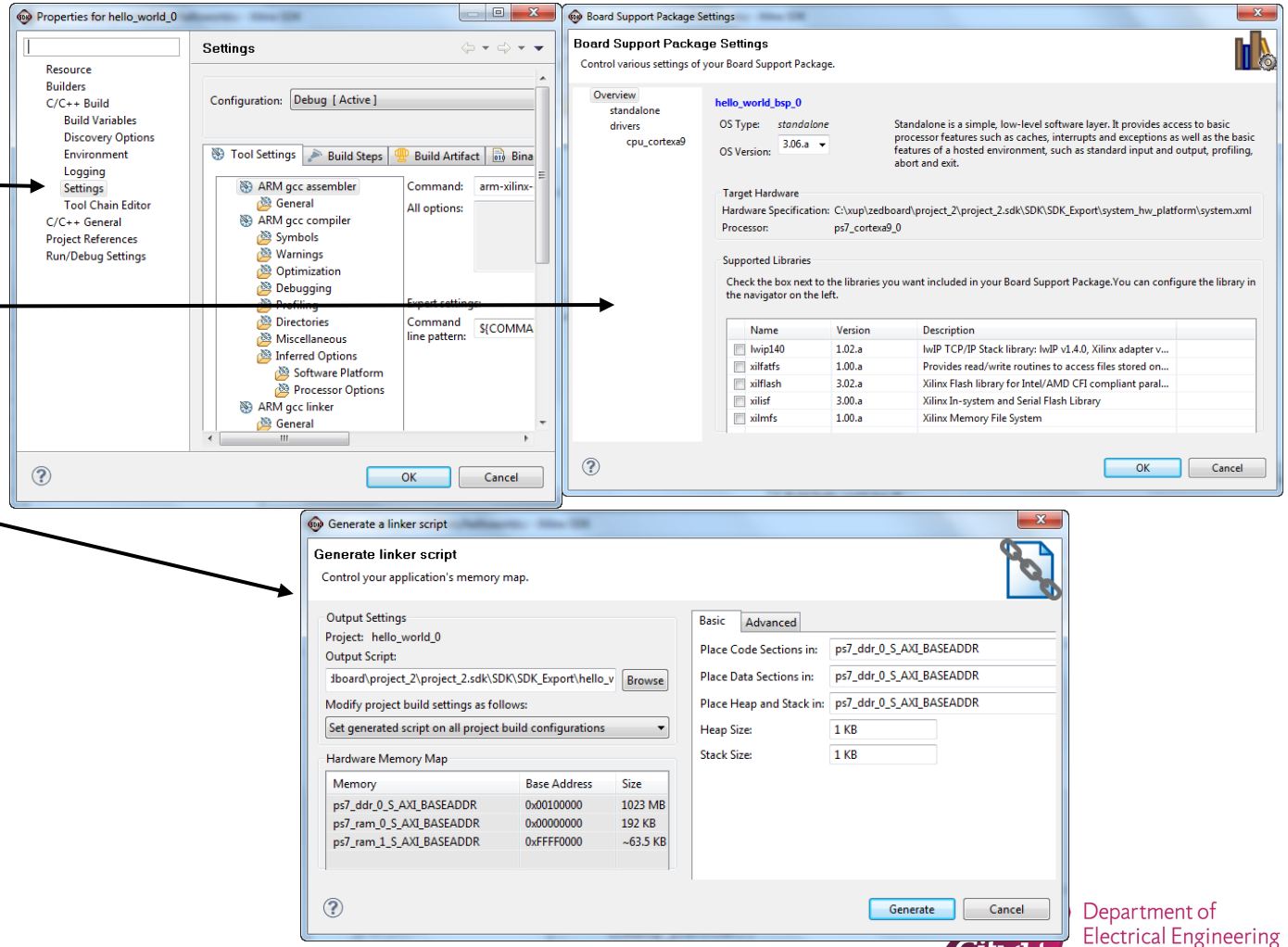
1. C/C++ project outline displays the elements of a project with file decorators (icons) for easy identification
2. C/C++ editor for integrated software creation
3. Code outline displays elements of the software file under development with file decorators (icons) for easy identification
4. Problems, Console, Properties views list output information associated with the software development flow



CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Software Management Settings

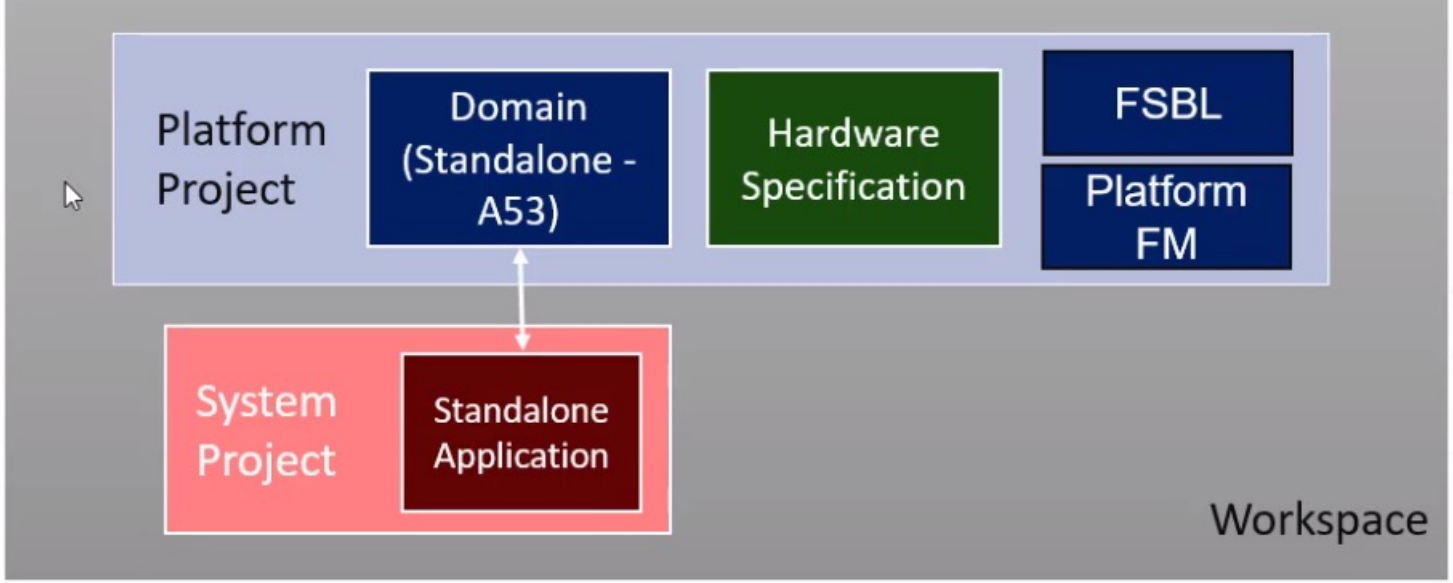
- Software is managed in three major areas
  - Compiler/Linker Options
  - Application program
  - Software Platform Settings
  - Board support package
  - Linker Script Generation
  - Assigning software to memory resources
- Covered in more detail later

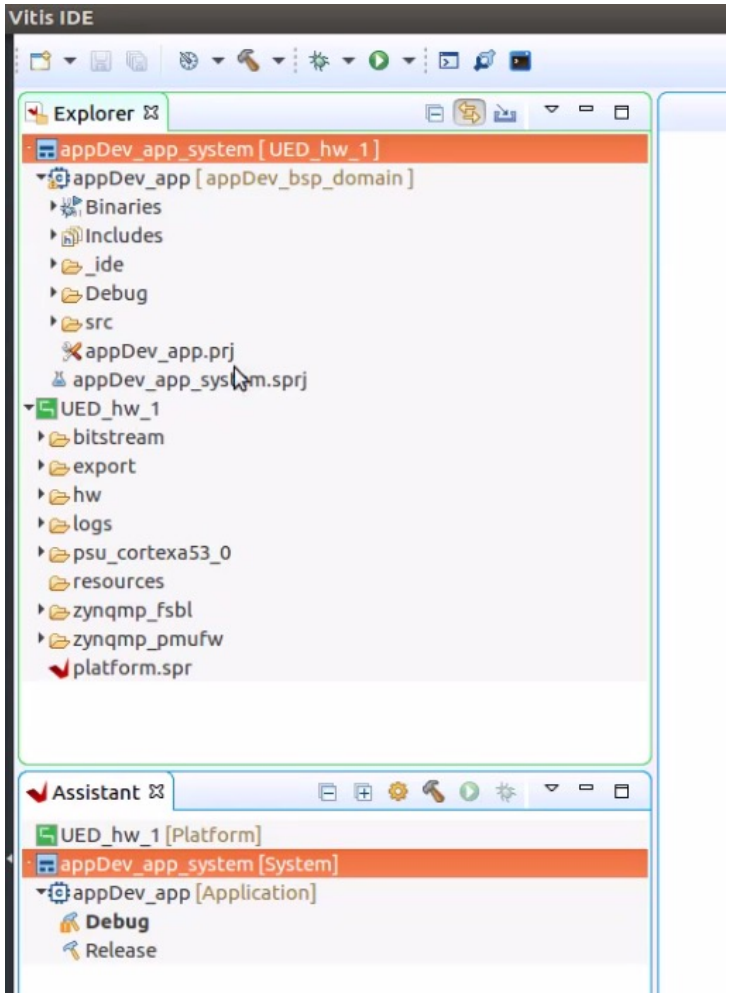


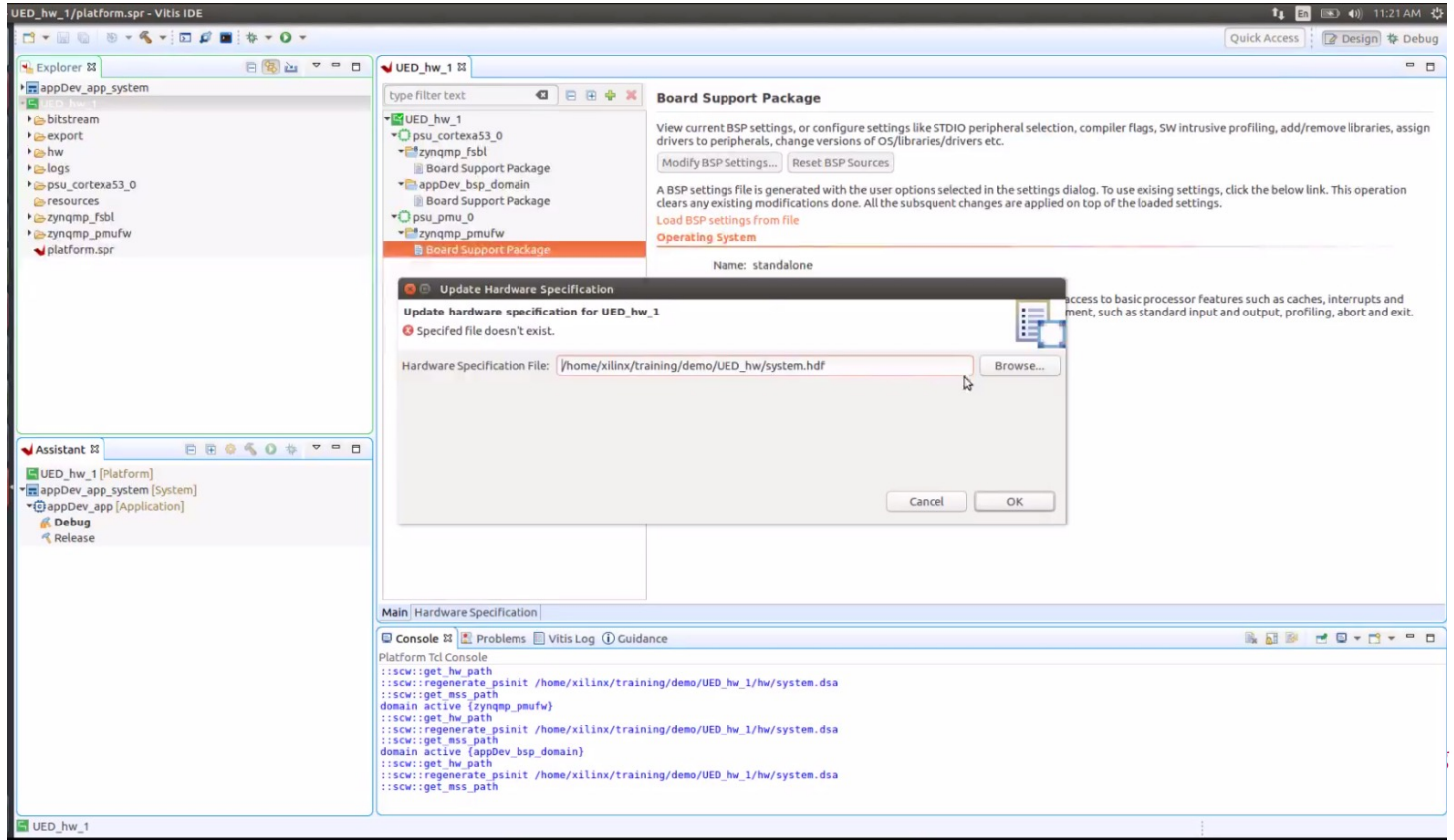
Department of Electrical Engineering
香港城市大學
City University of Hong Kong

From SDK to Vitis IDE

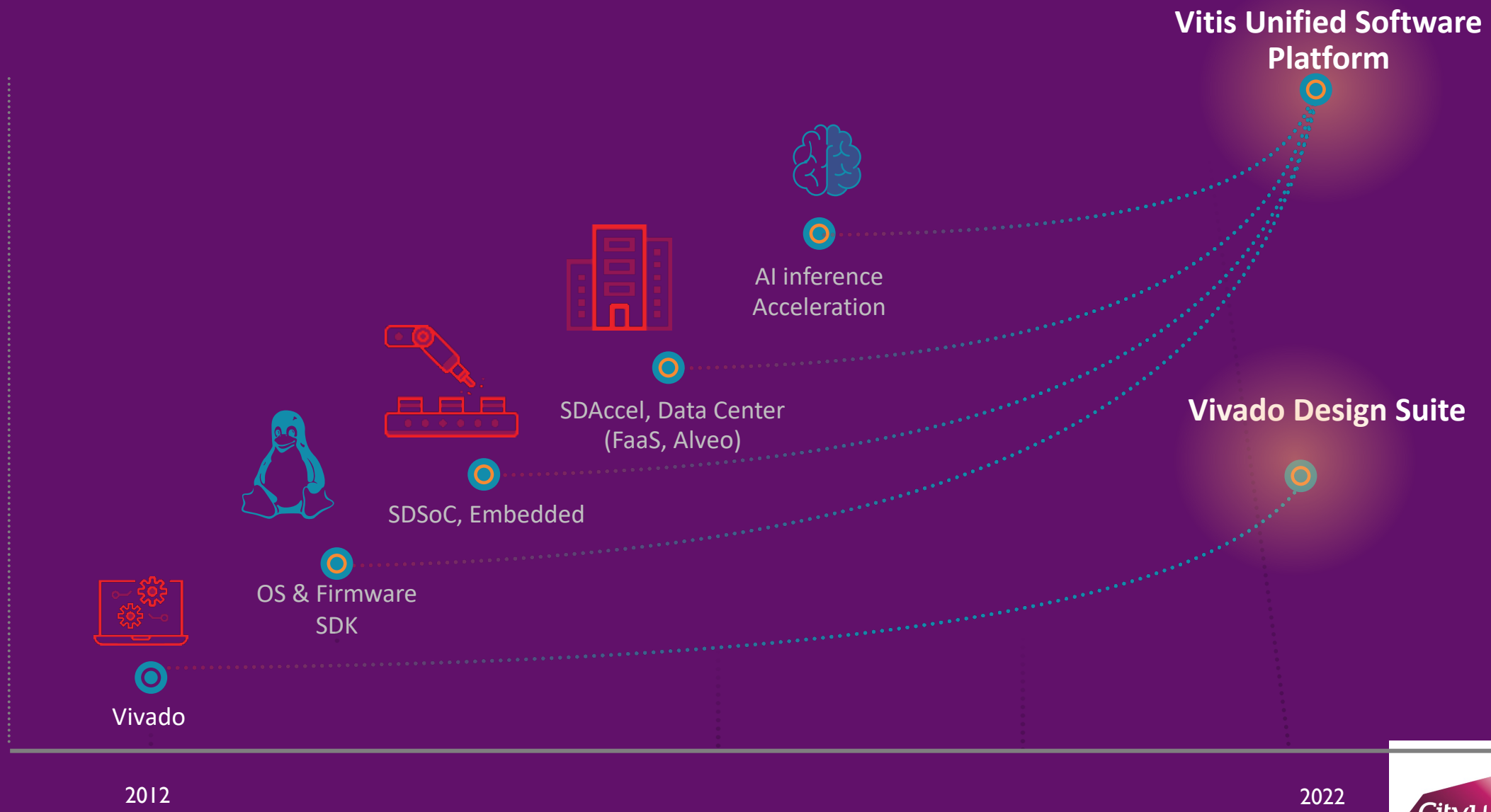
- Platform Project & System Project







Unifying Software Solutions: Vivado & Vitis



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

All Developers Can Build and Deploy on All Platforms

Build



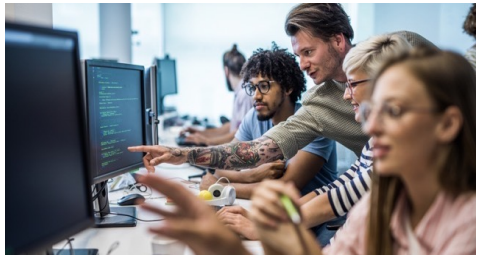
Embedded Developers



Enterprise Application Developers



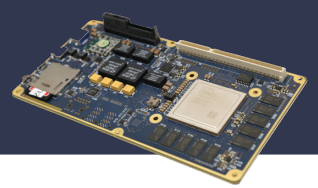
Enterprise Infrastructure Developers



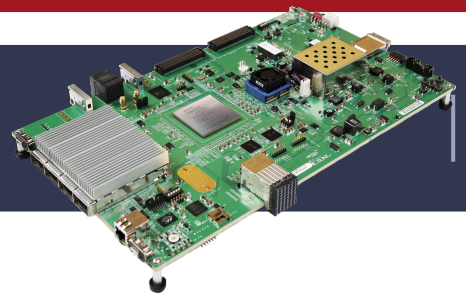
Data & AI Scientists

XILINX VITIS™

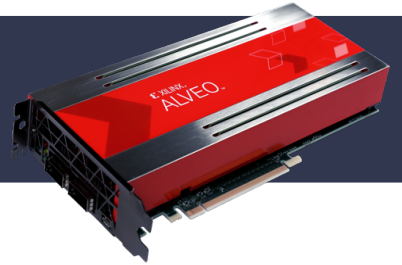
Deploy



Zynq-7000



Zynq UltraScale+ MPSoC



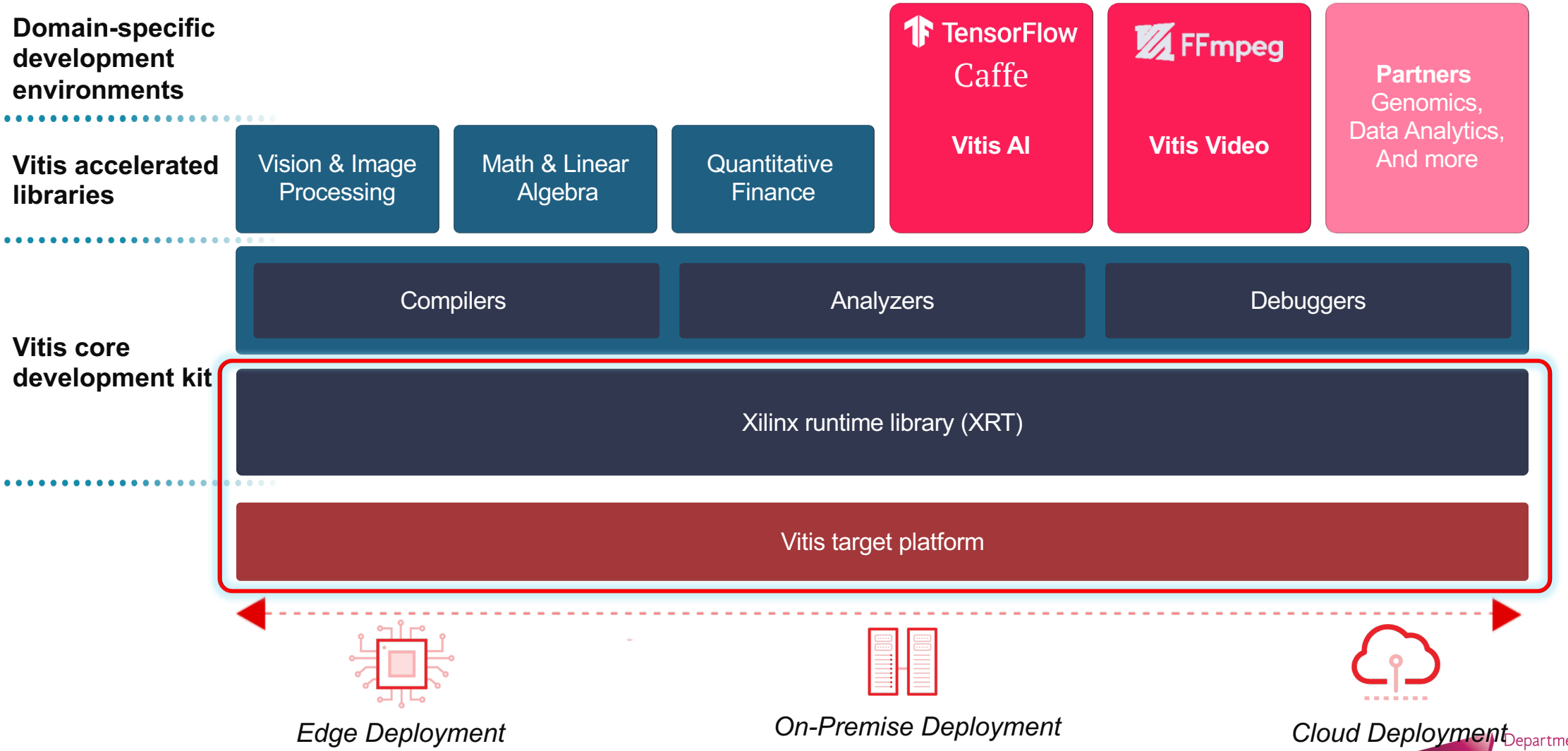
Alveo



Versal ACAPs

CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Vitis Unified Software Platform

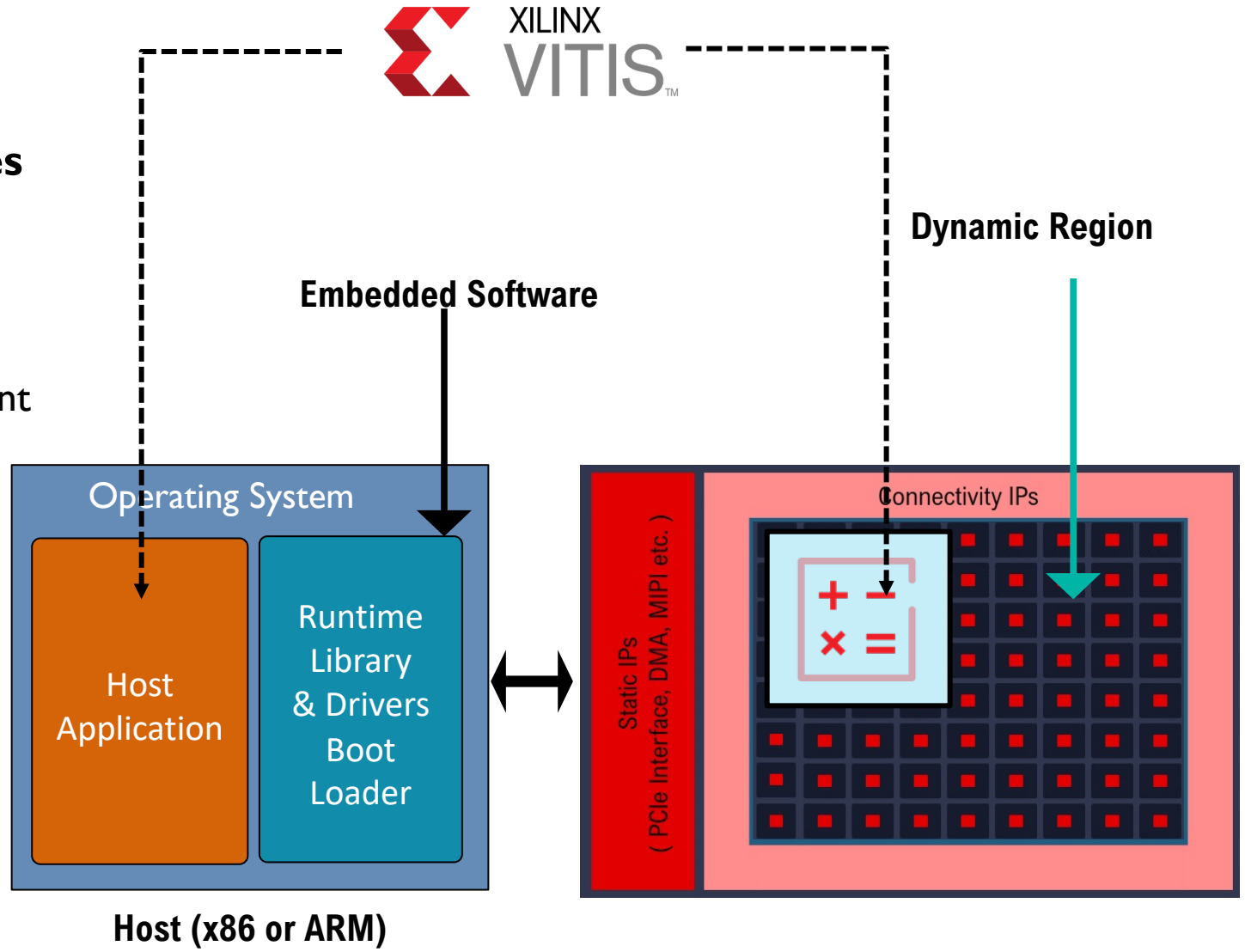


Department of Electrical Engineering
CityU
香港城市大學
City University of Hong Kong

Vitis Target Platform

Base Hardware, Software Architecture

- **For PCIe Accelerator Cards, Includes**
  - PCIe® Interface Logic
  - DDR memory interface controllers
  - XDMA logic etc.
  - Hardware Config & Lifecycle Management
- **For Embedded Devices, Includes**
  - Operating System
  - Runtime library (XRT)
  - Runtime drivers (XRT)
  - Firmware & Boot loader



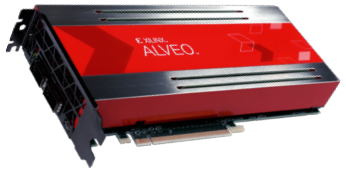
Ready-to-Use Vitis Target Platforms
OR
Build Your Own using Vivado Design Suite

CityU Department of Electrical Engineering 香港城市大學 City University of Hong Kong

Vitis Target Platforms for Alveo Accelerator Cards

Available Today

Alveo U200



UltraScale+ Architecture

1,182k LUTs

Dual slot, full height

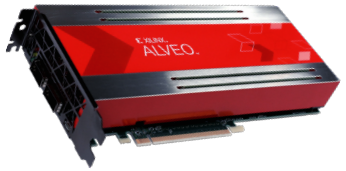
64GB DDR, 77GB/sec

PCIe Gen3

2x QSFP 28 (100GbE)

< 225W

Alveo U250



UltraScale+ Architecture

1,728k LUTs

Dual slot, full height

64GB DDR, 77GB/sec

PCIe Gen3

2x QSFP 28 (100GbE)

< 225W

Alveo U280



UltraScale+ Architecture

1,304k LUTs

Dual slot, full height

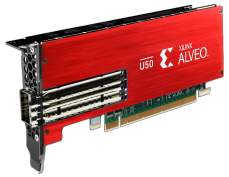
8GB HBM2, 460GB/sec

PCIe Gen3, Gen4, CCIX

2x QSFP 28 (100GbE)

< 225W

Alveo U50



UltraScale+ Architecture

872k LUTs

Single slot, half height

8GB HBM2, 316GB/sec

PCIe Gen3, Gen4, CCIX

1x QSFP 28 (100GbE)

< 75W

CityU Department of Electrical Engineering 香港城市大學 City University of Hong Kong

Vitis Target Platforms for Embedded Platforms

Available Today

Zynq-7000 SoC ZC702



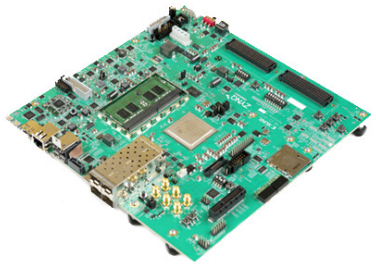
Learn More

Zynq-7000 SoC ZC706



Learn More

Zynq UltraScale+ MPSoC ZCU102



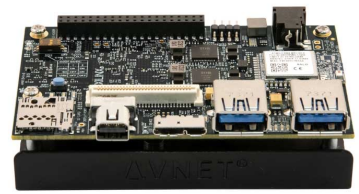
Learn More

Zynq UltraScale+ MPSoC ZCU104



Learn More

Avnet Ultra96-V2



Learn More

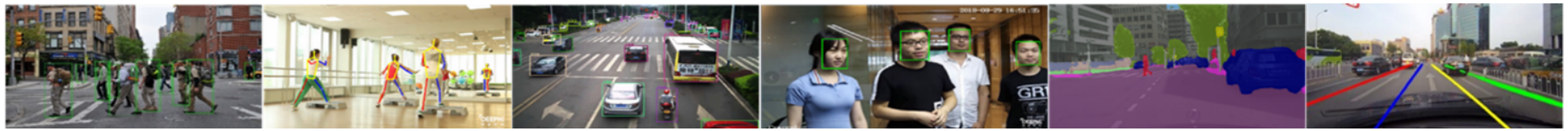
You Can Also Create Vitis Target Platforms for Your Custom Boards

Vitis AI: Deep Learning Acceleration

Frameworks

TensorFlow Caffe PyTorch

Vitis AI models



Vitis AI development kit

AI Optimizer | AI Quantizer | AI Compiler | AI Profiler | AI Library

Xilinx runtime library (XRT)

Deep Learning Processing Unit (DPU)

CNN DPU | LSTM DPU | MLP DPU

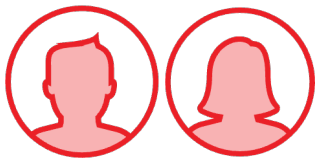
Edge Deployment

On-Premise Deployment

Cloud Deployment

Department of Electrical Engineering
CityU 香港城市大學 City University of Hong Kong

SDSoC, SDAccel and SDK Migration for Developers



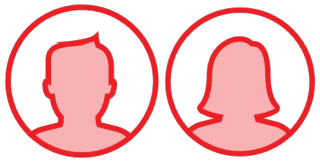
SDAccel™ Environment





XILINX VITIS™

Fundamental User-Flow Remains Same



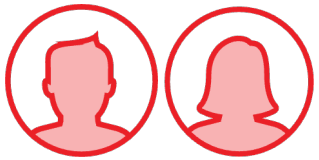
Xilinx SDK





XILINX VITIS™

Minor Changes to User-Flow



SDSoC™ Environment





XILINX VITIS™

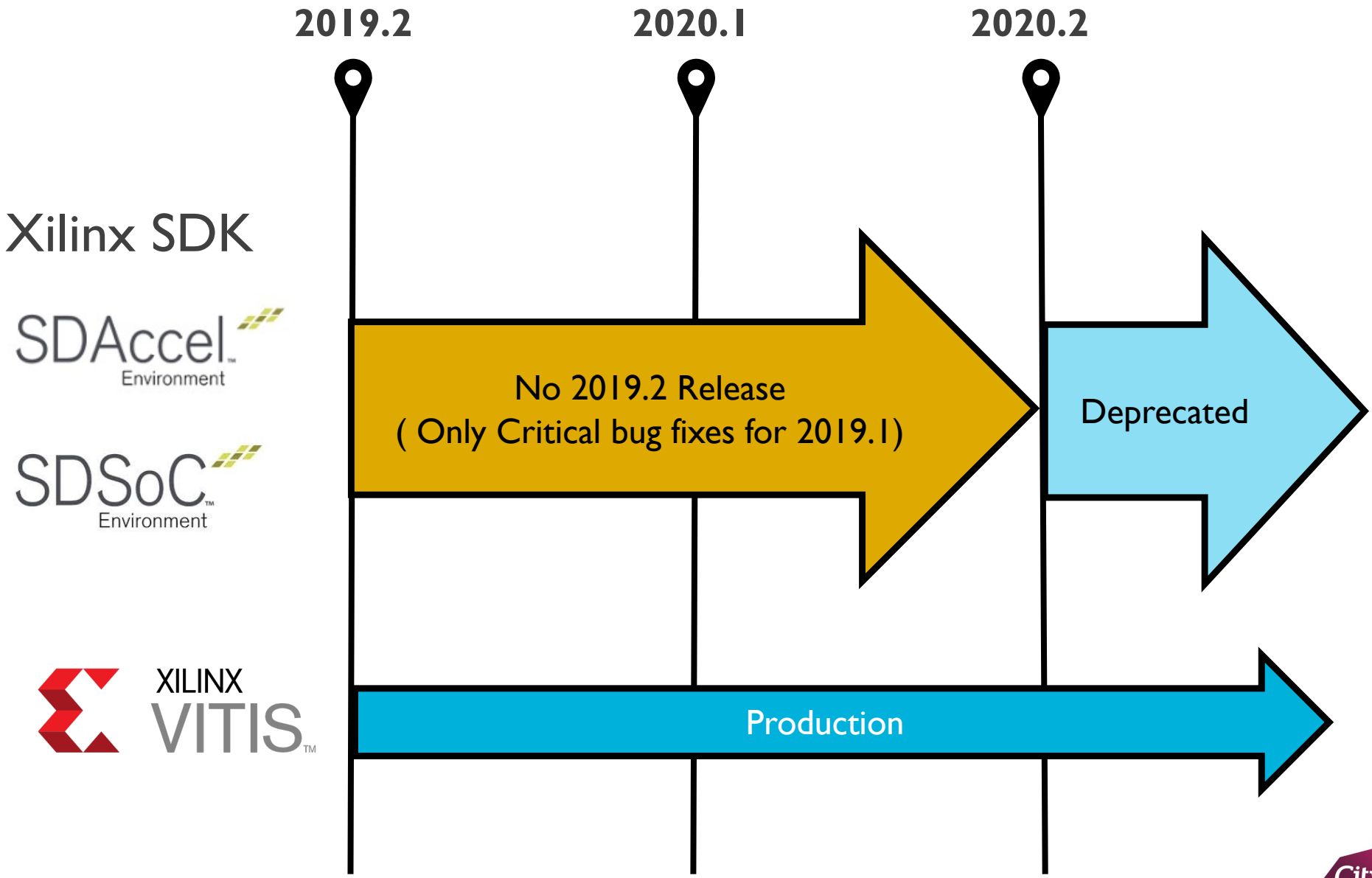
Significant Changes to User Paradigm

(Software & Accelerator Design Decoupled)

Migration Guides & Examples Available to Help Migration to Vitis Unified Software Platform

CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

SDK, SDSoC and SDAccel Releases and Support



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Overview

- FPGA Overview
- FPGA + ARM Processor
  - FPGA Electronic Design Automation Platform – Vivado & Vitis AI
  - Multi-processor System-on-Chip (MPSoC)
  - Building Blocks of a Generic Microcontroller
  - PicoBlaze vs. MicroBlaze
- Zynq SoC (AP SoC)
- Zynq SoC Processing System (PS)
- Processor Peripherals
- Clock, Reset, and Debug Features
- AXI Interfaces
- Summary

Building Blocks of a Generic Microcontroller

- There are several microcontroller families developed by different vendors.
- Although these have different properties, they share similar building blocks.

Central Processing Unit

- Central processing unit (CPU) is a sequential circuit in its basic sense. It is responsible for executing commands given to it in the form of instructions.
- Therefore, CPU is the fundamental block responsible for working of a microcontroller.

Arithmetic Logic Unit

- Arithmetic logic unit (ALU) is a sub-part of CPU responsible for executing arithmetic and logic operations.
- ALU is basically composed of combinational circuits.
- Depending on the microcontroller type, ALU can perform addition, subtraction, multiplication, and division operations.

Building Blocks of a Generic Microcontroller

Memory

- A microcontroller needs memory for two reasons.
- First, instructions to be executed by the CPU should be kept somewhere. Program memory (ROM) is the place for this operation.
- Second, some instructions to be executed will work on data which need to be stored in memory. Data memory (RAM) will be the block for this operation.
- A microcontroller should have ROM and RAM blocks.

Oscillator/Clock

- Being a sequential device, microcontroller needs a clock signal to operate.
- A clock is generated either by an external source or internal oscillator in the microcontroller.
- Initial microcontrollers had just one clock source to operate.
- Recent microcontrollers have more than one clock source such that each can be used by a different block in the microcontroller.

Building Blocks of a Generic Microcontroller

General Purpose Input/Output

- A microcontroller interacts with the outside world through its input and output pins.
- These are called general purpose input and output (GPIO).
- Most of the times, GPIO pins operate with digital data. These pins may be of use for other applications as well such as digital communication and analog to digital conversion.

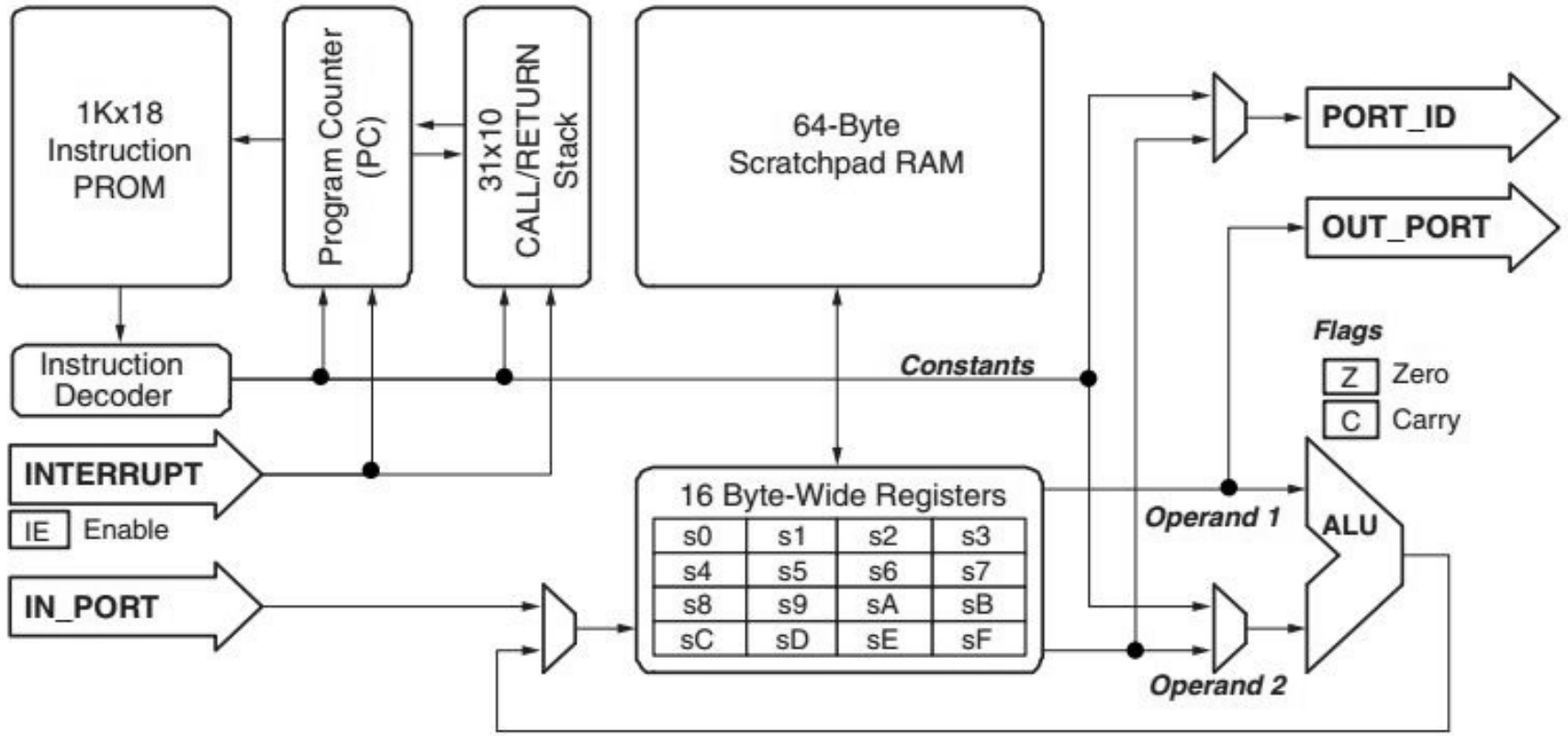
Other Blocks

- A microcontroller may also have other blocks generally called as peripherals.
- Digital communication, analog to digital converter (ADC), and digital to analog converter (DAC) can be counted as such blocks.

Xilinx PicoBlaze Microcontroller

- PicoBlaze is an eight-bit soft-core microcontroller developed by Xilinx.
- For example, we can program it on the Xilinx Artix-7 FPGAs.

Functional Blocks of PicoBlaze

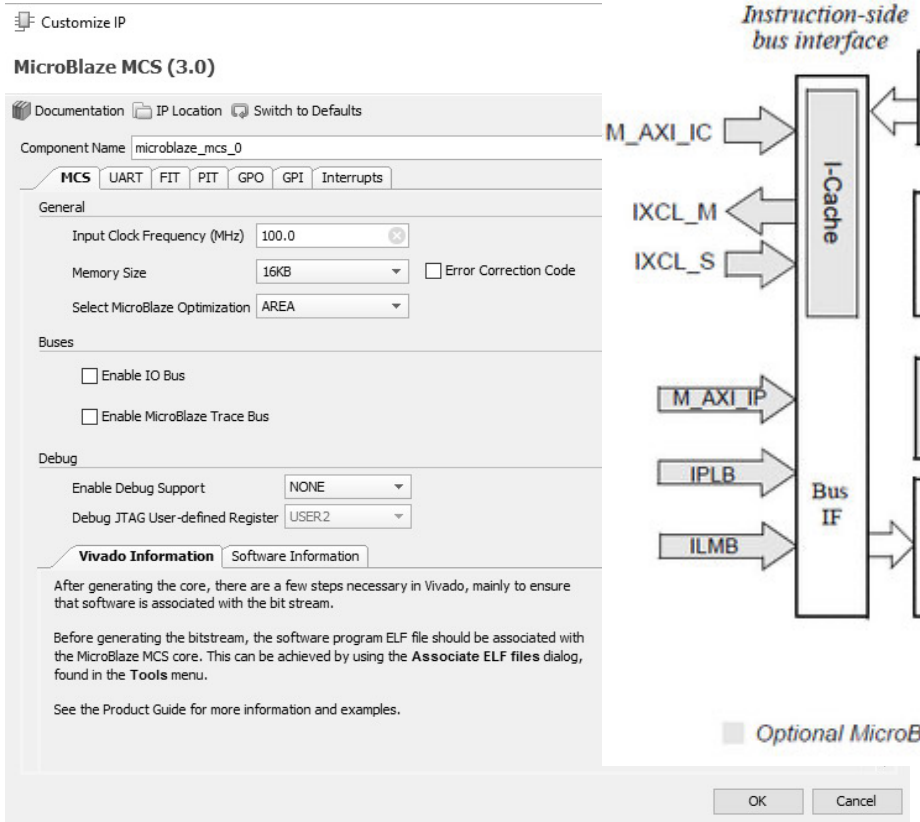


CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

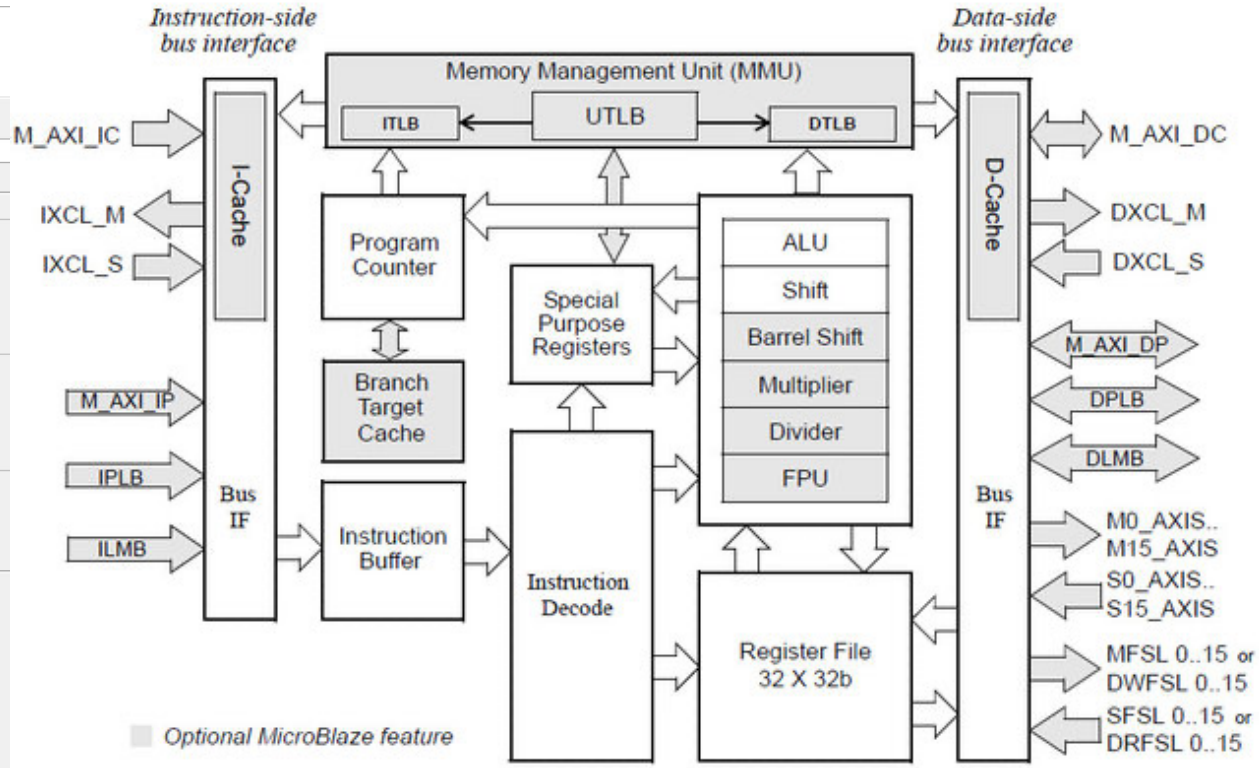
Xilinx MicroBlaze Microcontroller

- MicroBlaze is a 32-bit soft-core microcontroller developed by Xilinx.
- It has a fairly complex architecture compared to PicoBlaze.

MicroBlaze as an IP Block



Functional Blocks of MicroBlaze



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Objectives

- Identify the basic building blocks of the Zynq™ architecture processing system (PS)
- Describe the ARM Cortex-A9 processor memory space
- Understand how to connect PS to the programmable logic (PL) through the AXI ports
- Name the five AXI channels
- Describe the operation of the AXI streaming protocol

Outline

- **Zynq SoC (AP SoC)**
- Zynq SoC Processing System (PS)
- Processor Peripherals
- Clock, Reset, and Debug Features
- AXI Interfaces
- Summary

The PS and the PL

- The Zynq-7000 SoC architecture consists of two major sections
  - **PS: Processing system**
  - Dual ARM Cortex-A9 processor based
  - Single core versions also now available
  - Multiple peripherals
  - Hard silicon core
  - PL: Programmable logic
  - Shares the same 7 series programmable logic as
  - Artix™-based devices: Z-7010, Z-7015, and Z-7020 (high-range I/O banks only)
  - Kintex™-based devices: Z-7030, Z-7035, Z-7045, and Z-7100 (mix of high-range and high-performance I/O banks)

Zynq-7000 Family Highlights

- Complete ARM®-based processing system
  - Application Processor Unit (APU)
  - Dual ARM Cortex™-A9 processor
  - Caches and support blocks
  - Fully integrated memory controllers
  - I/O peripherals
- Tightly integrated programmable logic
  - Used to extend the processing system
  - Scalable density and performance
- Flexible array of I/O
  - Wide range of external multi-standard I/O
  - High-performance integrated serial transceivers
  - Analog-to-digital converter inputs

PS Components

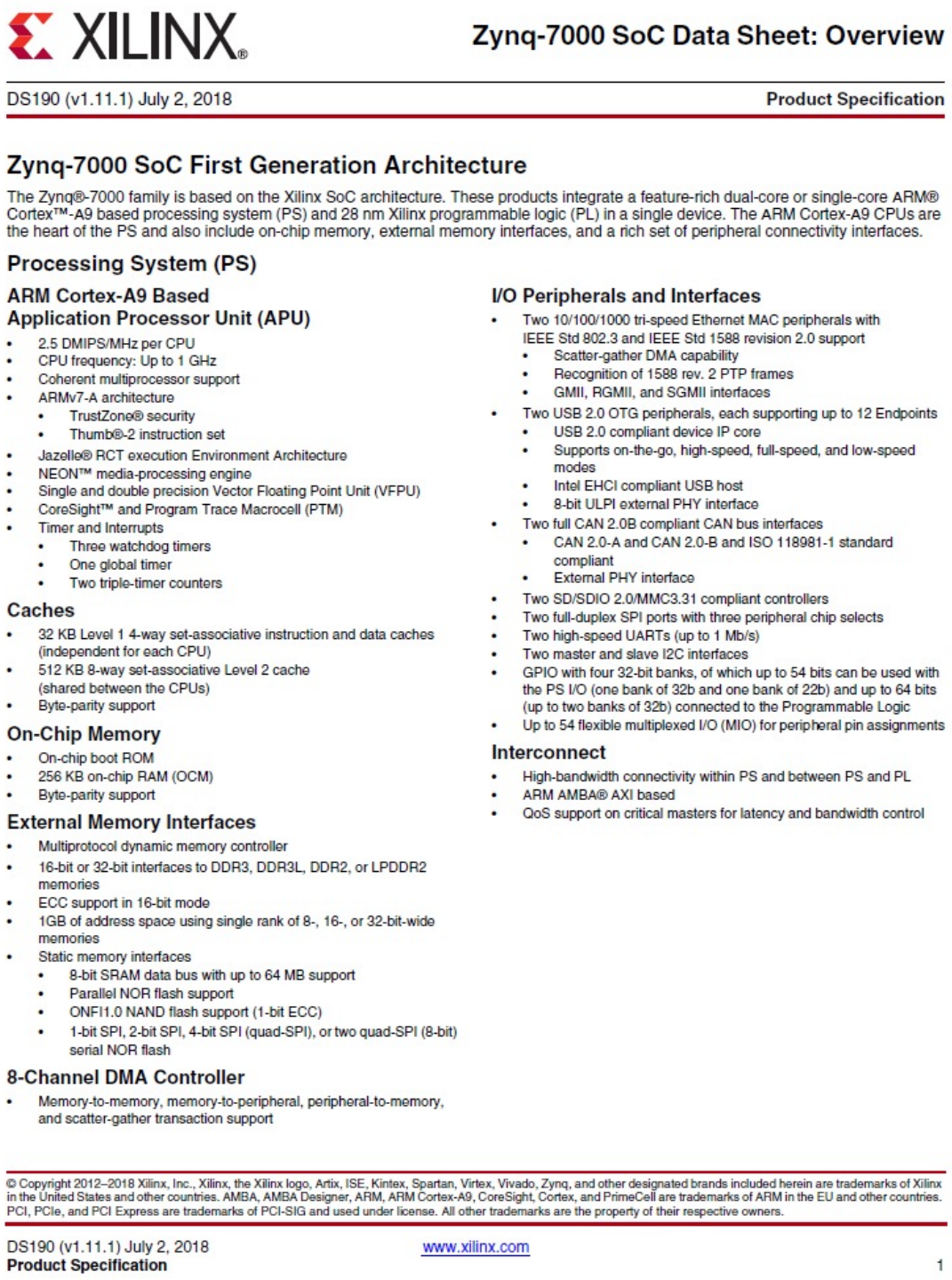
- Application processing unit (APU)
- I/O peripherals (IOP)
  - Multiplexed I/O (MIO), extended multiplexed I/O (EMIO)
- Memory interfaces
- PS interconnect
- DMA
- Timers
  - Public and private
- General interrupt controller (GIC)
- On-chip memory (OCM): RAM
- Debug controller: CoreSight

Outline

- Zynq SoC (AP SoC)
- **Zynq SoC Processing System (PS)**
- Processor Peripherals
- Clock, Reset, and Debug Features
- AXI Interfaces
- Summary

FPGA Data Sheet

- It is important for us to learn how to read this kind of datasheet as a professional hardware designer.



XILINX®

Zynq-7000 SoC Data Sheet: Overview

DS190 (v1.11.1) July 2, 2018 **Product Specification**

Zynq-7000 SoC First Generation Architecture

The Zynq®-7000 family is based on the Xilinx SoC architecture. These products integrate a feature-rich dual-core or single-core ARM® Cortex™-A9 based processing system (PS) and 28 nm Xilinx programmable logic (PL) in a single device. The ARM Cortex-A9 CPUs are the heart of the PS and also include on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces.

Processing System (PS)

ARM Cortex-A9 Based Application Processor Unit (APU)

- 2.5 DMIPS/MHz per CPU
- CPU frequency: Up to 1 GHz
- Coherent multiprocessor support
- ARMv7-A architecture
  - TrustZone® security
  - Thumb®-2 instruction set
- Jazelle® RCT execution Environment Architecture
- NEON™ media-processing engine
- Single and double precision Vector Floating Point Unit (VFPU)
- CoreSight™ and Program Trace Macrocell (PTM)
- Timer and Interrupts
  - Three watchdog timers
  - One global timer
  - Two triple-timer counters

Caches

- 32 KB Level 1 4-way set-associative instruction and data caches (independent for each CPU)
- 512 KB 8-way set-associative Level 2 cache (shared between the CPUs)
- Byte-parity support

On-Chip Memory

- On-chip boot ROM
- 256 KB on-chip RAM (OCM)
- Byte-parity support

External Memory Interfaces

- Multiprotocol dynamic memory controller
- 16-bit or 32-bit interfaces to DDR3, DDR3L, DDR2, or LPDDR2 memories
- ECC support in 16-bit mode
- 1GB of address space using single rank of 8-, 16-, or 32-bit-wide memories
- Static memory interfaces
  - 8-bit SRAM data bus with up to 64 MB support
  - Parallel NOR flash support
  - ONFI1.0 NAND flash support (1-bit ECC)
  - 1-bit SPI, 2-bit SPI, 4-bit SPI (quad-SPI), or two quad-SPI (8-bit) serial NOR flash

8-Channel DMA Controller

- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and scatter-gather transaction support

I/O Peripherals and Interfaces

- Two 10/100/1000 tri-speed Ethernet MAC peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
  - Scatter-gather DMA capability
  - Recognition of 1588 rev. 2 PTP frames
  - GMII, RGMII, and SGMII interfaces
- Two USB 2.0 OTG peripherals, each supporting up to 12 Endpoints
  - USB 2.0 compliant device IP core
  - Supports on-the-go, high-speed, full-speed, and low-speed modes
  - Intel EHCI compliant USB host
  - 8-bit ULPI external PHY interface
- Two full CAN 2.0B compliant CAN bus interfaces
  - CAN 2.0-A and CAN 2.0-B and ISO 118981-1 standard compliant
  - External PHY interface
- Two SD/SDIO 2.0/MMC3.31 compliant controllers
- Two full-duplex SPI ports with three peripheral chip selects
- Two high-speed UARTs (up to 1 Mb/s)
- Two master and slave I2C interfaces
- GPIO with four 32-bit banks, of which up to 54 bits can be used with the PS I/O (one bank of 32b and one bank of 22b) and up to 64 bits (up to two banks of 32b) connected to the Programmable Logic
- Up to 54 flexible multiplexed I/O (MIO) for peripheral pin assignments

Interconnect

- High-bandwidth connectivity within PS and between PS and PL
- ARM AMBA® AXI based
- QoS support on critical masters for latency and bandwidth control

© Copyright 2012–2018 Xilinx, Inc., Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. AMBA, AMBA Designer, ARM, ARM Cortex-A9, CoreSight, Cortex, and PrimeCell are trademarks of ARM in the EU and other countries. PCI, PCIe, and PCI Express are trademarks of PCI-SIG and used under license. All other trademarks are the property of their respective owners.

Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Overview of the Zynq Chip

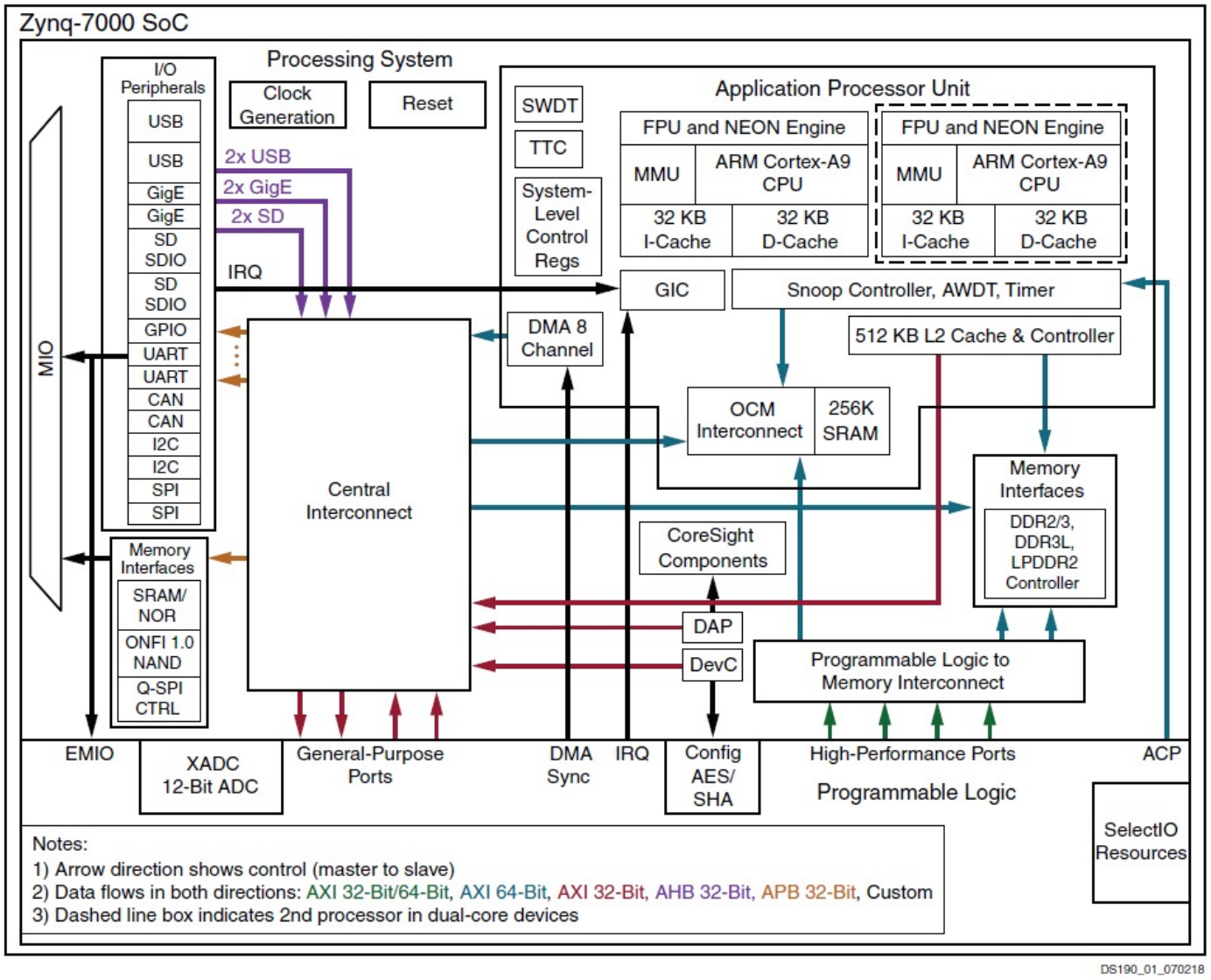


Figure 1: **Architectural Overview**

CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

ARM Processor Architecture

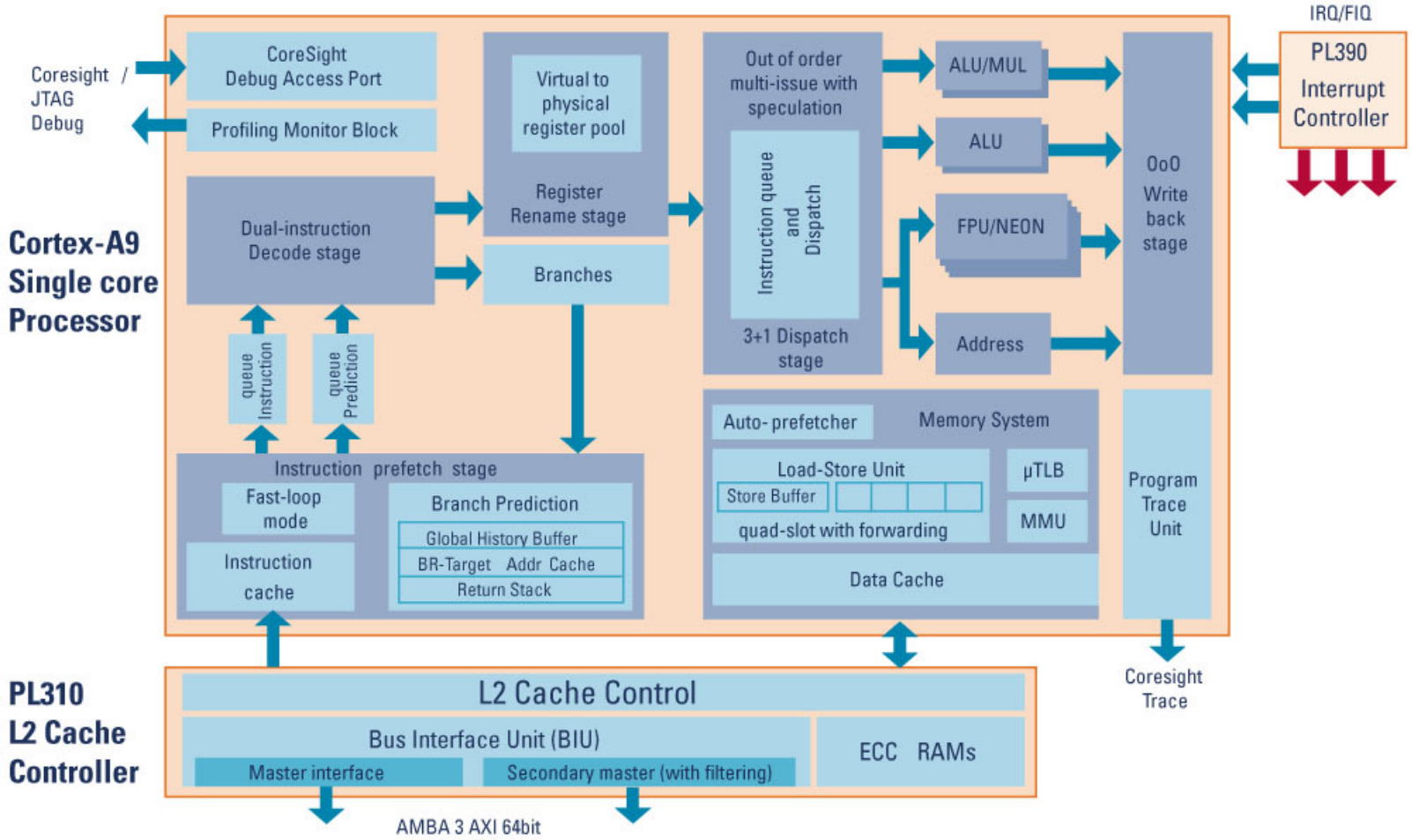
- ARM Cortex-A9 processor implements the ARMv7-A architecture
  - ARMv7 is the ARM Instruction Set Architecture (ISA)
  - ARMv7-A: Application set that includes support for a Memory Management Unit (MMU)
  - ARMv7-R: Real-time set that includes support for a Memory Protection Unit (MPU)
  - ARMv7-M: Microcontroller set that is the smallest set
- The ARMv7 ISA includes the following types of instructions (for backwards compatibility)
  - Thumb instructions: 16 bits; Thumb-2 instructions: 32 bits
  - NEON: ARM's Single Instruction Multiple Data (SIMD) instructions
- ARM Advanced Microcontroller Bus Architecture (AMBA®) protocol
  - AXI3: Third-generation ARM interface
  - AXI4: Adding to the existing AXI definition (extended bursts, subsets)
- Cortex is the new family of processors
  - ARM family is older generation; Cortex is current; MMUs in Cortex processors and MPUs in ARM

ARM Cortex-A9 Processor Power

- Dual-core processor cluster
- 2.5 DMIP/MHz per processor
- Harvard architecture
- Self-contained 32KB L1 caches for instructions and data
- External memory based 512KB L2 cache
- Automatic cache coherency between processor cores
- 1GHz operation (fastest speed grade)

ARM Cortex-A9 Processor Micro-Architecture

- Instruction pipeline supports out-of-order instruction issue and completion
- Register renaming to enable execution speculation
- Non-blocking memory system with load-store forwarding
- Fast loop mode in instruction pre-fetch to lower power consumption



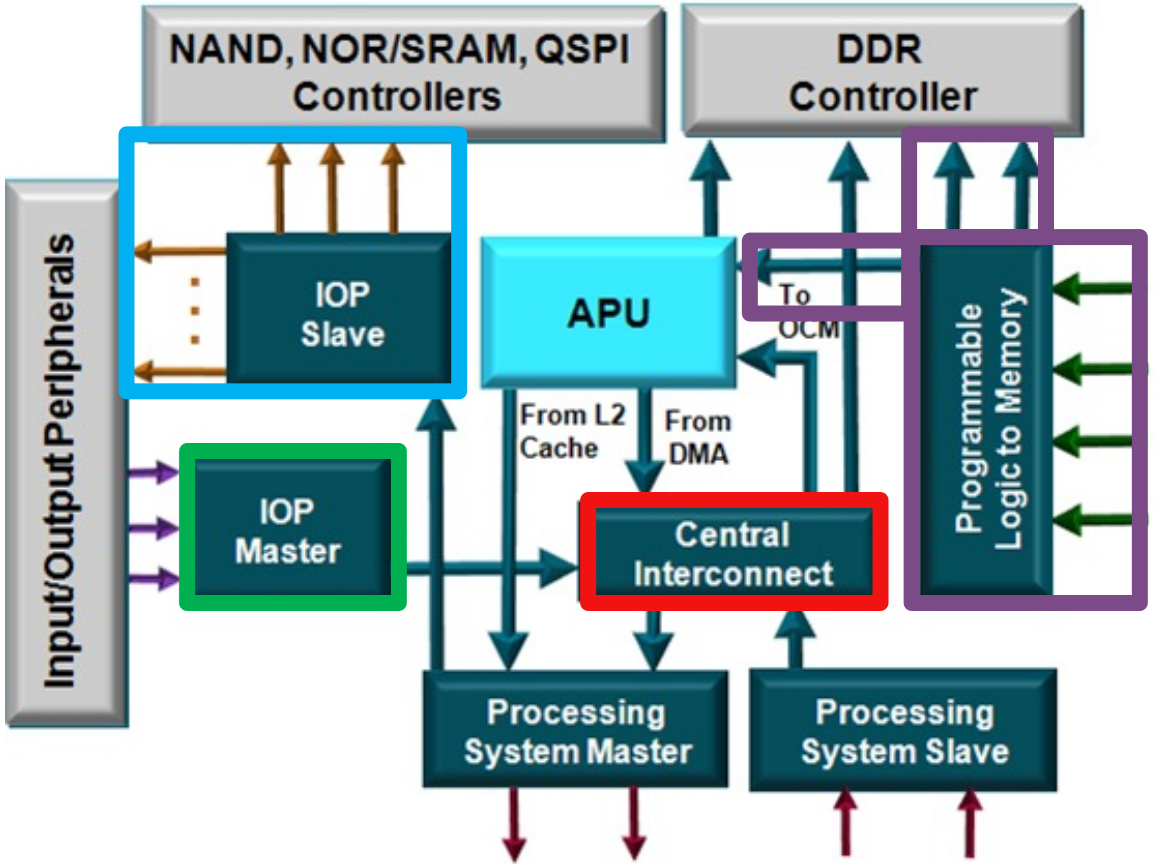
CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

ARM Cortex-A9 Processor Micro-Architecture

- Variable length, out-of-order, eight-stage, super-scalar instruction pipeline
  - Advanced pre-fetch with parallel branch pipeline enabling early branch prediction and resolution
  - Multi-issued into
  - Primary data processing pipeline
  - Secondary full data processing pipeline
  - Load-store pipeline
  - Compute engine (FPU/NEON) pipeline
- Speculative execution
  - Supports virtual renaming of ARM physical registers to remove pipeline stalls due to data dependencies
  - Increased processor utilization and hiding of memory latencies
  - Increased performance by hardware unrolling of code loops
  - Reduced interrupt latency via speculative entry to Interrupt Service Routine (ISR)

Processing System Interconnect

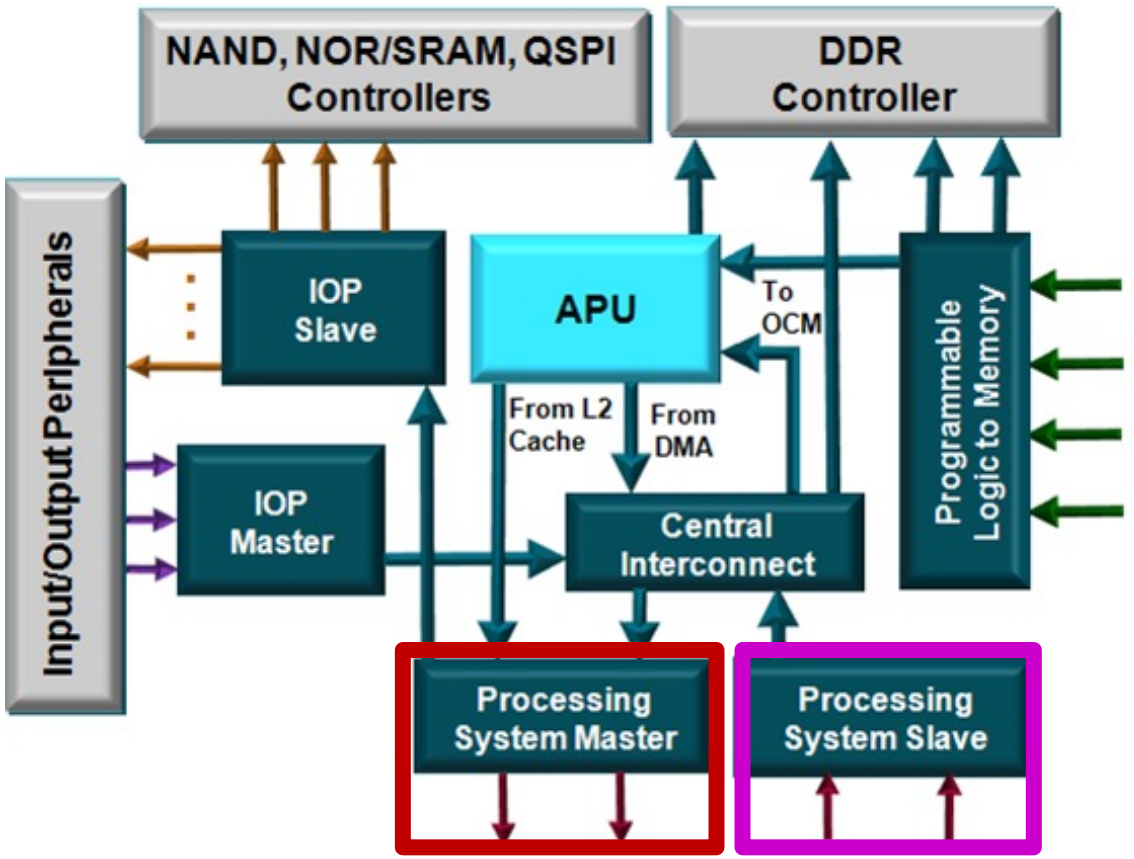
- Programmable logic to memory
  - Two ports to DDR
  - One port to OCM SRAM
- Central interconnect
  - Enables other interconnects to communicate
- Peripheral master
  - USB, GigE, SDIO connects to DDR and PL via the central interconnect
- Peripheral slave
  - CPU, DMA, and PL access to IOP peripherals



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Processing System Interconnect

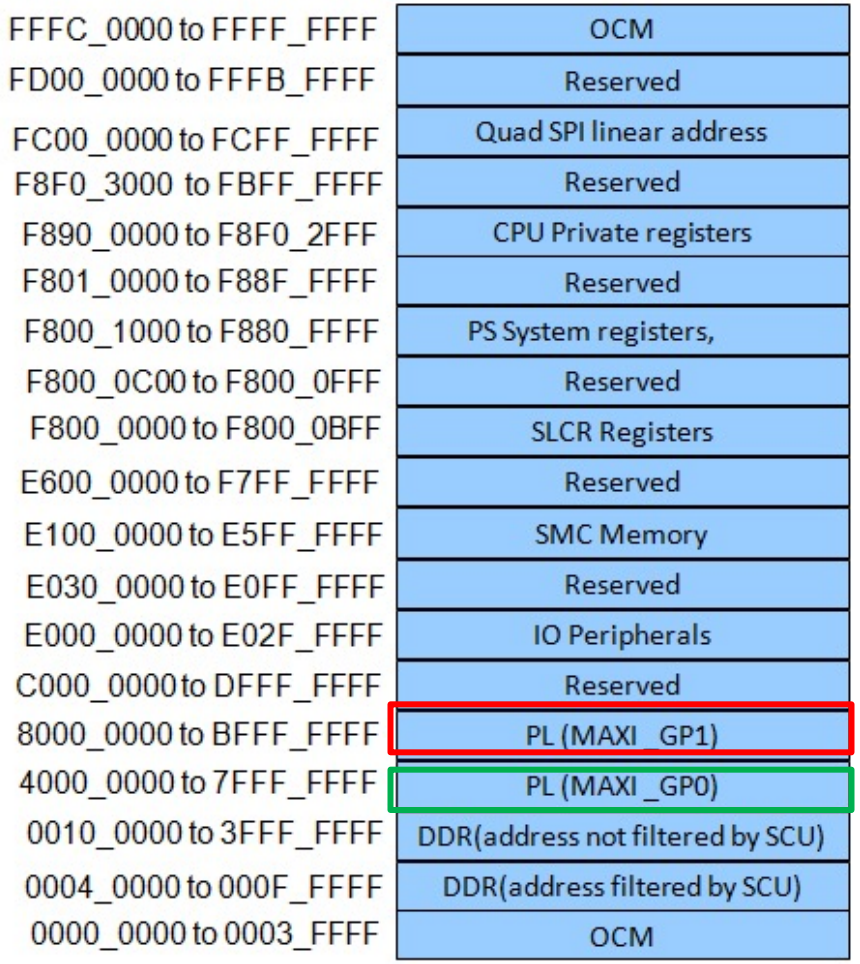
- Processing system master
  - Two ports from the processing system to programmable logic
  - Connects the CPU block to common peripherals through the central interconnect
- Processing system slave
  - Two ports from programmable logic to the processing system



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Memory Map

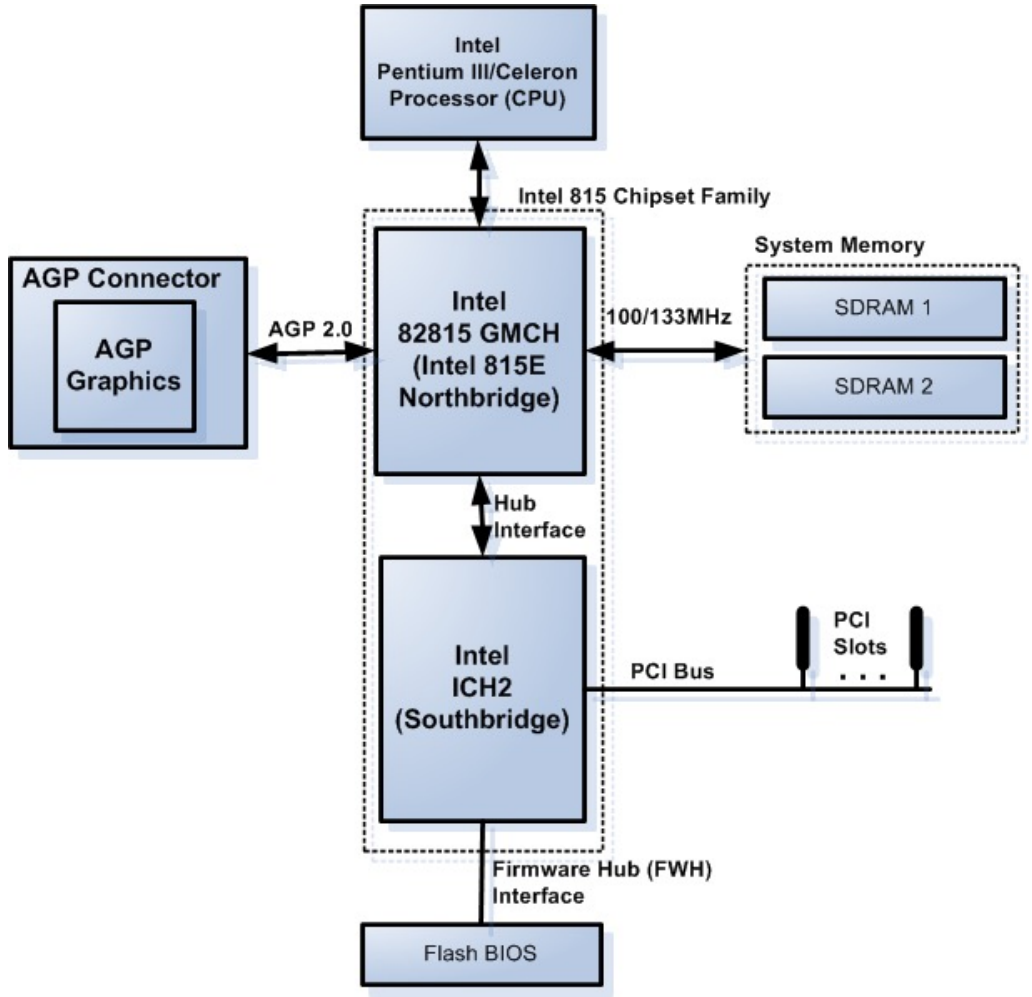
- The Cortex-A9 processor uses 32-bit addressing
- PS peripherals and PL AXI slave interfaces are memory mapped to the Cortex-A9 processor cores
- All AXI slave PL peripherals will be located between
  4000_0000 and 7FFF_FFFF (connected to GP0)
  and
  8000_0000 and BFFF_FFFF (connected to GP1)



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

System Address Map - Intro

- If we want to access a device outside the CPU, we need to pass through this Bridge chipset.
- Address point of view – serve as an address mapping router.



CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Zynq SoC Memory Resources

- On-chip memory (OCM)
  - RAM
  - Boot ROM
- DDRx dynamic memory controller
  - Supports LPDDR2, DDR2, DDR3
- Flash/static, memory controller
  - Supports SRAM, QSPI, NAND/NOR FLASH

PS Boots First

- CPU0 boots from OCM ROM; CPU1 goes into a sleep state
- On-chip boot loader in OCM ROM (Stage 0 boot)
- Processor loads First Stage Boot Loader (FSBL) from external flash memory
  - NOR
  - NAND
  - Quad-SPI
  - SD Card
  - Load from JTAG; not a memory device—used for development/debug only
- Boot source selected via package bootstrapping pins
- Optional secure boot mode allows the loading of encrypted software from the flash boot memory

CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Configuring the PL

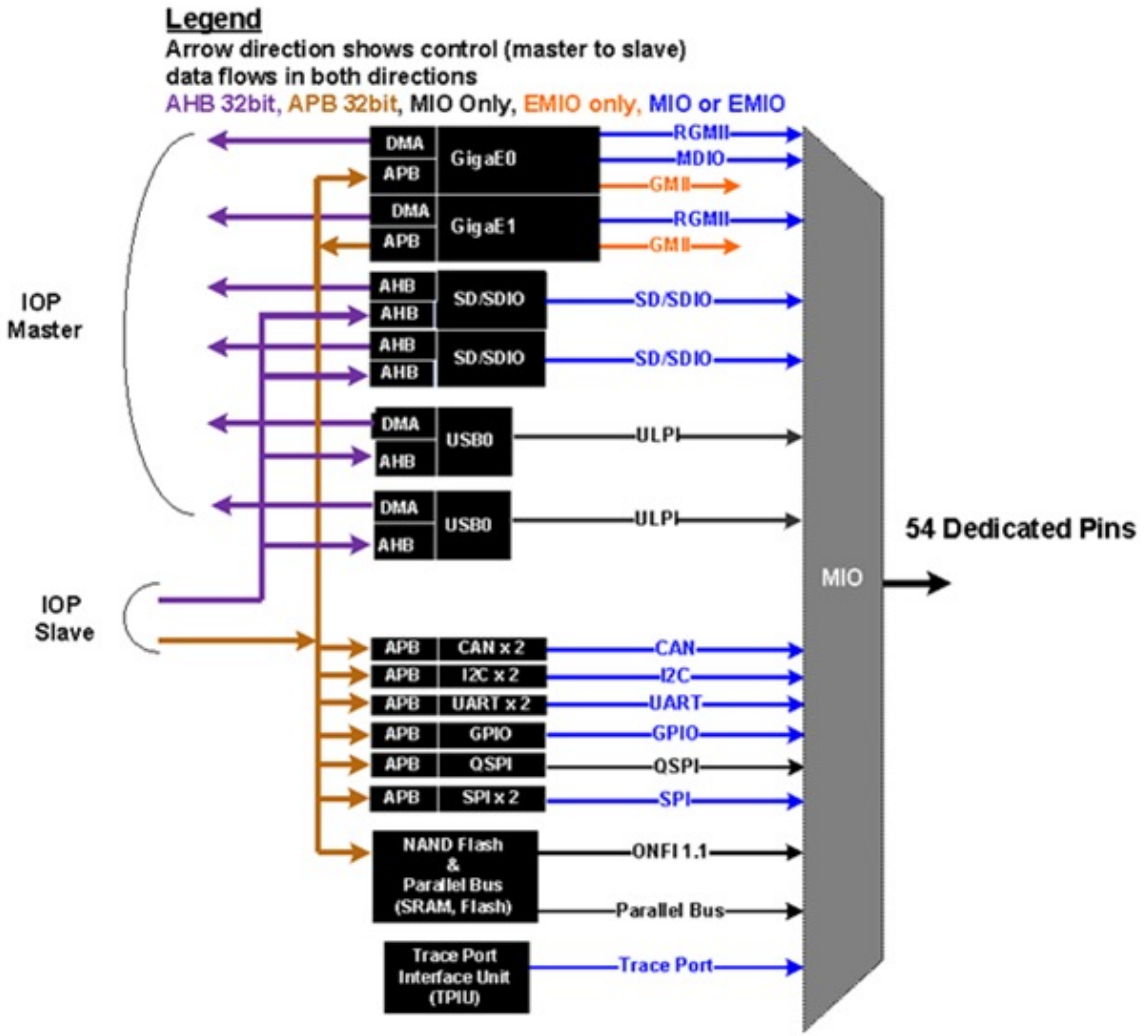
- The programmable logic is configured after the PS boots
- Performed by application software accessing the hardware device configuration unit
  - Bitstream image transferred
  - 100-MHz, 32-bit PCAP stream interface
  - Decryption/authentication hardware option for encrypted bitstreams
  - In secure boot mode, this option can be used for software memory load
  - Built-in DMA allows simultaneous PL configuration and OS memory loading

Outline

- Zynq SoC (AP SoC)
- Zynq SoC Processing System (PS)
- **Processor Peripherals**
- Clock, Reset, and Debug Features
- AXI Interfaces
- Summary

Input/Output Peripherals

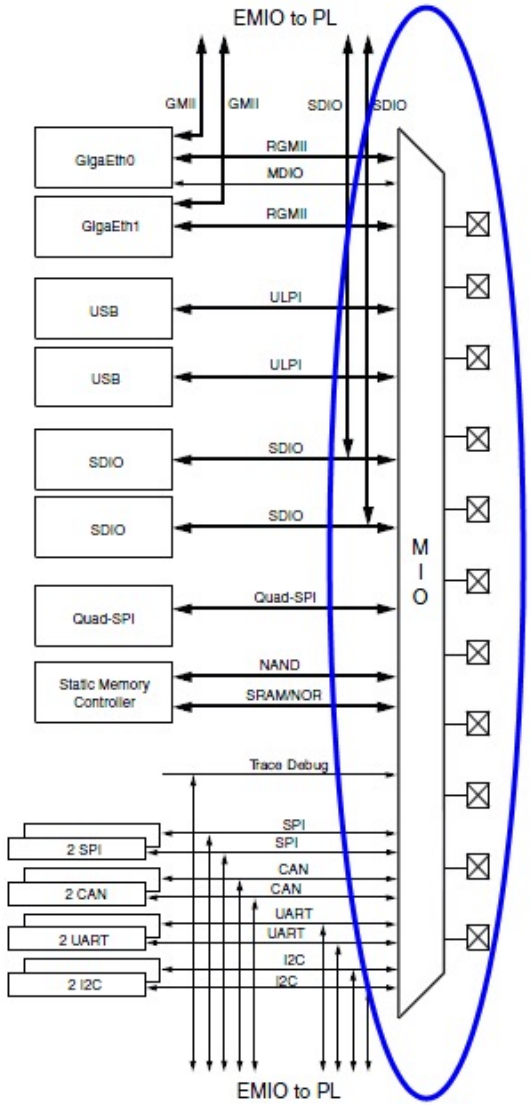
- Two GigE
- Two USB
- Two SPI
- Two SD/SDIO
- Two CAN
- Two I2C
- Two UART
- Four 32-bit GPIOs
- Static memories
  - NAND, NOR/SRAM, Quad SPI
- Trace ports



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Multiplexed I/O (MIO)

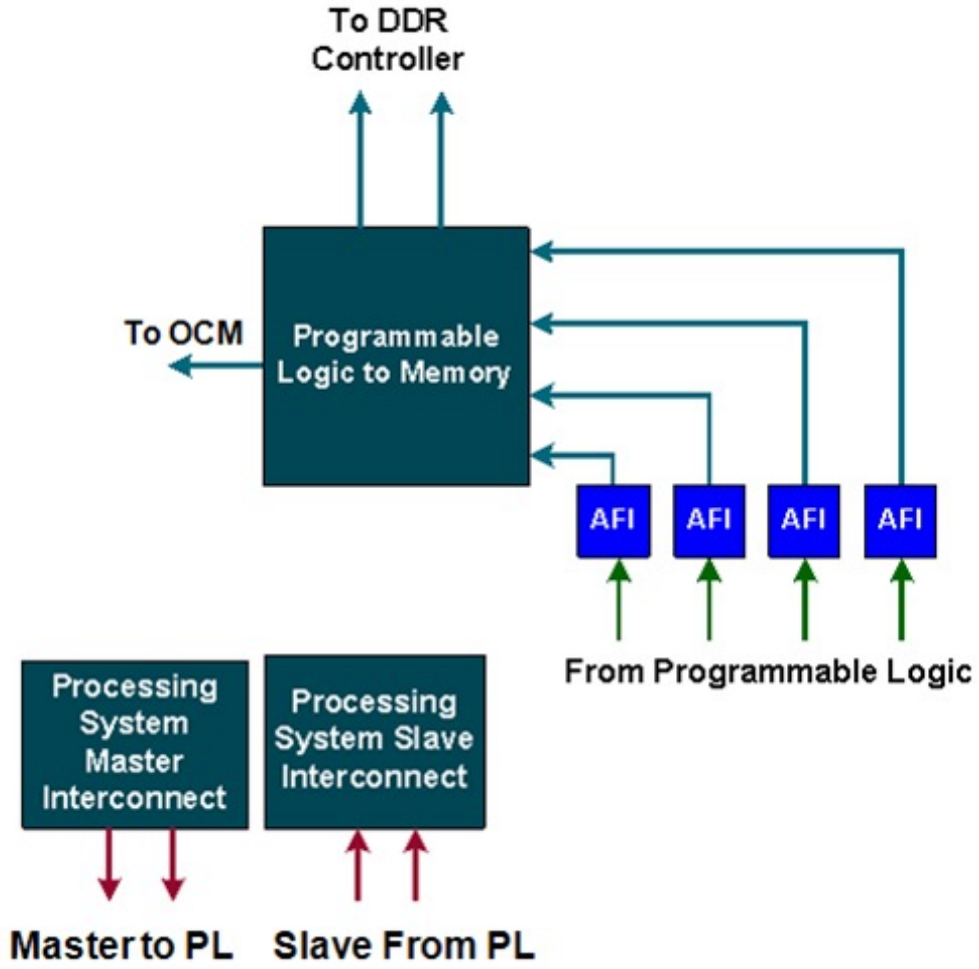
- External interface to PS I/O peripheral ports
  - 54 dedicated package pins available
  - Software configurable
  - Automatically added to bootloader by tools
  - Not available for all peripheral ports
  - Some ports can only use EMIO



CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

PS-PL Interfaces

- AXI high-performance slave ports (HP0-HP3)
  - Configurable 32-bit or 64-bit data width
  - Access to OCM and DDR only
  - Conversion to processing system clock domain
  - AXI FIFO Interface (AFI) are FIFOs (1KB) to smooth
    large data transfers
- AXI general-purpose ports (GP0-GP1)
  - Two masters from PS to PL
  - Two slaves from PL to PS
  - 32-bit data width
  - Conversation and sync to processing system clock domain



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

From PL to PS Sub-system

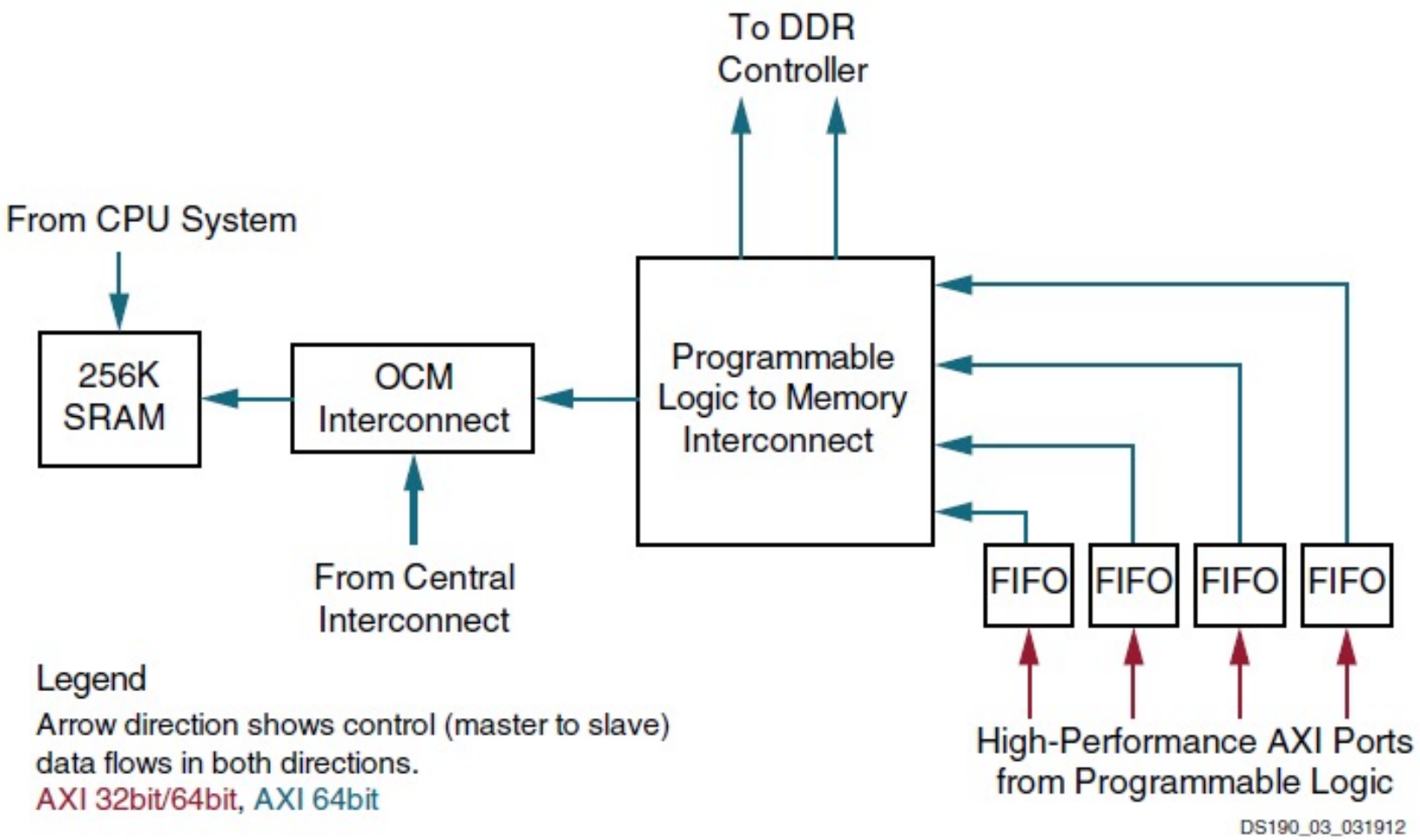


Figure 3: **PL Interface to PS Memory Subsystem**

CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

PS-PL Interfaces

- One 64-bit accelerator coherence port (ACP) AXI slave interface to CPU memory
- DMA, interrupts, events signals
  - Processor event bus for signaling event information to the CPU
  - PL peripheral IP interrupts to the PS general interrupt controller (GIC)
  - Four DMA channel RDY/ACK signals
- Extended multiplexed I/O (EMIO) allows PS peripheral ports access to PL logic and device I/O pins
- Clock and resets
  - Four PS clock outputs to the PL with enable control
  - Four PS reset outputs to the PL
- Configuration and miscellaneous

Outline

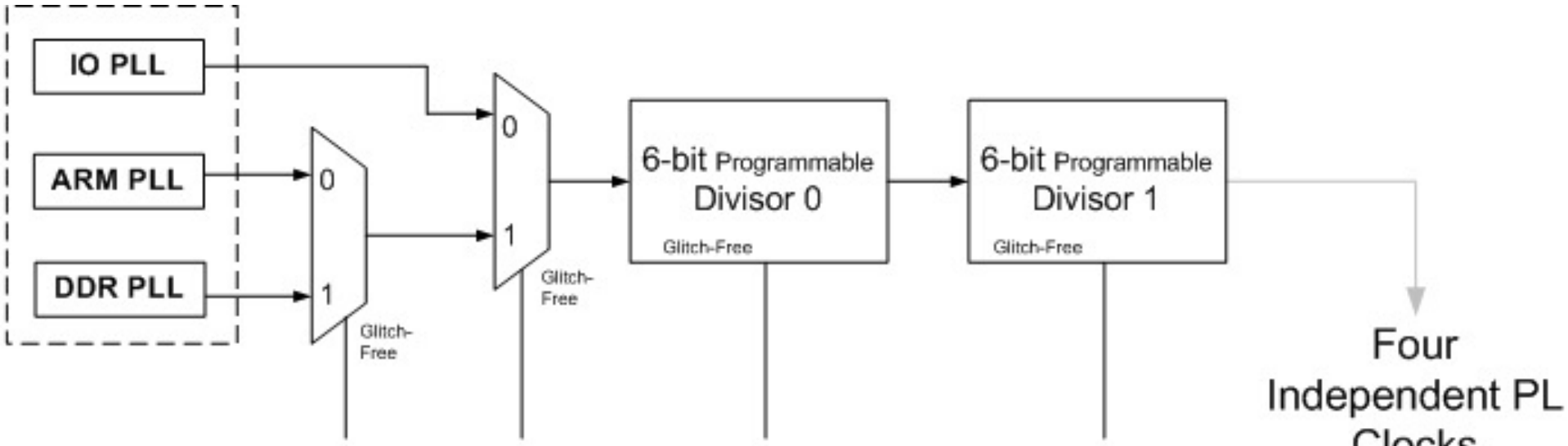
- Zynq SoC (AP SoC)
- Zynq SoC Processing System (PS)
- Processor Peripherals
- **Clock, Reset, and Debug Features**
- AXI Interfaces
- Summary

CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

PL Clocking Sources

- PS clocks
  - PS clock source from external package pin
  - PS has three PLLs for clock generation
  - PS has four clock ports to PL
- The PL has 7 series clocking resources
  - PL has a different clock source domain compared to the PS
  - The clock to PL can be sourced from external clock capable pins
  - Can use one of the four PS clocks as source
- Synchronizing the clock between PL and PS is taken care of by the architecture of the PS
- PL cannot supply clock source to PS

Clocking the PL

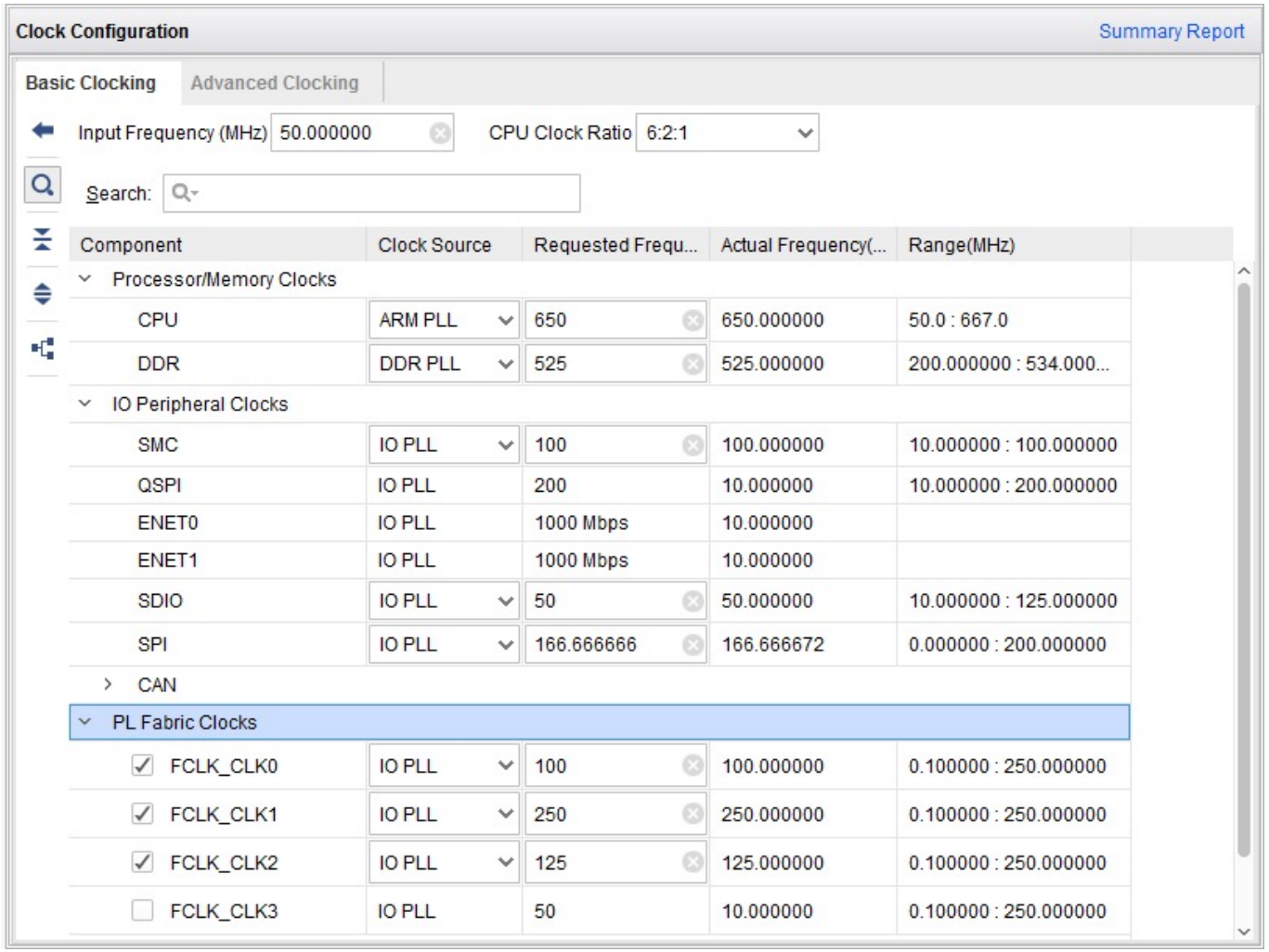


PL Fabric Clock	Control Register	Mux Ctrl Field	Mux Ctrl Field	Divider 0 Ctrl Field	Divider 1 Ctrl Field	
PL Fabric 0	FPGA0_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	→ FCLKCLK0
PL Fabric 1	FPGA1_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	→ FCLKCLK1
PL Fabric 2	FPGA2_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	→ FCLKCLK2
PL Fabric 3	FPGA3_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	→ FCLKCLK3

CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Clock Generation (Using Zynq Tab)

- The Clock Generator allows configuration of PLL components for both the PS and PL
  - One input reference clock
- Access GUI by clicking the Clock Generation Block, or select from Navigator
- Configure the PS Peripheral Clock in the Zynq tab
  - PS uses a dedicated PLL clock
  - PS I/O peripherals use the I/O PLL clock and ARM PLL

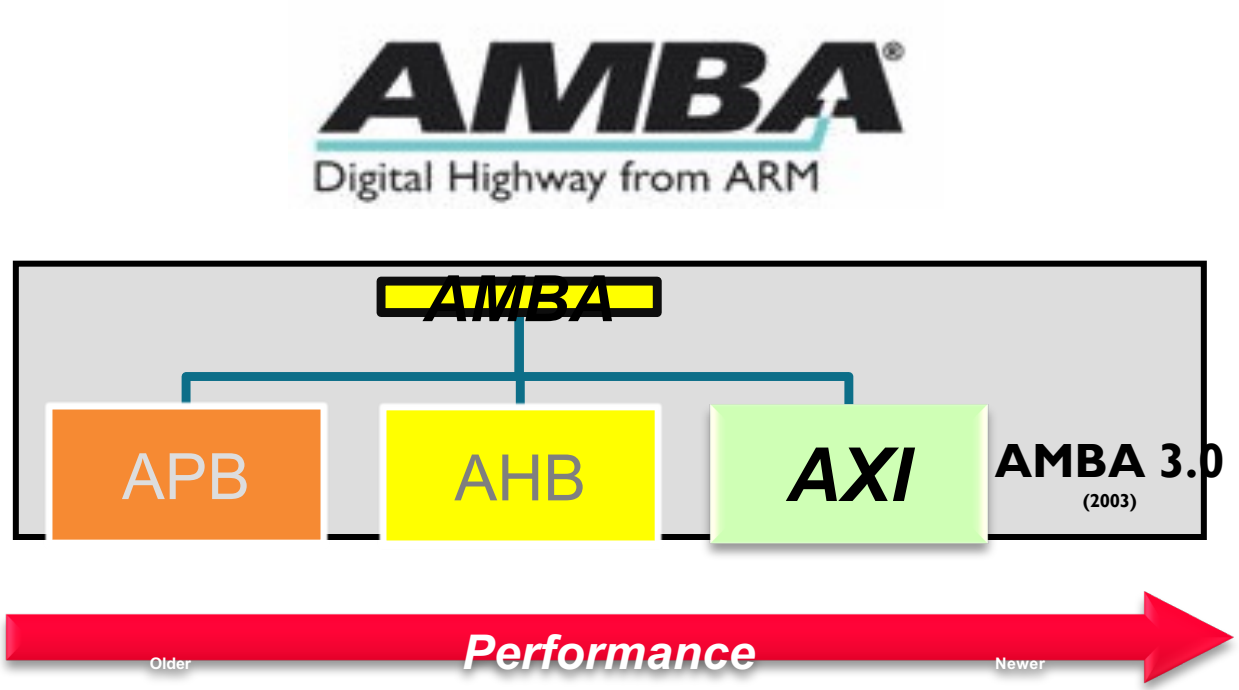


CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Zynq Resets

- Internal resets
  - Power-on reset (POR)
  - Watchdog resets from the three watchdog timers
  - Secure violation reset
- PS resets
  - External reset: PS_SRST_B
  - Warm reset: SRSTB
- PL resets
  - Four reset outputs from PS to PL
  - FCLK_RESET[3:0]

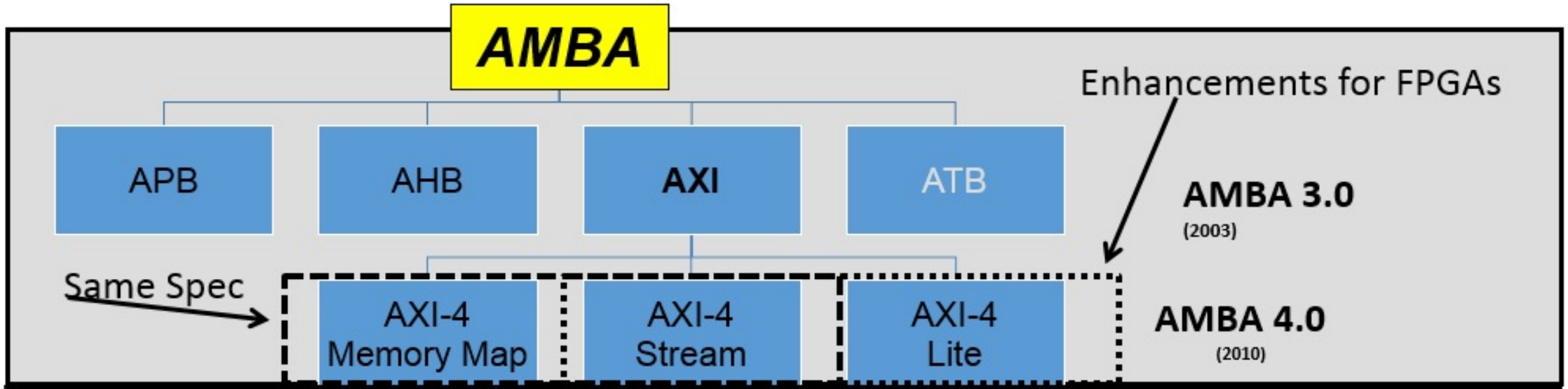
AXI is Part of ARM's AMBA



AMBA: Advanced Microcontroller Bus Architecture
AXI: Advanced Extensible Interface

CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

AXI is Part of AMBA

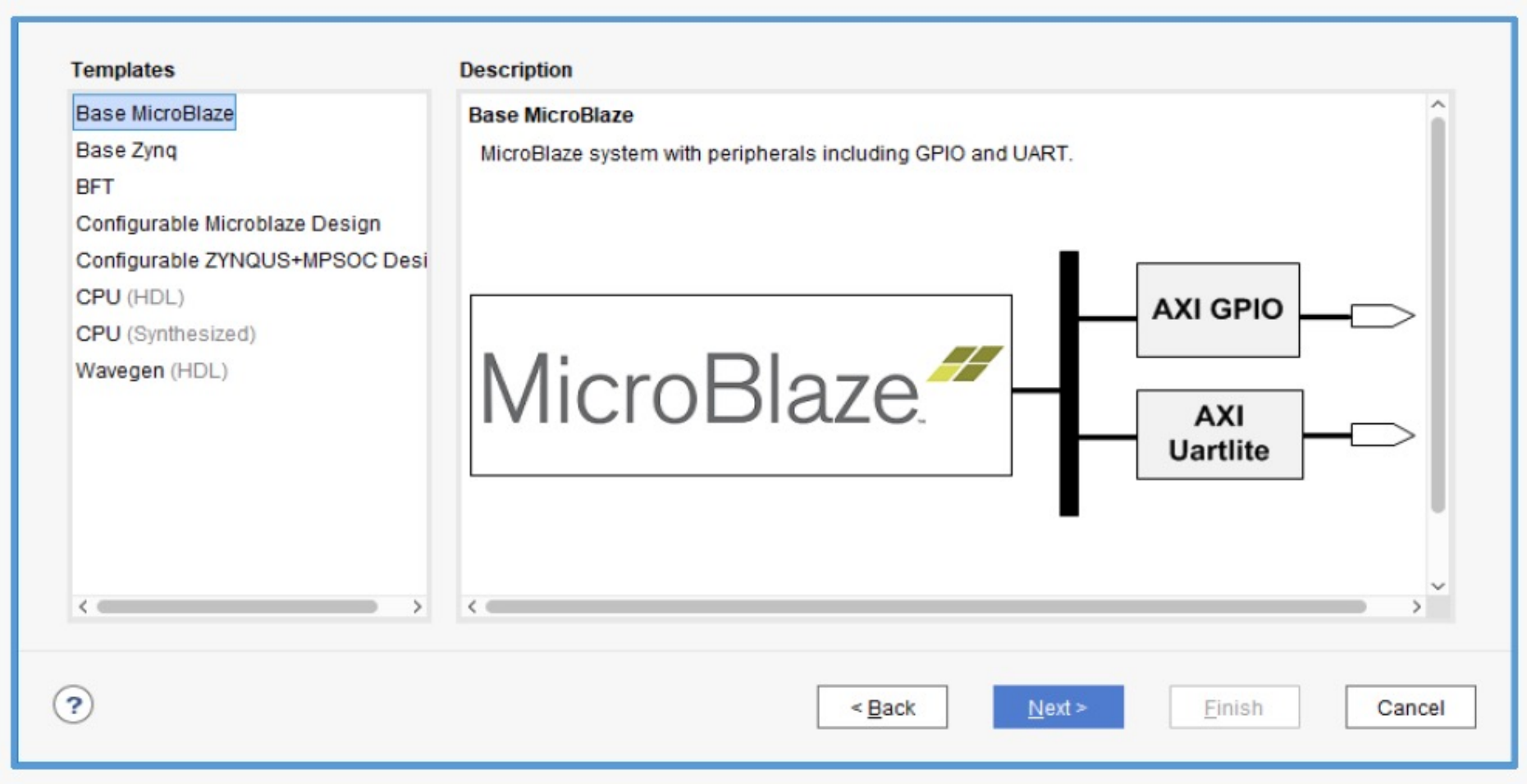


Interface	Features	Similar to
Memory Map / Full (AXI4)	Traditional Address/Data Burst (single address, multiple data)	PLBv46, PCI
Streaming (AXI4-Stream)	Data-Only, Burst	Local Link / DSP Interfaces / FIFO / FSL
Lite (AXI4-Lite)	Traditional Address/Data—No Burst (single address, single data)	PLBv46-single OPB

CityU Department of Electrical Engineering 香港城市大學 City University of Hong Kong

MicroBlaze & AXI Bus Interface

MicroBlaze is Xilinx's 32-bit RISC soft processor core, optimized for embedded applications on Xilinx devices.

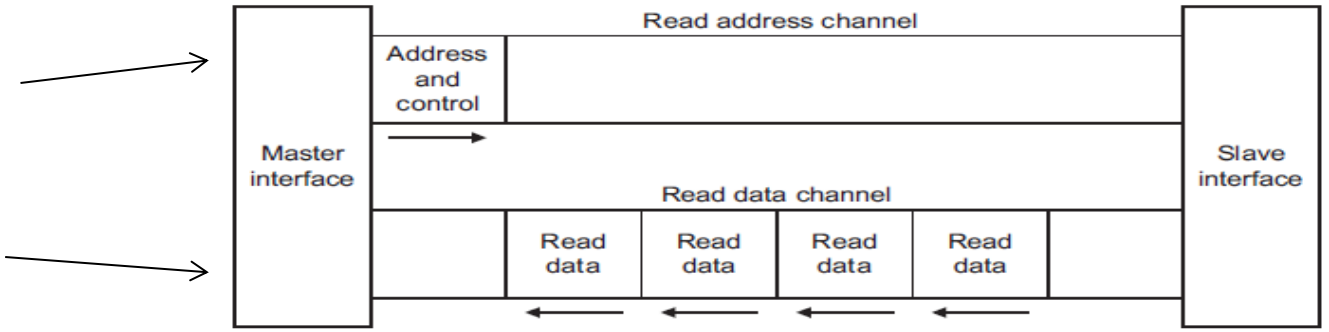


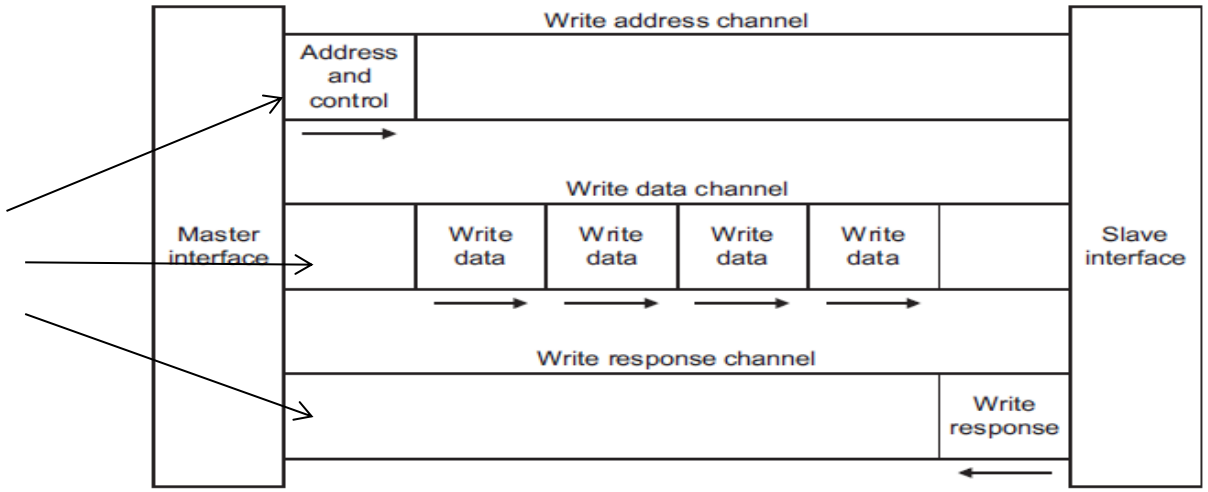
Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Basic AXI Signaling – 5 Channels

1. Read Address Channel
2. Read Data Channel

3. Write Address Channel
4. Write Data Channel
5. Write Response Channel



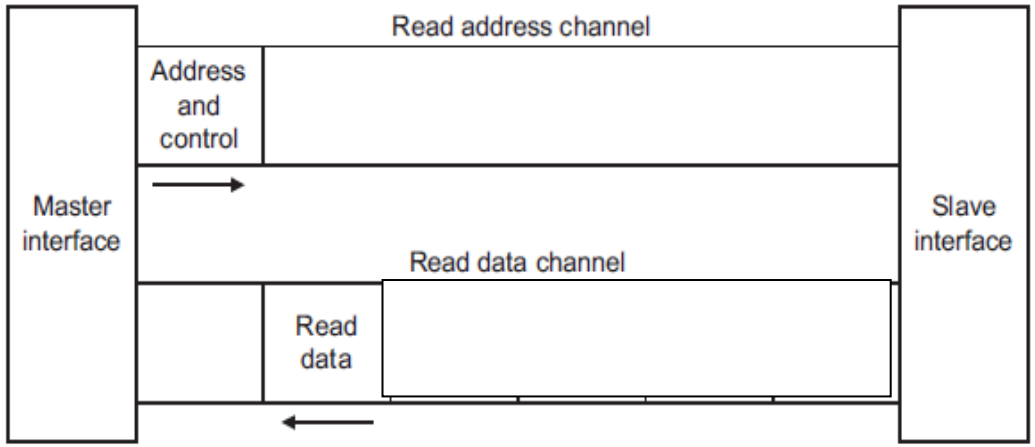


CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

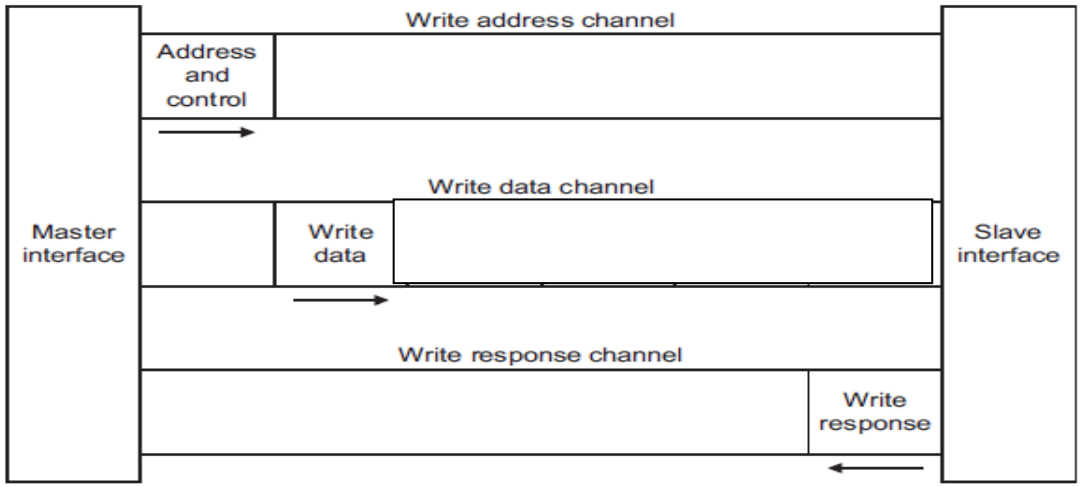
AXI Interface - AXI4-Lite

- No burst
- Data width 32 or 64 only
  - Xilinx IP only supports 32-bits
- Very small footprint
- Bridging to AXI4 handled automatically by AXI_Interconnect

AXI4-Lite Read



AXI4-Lite Write

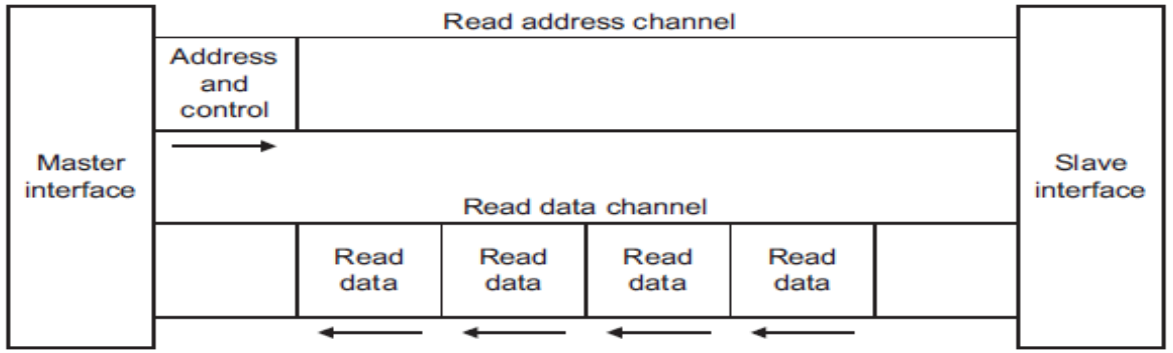


CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

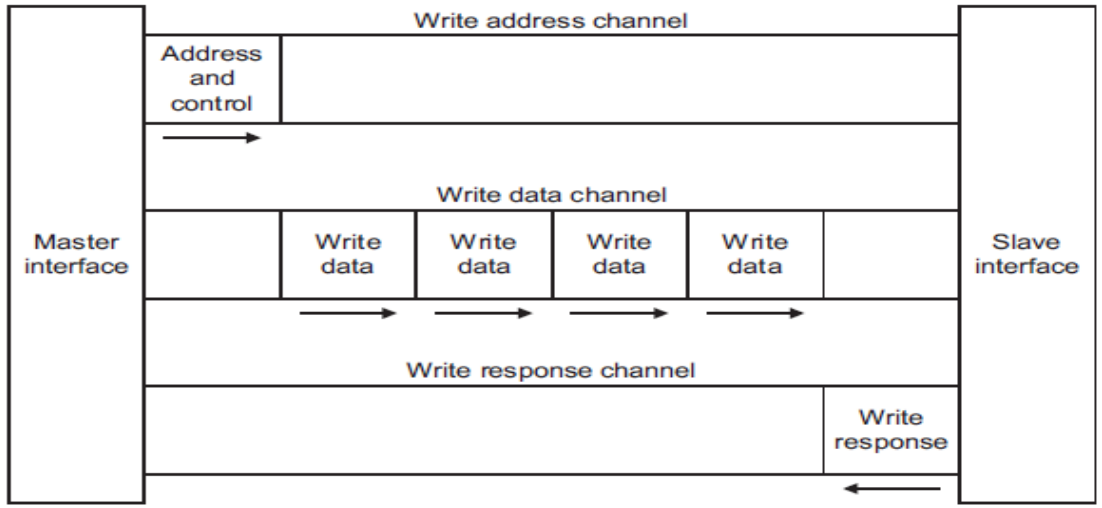
The AXI Interface - AXI4

- Sometimes called "Full AXI" or "AXI Memory Mapped"
- Single address multiple data
  - Burst up to 256 data beats
- Data Width parameterizable
  - 1024 bits

AXI4 Read



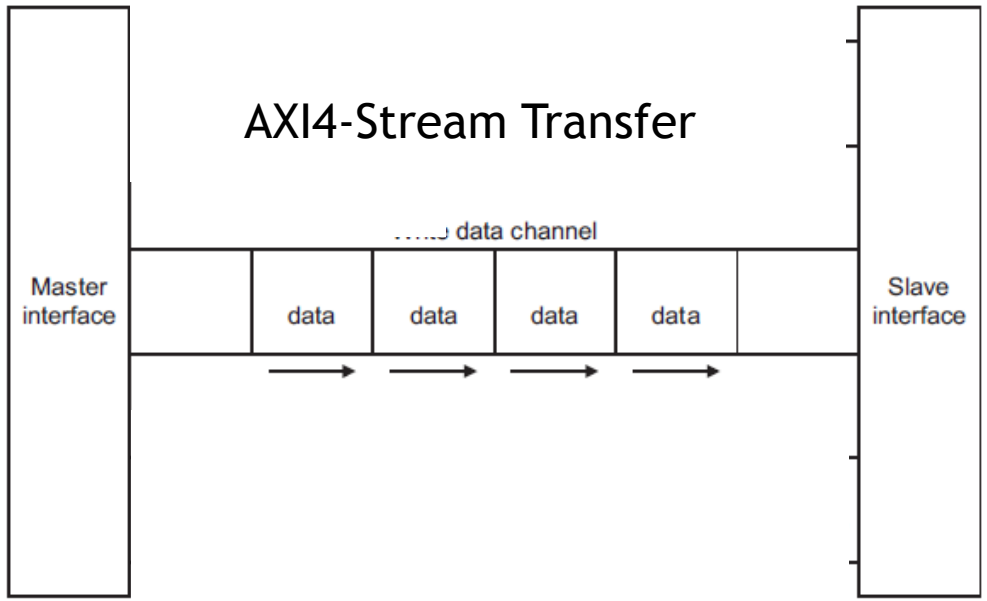
AXI4 Write



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

The AXI Interface—AXI4-Stream

- No address channel, no read and write, always just master to slave
  - Effectively an AXI4 "write data" channel
- Unlimited burst length
  - AXI4 max 256
  - AXI4-Lite does not burst
- Virtually same signaling as AXI Data Channels
  - Protocol allows merging, packing, width conversion
  - Supports sparse, continuous, aligned, unaligned streams



CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Streaming Applications

- May not have packets
  - E.g. Digital up converter
    - No concept of address
    - Free-running data (in this case)
    - In this situation, AXI4-Stream would optimize to a very simple interface
- May have packets
    - E.g. PCIe
    - Their packets may contain different information
    - Typically bridge logic of some sort is needed

CityU Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Ordering Information

- Each Letter has a special meaning

Device	Speed Grade and Junction Temperature Range		
	Commercial (C) 0°C to +85°C	Extended (E) 0°C to +100°C	Industrial (I) –40°C to +100°C
XC7Z007S XC7Z012S XC7Z014S	-1	-2	-1, -2
XC7Z010 XC7Z015 XC7Z020	-1	-2, -3	-1, -2, -1L
XC7Z030 XC7Z035 XC7Z045	-1	-2, -3	-1, -2, -2L
XC7Z100	-1	-2	-1, -2, -2L

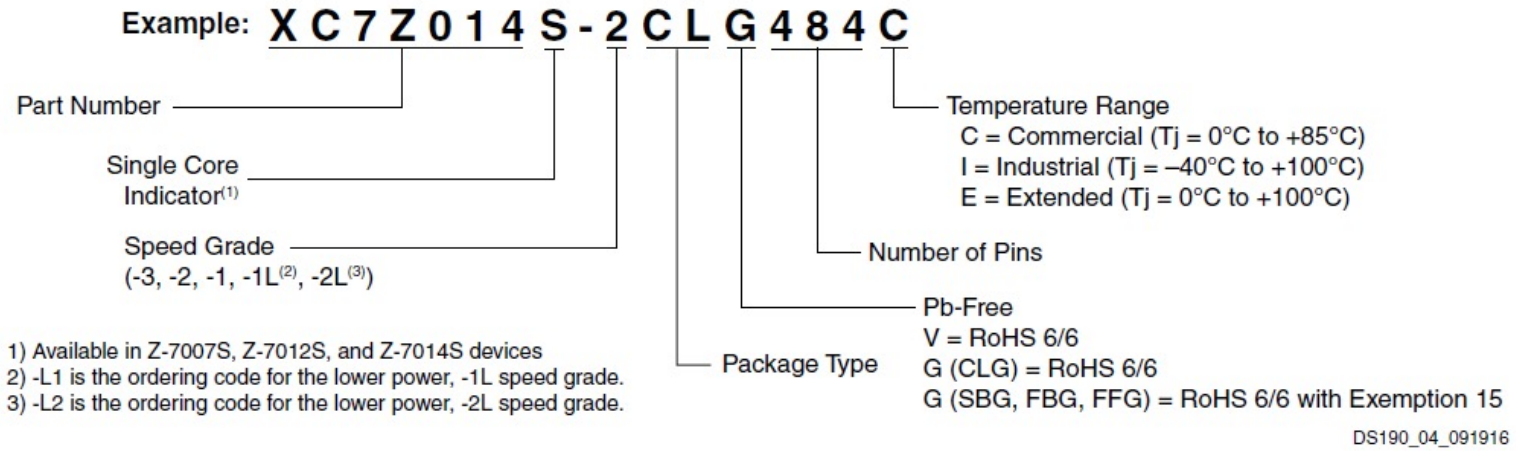


Figure 4: **Ordering Information**

CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

Summary

- The Zynq-7000 processing platform is a system on a chip (SoC) processor with embedded programmable logic
- The processing system (PS) is the hard silicon dual core consisting of
  - APU and list components
  - Two Cortex-A9 processors
  - NEON co-processor
  - General interrupt controller (GIC)
  - General and watchdog timers
  - I/O peripherals
  - External memory interfaces

Summary

- The programmable logic (PL) consists of Xilinx "7 series" technology (28nm)
- AXI is an interface providing high performance through point-to-point connection
- AXI has separate, independent read and write interfaces implemented with channels
- The AXI4 interface offers improvements over AXI3 and defines
  - Full AXI memory mapped
  - AXI Lite
  - AXI Stream
- Tightly coupled AXI ports interface the PL and PS for maximum performance
- The PS boots from a selection of external memory devices
- The PL is configured by and after the PS boots