

Logic Circuit Design - Tutorial 7

1. Figure Q1 shows a bidirectional universal shift register and its functional table is given in Table Q1.

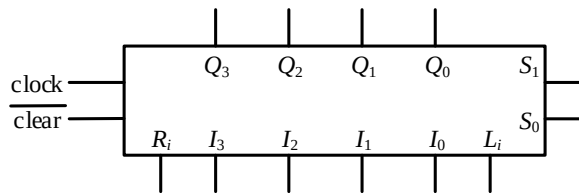


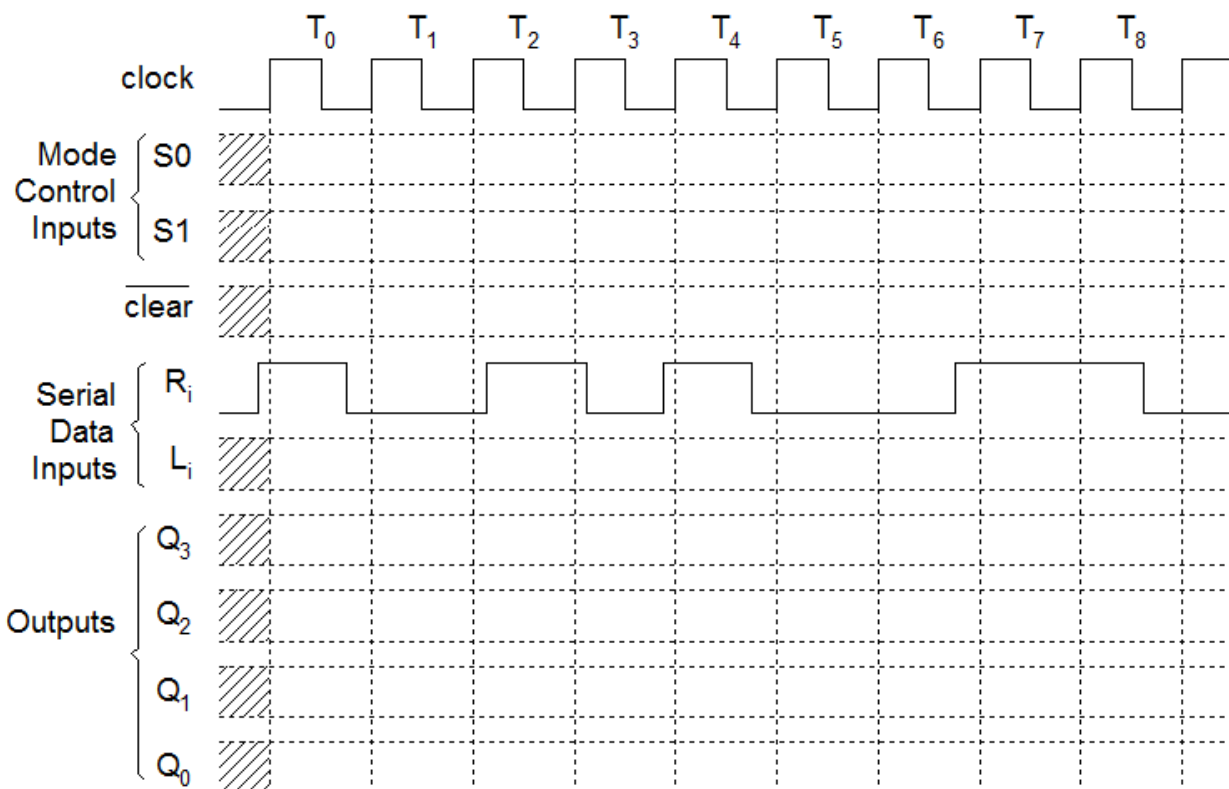
Figure Q1

$\overline{\text{clear}}$	$S_1 S_0$	clock	Q_i	Description
L	X X	X	0	Clear output
H	L L	$\uparrow$	Q_i	Data hold (inhibit)
H	L H	$\uparrow$	Q_{i+1}	Shift right
H	H L	$\uparrow$	Q_{i-1}	Shift left
H	H H	$\uparrow$	I_i	Parallel load

Table Q1

The above register can be used to perform serial data to parallel data conversion. Complete the timing diagram given below according to the following steps for each serial-to-parallel conversion. (**You must consider the propagation delay time when completing the timing diagram.**)

- Clear the output;
- Start to shift the 4 bits serial data to the register;
- Hold the data for one clock cycle;
- Repeat step i.



- Q2. Figure Q2 shows a 3-bit up-count counter with an active high asynchronous preset pin. Draw a circuit with counting sequence as follow:

000, 001, 011, 010, 110, 111, 000, 001, 011, ..., ..., .

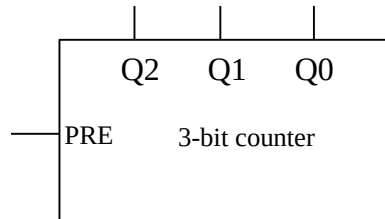


Figure Q2

- Q3. Design a modulo-6 counter based on a synchronous 3-bit binary counter with synchronous preset and clear pins.
- Q4. Design a counter circuit to generate a single pulse for every 10 clock pulse based on a synchronous 4-bit binary counter with synchronous clear 74LS163. Can 74LS161 be used in this design and why?