

13 Display System

- Display is an important part of a human-computer-interface system.
- From CRT (Cathode Ray Tube) to LCD (Liquid Crystal Display)
- The display system design is evolved from TV system.
- Video is displayed using raster scanning principle.

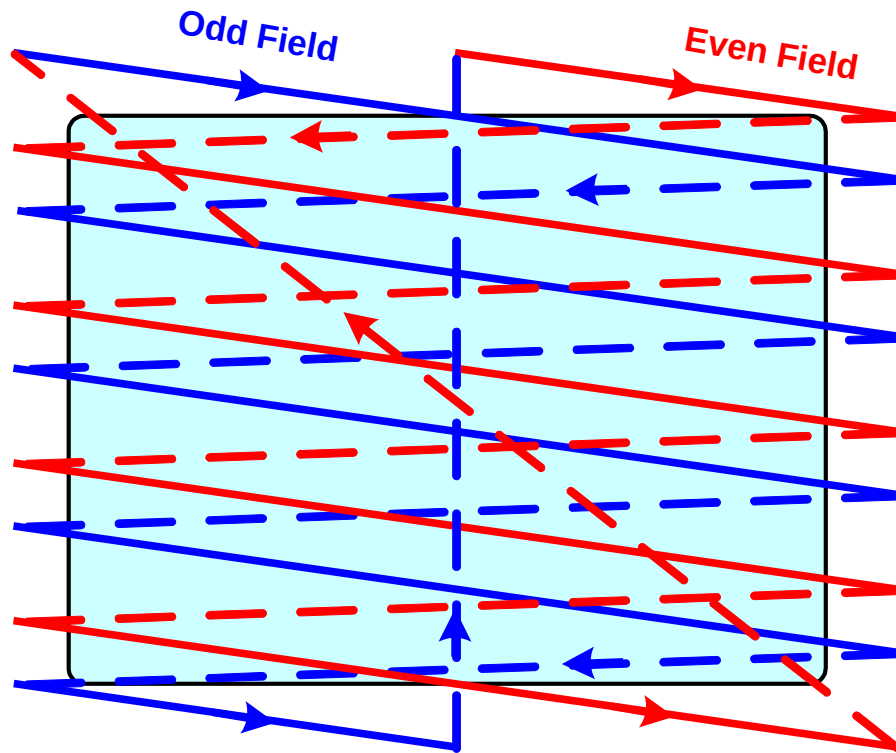
13.1 Raster scanning



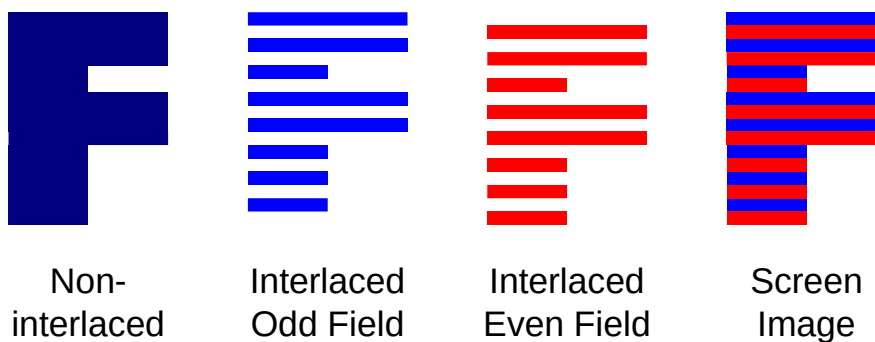
- An image can be considered as a matrix of pixels (picture elements).
- CRT display screen is coated with a matrix of phosphors and they will be bright up when stroke by an electron beam.
- If we map the image pixels to the phosphors, then the image can be displayed on the screen by sweeping an electron beam through the entire screen.
- Two types of technique are used to sweep the electron beam: interlaced scanning and progressive scanning.

13.1.1 Interlaced scanning

- TV and video pictures are made up of a number of images (frames) that are sequentially displayed on your screen to give the illusion of movement.
- The rate at which the frames are displayed is fixed at 25 fps (frames-per second) in the PAL system, and 30 fps in the NTSC system.
- In order not to perceive the flickering effect, each frame is divided into two fields: odd-field and even-field.

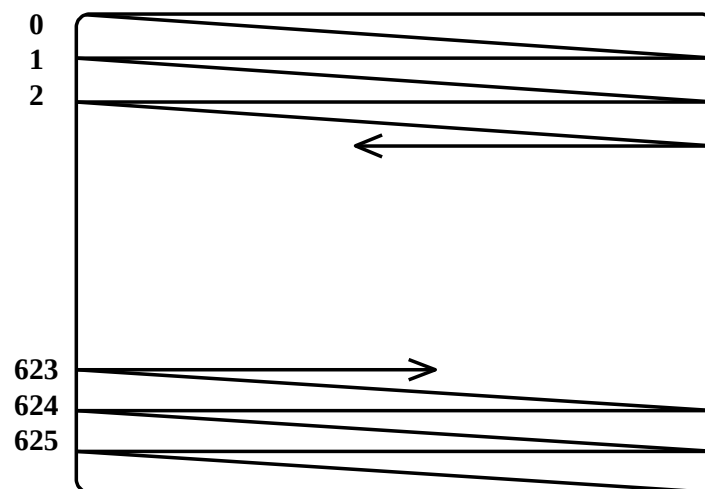


- During retrace (dotted-lines), the electron beam is turned off and the screen will not be affected.
- Only the middle part will be seen on the TV screen and it is called the active region.
- The figure below shows an image of an alphabet F produced from different fields.



13.1.2 Progressive scanning

- Also called non-interlaced scanning.
- The lines of each frame are drawn in sequence, i.e. one field per frame.
- In order to avoid flickering effects, the frame rate is higher, twice of that of the interlaced scanning.
- This technique is mostly used in computer monitor, DVD and HDTV (high-definition TV).
- Deinterlacing is used to display DVD video in ordinary TV set.



Progressive scan

13.2 LCD

The recent technological advancement brings down the cost of produce LCD and it becomes the main stream of computer monitor.

13.2.1 Liquid crystal

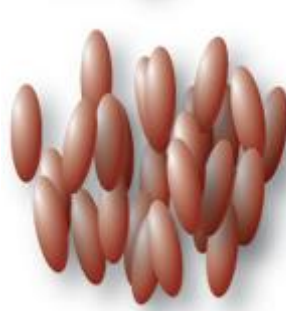
- Substance exists in three states (solid, liquid and gas: classic example is H₂O) and it can be attributed to the temperature of the substance.
- A thermotropic liquid crystalline phase occurs in some substances in a temperature region between the solid and liquid states.
- In this state *the substance possesses some properties of both liquids and solids.*
- A liquid crystal is a fluid like but is anisotropic in its optical and electro-magnetic characteristics like a solid.
- When the liquid crystal is formed from the isotropic state some amount of positional or orientational order is gained.

13.2.2 Nematics

By decreasing the temperature from the isotropic phase, in which the liquid crystal molecules (like a long thin rod) are randomly positioned and oriented, to the nematic phase the material gains an amount of orientational order but no positional order.



Isotropic phase



Nematic phase

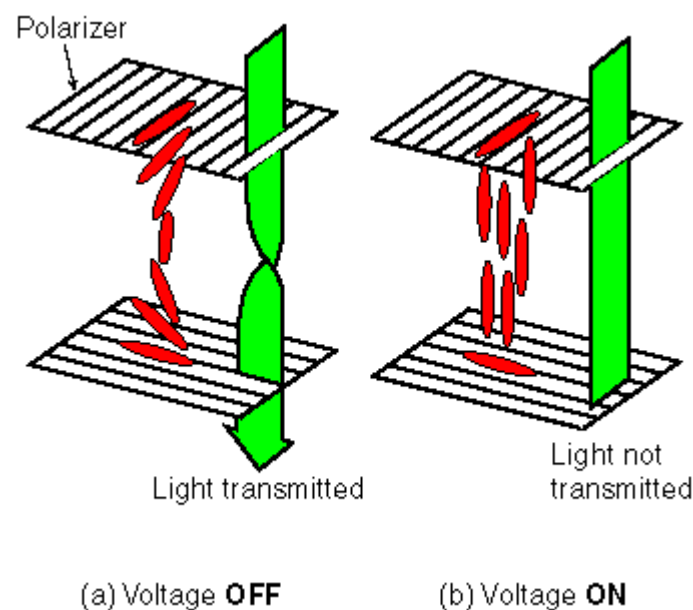
13.2.3 Chiral nematics

- Chiral nematic phase will occur when the molecules that make up a nematic liquid crystal are chiral (i.e. they are not symmetric when reflected).
- In this phase the molecules prefer to lie next to each other in a slightly skewed orientation and this induces a helical director configuration in which the director rotates through the material.



13.2.4 Twisted Nematic (TN)

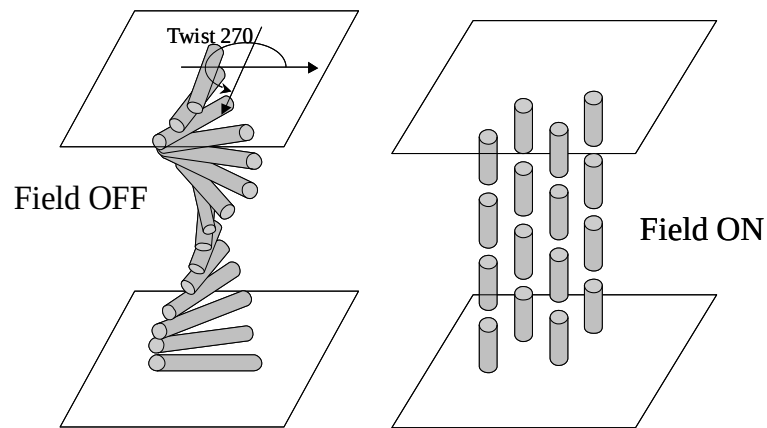
- This helical internal structure is the key to the operation of Twisted Nematic (TN) liquid crystal displays.
- A nematic is placed between two crossed polarizers and the molecules at the cell surfaces are aligned such that the director lies parallel to the polarizers.
- Without the presence of the liquid crystal, light entering from the top of the cell would not be transmitted through the cell due to the crossed polarizer.
- However the helical director structure **guides** the polarized light from the upper polarizer round so that the light may be transmitted through the lower polarizer.
- When a voltage is applied across the cell, the molecules align with the electric field due to a dielectric interaction between the molecule and the electric field. This destroys the helical structure and the light cannot be transmitted through the cross-polarized glasses as shown in the figure below.



Principle of TN

13.2.5 Super Twisted Nematic (STN)

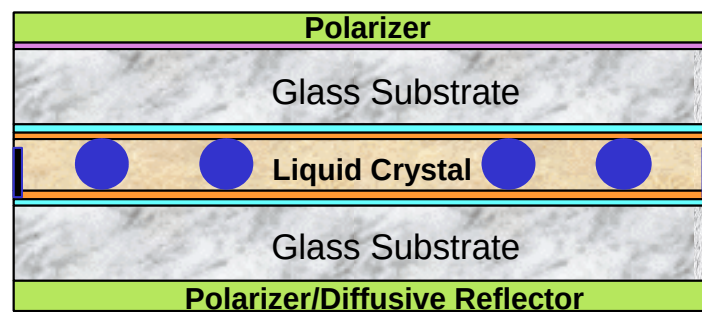
- Twisted nematic displays rotate the director of the liquid crystal by 90° ,
- Super-twisted nematic displays employ up to a 270° rotation.



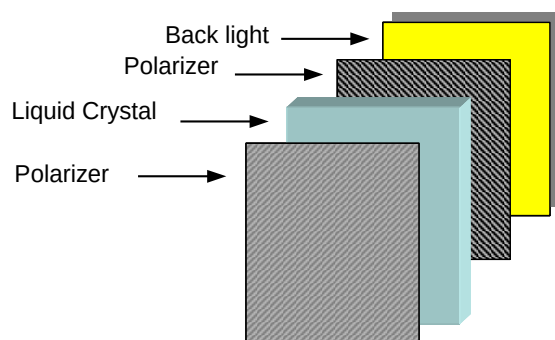
Principle of STN

13.2.6 **Passive** matrix LCD

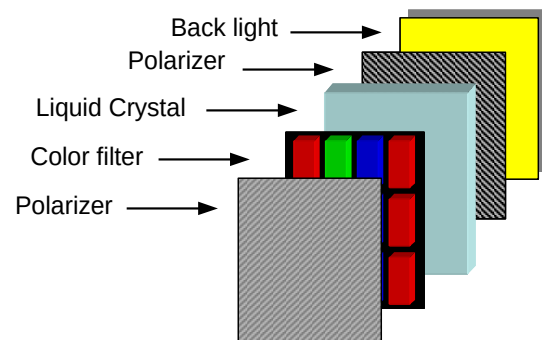
- Passive matrix LCD is implemented with STN technology.
- Passive-matrix LCD uses a simple grid to supply the charge to a particular pixel (LC cell) on the display.
- Two glass layers called substrates are used.
- One substrate is given columns and the other is given rows.
- The liquid crystal material is sandwiched between the two glass substrates, and a polarizing film is added to the outer side of each substrate.



- To turn on a pixel, charges are sent to the correct column of one substrate and a ground activated on the correct row of the other.
- The row and column intersect at the designated pixel, and that delivers the voltage to untwist the liquid crystals at that pixel.
- For color passive LCD, a color filter is added.



Monochrome STN LCD



Color STN LCD

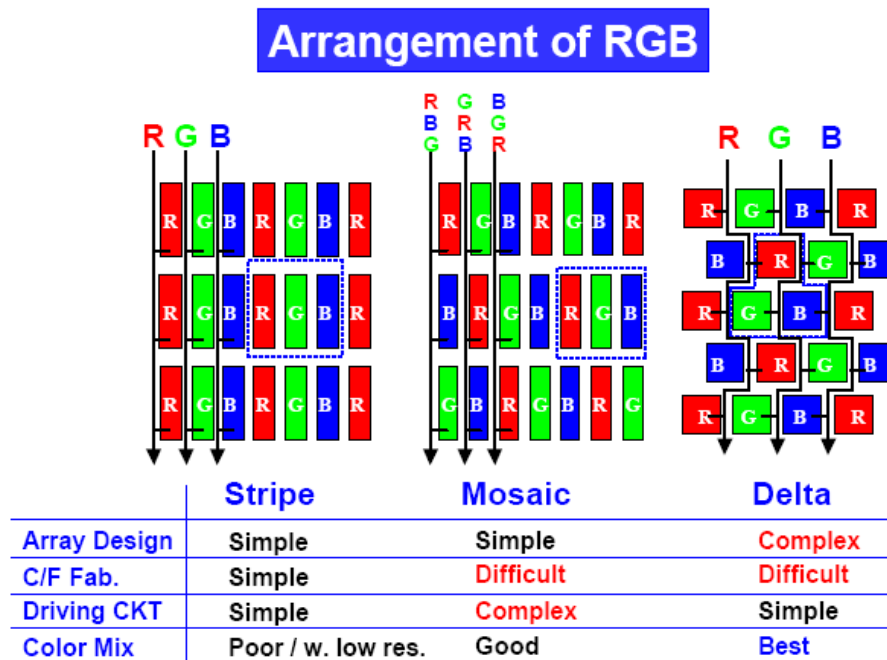


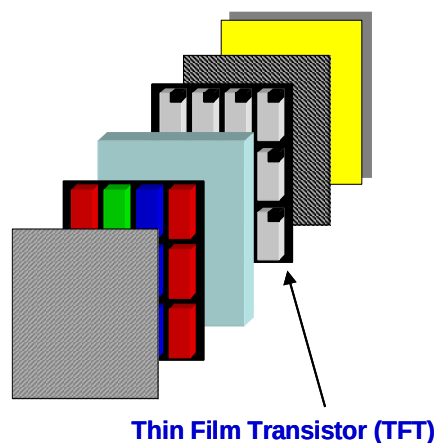
Figure 43. Arrangement of the RGB color-filter

Arrangement of the RGB color filter

- By comparing with the monochrome LCD, pixels number will be tripled for color LCD, i.e., one pixel consists of 3 subpixels, with red, green and blue color filters to create each color pixel.
- **Passive LCD only turns ON/OFF the LC cell and hence it cannot display gray level in a single cycle.**
- *Dithering technique* and *Frame Rate Control (FRC)* are used to generate gray level for passive LCD.
- The quality of passive STN LCD is low, not suitable for fast change scene or movie
- However passive LCD is relatively cheap to produce.
- Limited color choices.

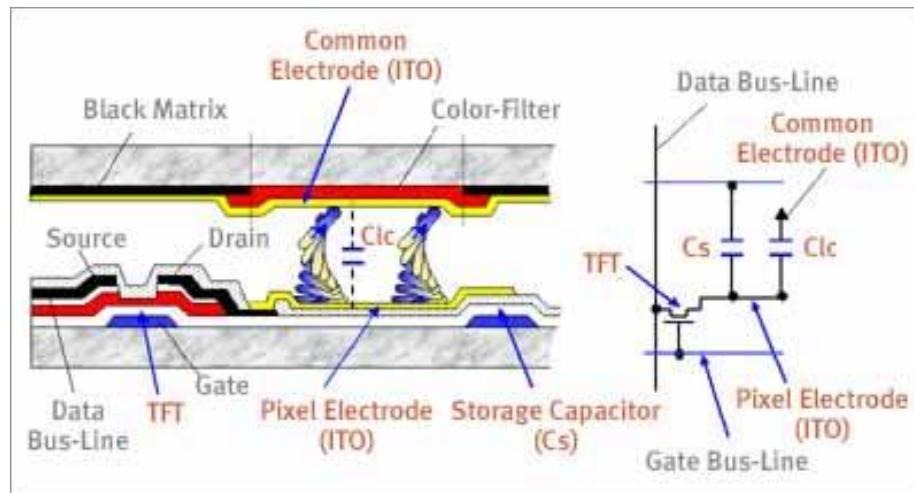
13.2.7 TFT **Active** matrix LCD

- TFT (thin film transistors - which are tiny switching transistors and capacitors) LCD is one type of active-matrix LCD.
- They are also arranged in a matrix on a glass substrate.
- When a particular pixel is addressed, only the capacitor at the designated pixel receives a charge.
- The capacitor is able to hold the charge until the next refresh cycle.
- If the amount of voltage supply a crystal LC is carefully controlled, the LC elements can be made untwist to allow the corresponding amount of light through the LCD.
- By doing this in very exact, very small increments, LCDs can create a gray scale. Most displays today offer 256 levels (8-bit) of brightness per pixel.

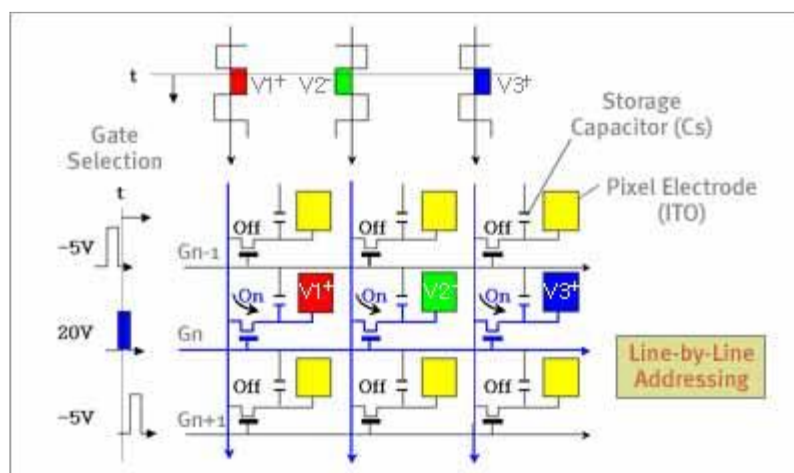


Color TFT LCD

- With 3 color (R,G and B) filters, more color can be achieved – 8-bit each can produce 24-bit color.



Vertical structure of a unit pixel and its equivalent circuit



Active addressing of a 3x3 matrix

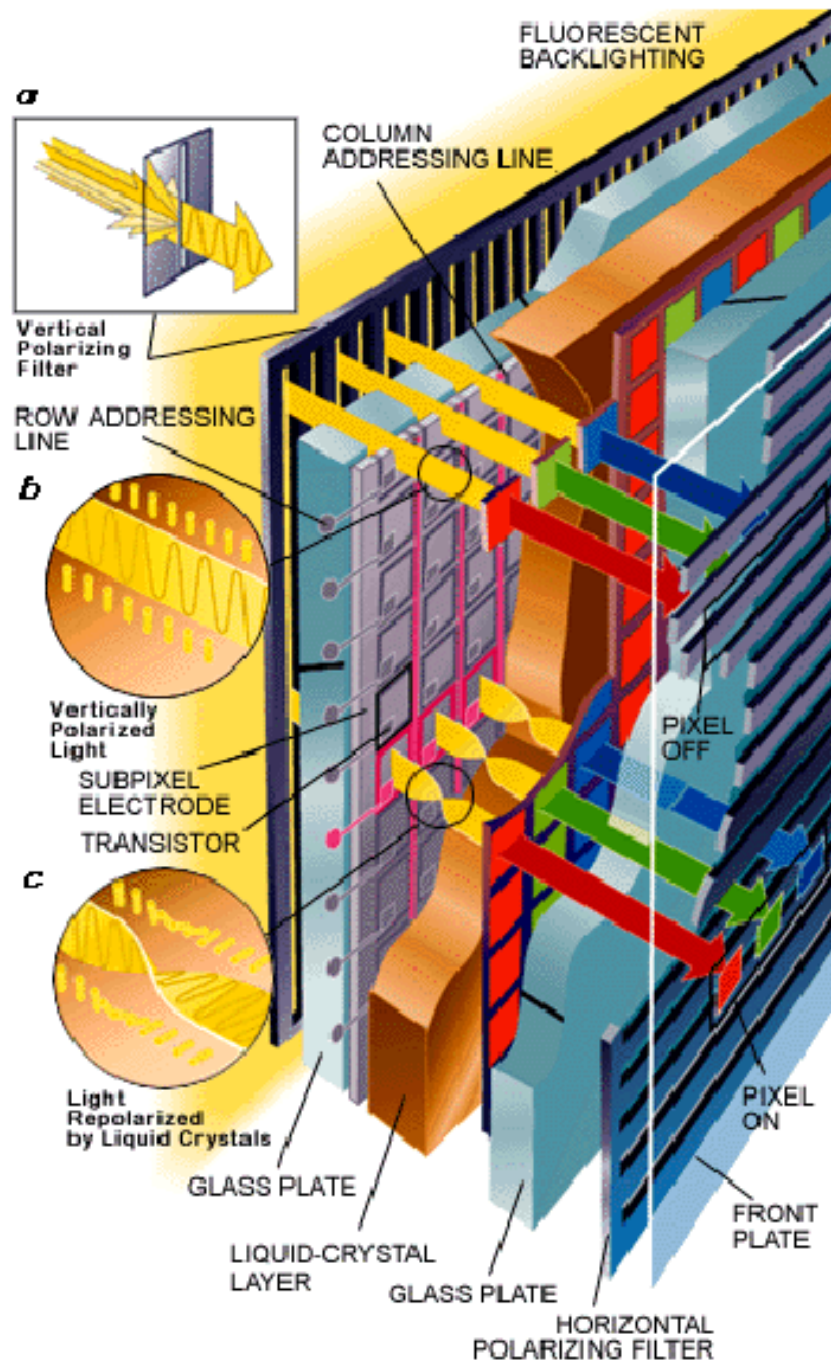
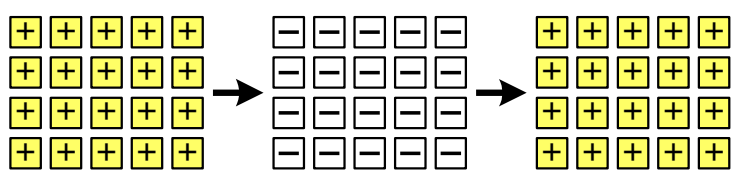
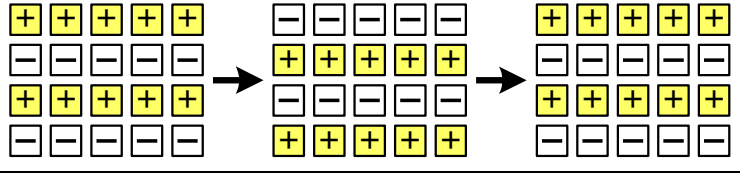
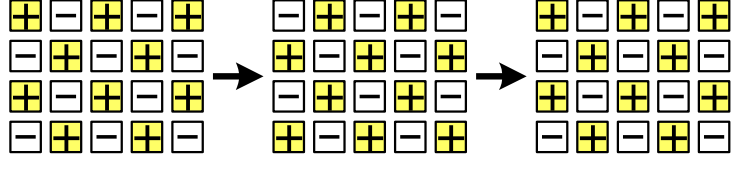


Illustration of Active matrix display

13.2.8 LC driving method

- Liquid crystal must be driven with an alternating current to prevent any deterioration of image quality resulting from dc stress.
- This is usually implemented with a frame-reversal drive method, in which the voltage applied to each pixel varies from frame to frame.
- If the LC voltage changes unevenly between frames, flickering effects will be observed.
- Other drive methods are available that prevent this flicker problem.

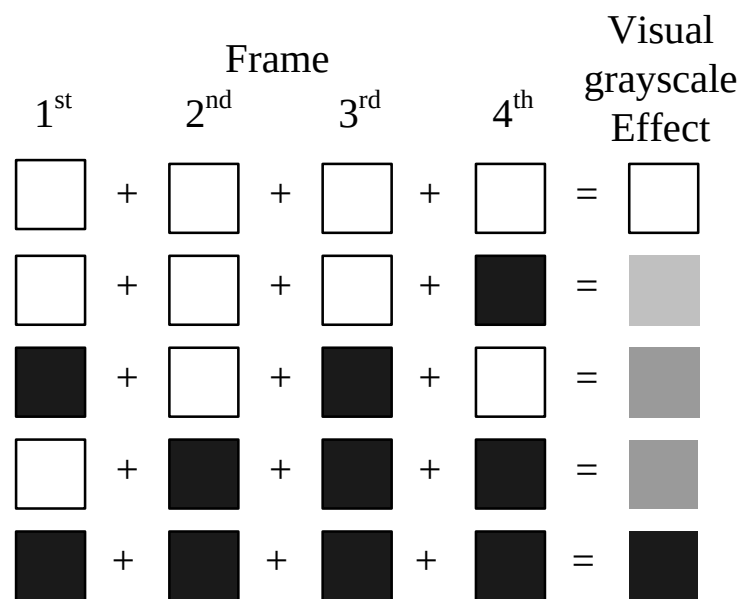
Driving Method	1 st frame → 2 nd frame → 3 rd frame
Frame Inversion	
H-Line Inversion	
Dot Inversion (Flicker free)	

13.2.9 **Passive TN/STN** gray level (color depth) production

- TN/STN can only display black (off) and white (on) and unable to display gray shades or gray scales.
- **Dithering technique** and **Frame Rate Control (FRC)** are two common driving methods to generate grayscale in STN LCD Panel.
- If a **color filter** is used, the output will be of different color depth.

13.2.9.1 Frame rate control (FRC)

- FRC generates grayscales by turning pixels on and off over several frame periods.
- With sufficient frame refreshing frequency, our human eyes will average out the darkness of a pixel so that the individual pixel will show as gray.
- Here is an example of using FRC over 4 frame periods to generate 5 grayscale levels:



FRC Driving Method

- FRC is an easier driving method for implementing grayscale and thus is commonly used for gray level STN LCD.
- To avoid flickering on the display, the sequence of “ON” and “OFF” pattern should be randomized across each group of FRC pattern.
- Besides, sufficient high frequency is necessary in order to achieve a smooth display.
- The potential problems with this method are brightness variations and shadowing, especially when used to shade larger areas.

FRC:

Number of frames to produce different gray levels is fixed.

13.2.9.2 Time-based Dithering

- Extend the concept of FRC.
- Gray level (or color depth) is controlled by the duty cycle of a dither pattern.
- The following shows the pixel on/off state of a 16-bit dither pattern for a 16 gray levels display device.

Gray level	Duty cycle	Frame no.															
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0/16																
1	1/16	1															
2	2/16	1								1							
3	3/16	1						1					1				
4	4/16	1				1				1				1			
5	5/16	1				1			1			1			1		
6	6/16	1			1			1		1			1			1	
7	7/16	1			1		1		1		1			1		1	
8	8/16	1		1		1		1		1		1		1		1	
9	9/16		1	1		1		1		1		1		1	1		1
10	10/16		1	1		1	1		1		1	1		1	1		1
11	11/16		1	1	1		1	1		1	1		1	1		1	1
12	12/16		1	1	1		1	1	1		1	1	1		1	1	1
13	13/16		1	1	1	1	1		1	1	1	1	1		1	1	1
14	14/16		1	1	1	1	1	1	1		1	1	1	1	1	1	1
15	15/16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Probability of Pixel "ON"		9/16	7/16	8/16	7/16	8/16	7/16	8/16	7/16	8/16	7/16	8/16	7/16	8/16	7/16	8/16	7/16
		0.5625	0.4375	0.5	0.4375	0.5	0.4375	0.5	0.4375	0.5	0.4375	0.5	0.4375	0.5	0.4375	0.5	0.4375

Note that empty box is "0" and represents pixel-off.

- Each pixel will be turned on and off over a period of time (in principle 16 frames for 16 gray levels) to realize different gray level.

- General assumption: probability of the 16 gray levels appearing in each pixel is equal due to the random distribution nature of graphics/images.
- The probability of pixel-on and pixel-off for each frame should be made equal as far as possible, if not it should be at least close to 0.5 (range from 0.4375 to 0.5625), in order to avoid flickering noise.
- Flickering noise becomes severe if adjacent pixels are of the same gray level, effectively seeing a large size pixel.
- Employs a time-base dithering algorithm to vary the dither pattern for adjacent pixels on every frame.
- The algorithm can be realized by using modulo counters to count the line number and frame number for selecting the starting point of the dither pattern (duty cycle will not be changed for a cyclic pattern).
- In practice, most STN LCD controllers employ dither patterns that only approximate the duty cycles, an example is shown below:

Gray Level (pre-dither duty cycle)	Duty Cycle	Gray Level (pre-dither duty cycle)	Duty Cycle
15	1	7	1/2
14	6/7	6	3/7
13	4/5	5	2/5
12	3/4	4	1/3
11	5/7	3	1/4
10	2/3	2	1/5
9	3/5	1	1/7
8	4/7	0	0

**** The length (number of frames) of the time-based dither pattern is different for different duty cycle, whereas the length is the same for FRC method.

- S3C44B0X has eight programmable dither registers DPn_m

Pattern Name	Gray Level	Number of Bits	Recommended Dithering Pattern
DP1_2	7	16	1010 0101 1010 0101 (0xA5A5)
DP4_7	8	28	1011 1010 0101 1101 1010 0110 0101 (0xBA5DA65)
DP3_5	9	20	1010 0101 1010 0101 1111 (0xA5A5F)
DP2_3	10	12	1101 0110 1011 (0xD6B)
DP5_7	11	28	1110 1011 0111 1011 0101 1110 1101 (0xEB7B5ED)
DP3_4	12	16	0111 1101 1011 1110 (0x7DBE)
DP4_5	13	20	0111 1110 1011 1101 1111 (0x7EBDF)
DP6_7	14	28	0111 1111 1101 1111 1011 1111 1110 (0x7FDFBFE)

- Gray level dither pattern for **1-6** can be obtained by inverting its counterpart:
e.g. 1/7 (1/4) can be made by inverting 6/7 (3/4).

13.2.10 STN LCD versus TFT LCD

- Generally, time-based dithering algorithm is used to drive STN LCD to produce different color depth.
- STN LCD also requires higher refresh rate to produce color depth.
- Consequently it cannot respond to fast changing scene.
- Cost of production is lower.
- The color depth of each pixel of TFT LCD can be precisely adjusted in each frame by directly applying a voltage to the LC.
- TFT LCD can respond to fast changing scene.
- Thus, the visual color performance for TFT LCD is much better than STN LCD.
- Cost of production is higher.
- Applications of STN LCD:
 - Low-end product (cheap)
 - Character LCD display
 - Clock display for mobile phone
 - Display panel for instrument
 - Display module for VCD/DVD player, etc.
- Applications of TFT LCD:
 - High-end product (a bit expensive)
 - Display requires high performance – monitor, TV, etc.

13.2.11 Illumination techniques

- All of the light seen by the user comes through the LCD from the backlight.
- It is typically completely black (unreadable) in direct sunlight since sunlight is much brighter than LCD's backlight and the reflection of sunlight from the surface of the LCD overwhelms any light coming through the LCD.
- Cold Cathode Fluorescent (CCFL) or LED
- It consists of a *rectangular light guide*, a *diffuser*, which enhances display uniformity, and a *brightness enhancement film* (BEF), which enhances display brightness.
- High power LEDs are now commonly used
- Light sources can be arranged in evenly distributed manner.
- Slim, low power consumption

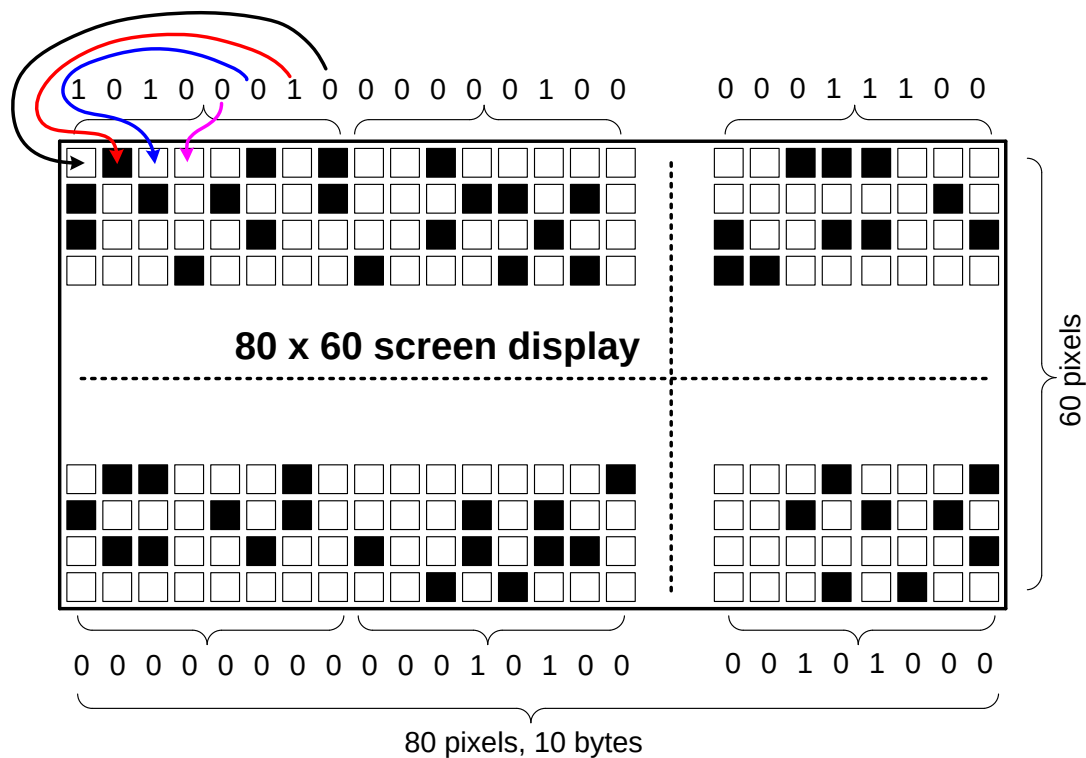
13.3 Frame Buffer

- Video display content is digitized and stored in binary format in main memory.
- This portion of memory is called frame buffer since it stores the content of one complete video frame.
- A video display controller will scan the content of the frame buffer and output the content to the display device with a pre-defined frame rate.
- When the information stored in the frame buffer is altered, its corresponding pixel positions on screen will also be changed.
- Frame buffer size is associated with screen resolution and display mode (monochrome, gray level and color).

Example: For monochrome (black & white) display with resolution 80×60 , 1 byte can represent 8 pixels.

Total no of pixel: $80 \times 60 = 4800$

Total frame buffer size: $4800 / 8 = 600$ bytes



Frame buffer size content (Byte size)	
Memory Address	Content
FB-add + 0	10100010
FB-add + 1	00000100
.	.
.	.
FB-add + 9	00011100
.	.
.	.
.	.
FB-add + 590	00000000
FB-add + 591	00010100
.	.
.	.
FB-add + 599	00101000

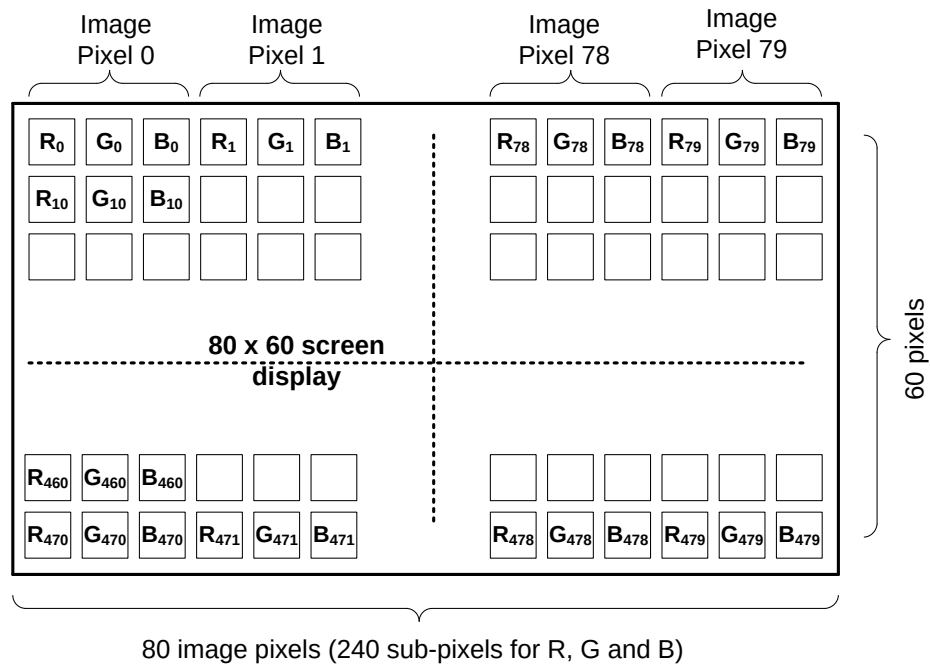
- **Note that the frame buffer storage format must match with that of the display controller, that means the storage format varies with different controllers.**

- The above example is for controller sending the top left pixel first and that corresponding to the LSB of the first byte in the frame buffer.
- For color display, the format of the video data stored in the frame buffer is also dependent on controller design.
- For true color (24-bit), i.e., 8-bit for Red (R), 8-bit for Green (G) and 8-bit for Blue (B), one pixel will occupy 3 bytes of memory and number of available color is 2^{24} .
- Color display device uses 3 sub-pixels to form one image pixel and the effective resolution is 3 times higher.
- The clock rate for sending the color video data to the display device will also be 3 times.

Example: For 24-bit color display with resolution 80×60 , it requires 3 bytes to represent 1 pixel.

Total no of pixel: $80 \times 60 = 4800$

Total frame buffer size: $4800 \times 3 = 14400$ bytes

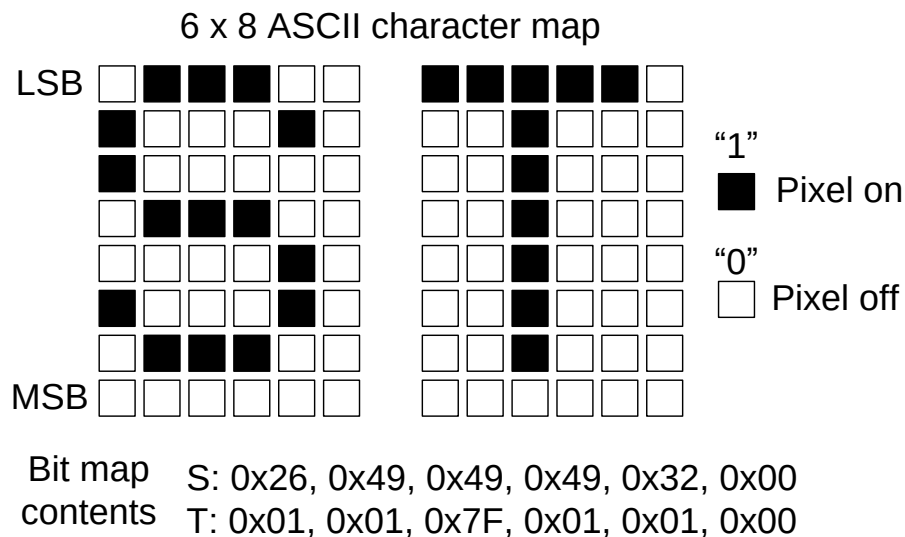


Frame buffer content (word size)	
Memory Address	Content
FB-add + 0	$R_1 B_0 G_0 R_0$
FB-add + 4	$G_2 R_2 B_1 G_1$
FB-add + 8	$B_3 G_3 R_3 B_2$
FB-add + 12	$R_5 B_4 G_4 R_4$
FB-add + 16	$G_6 R_6 B_5 G_5$
.	.
.	.
.	.
FB-add + 14280	$G_{474} R_{474} B_{473} G_{473}$
FB-add + 14284	$B_{475} G_{475} R_{475} B_{474}$
FB-add + 14288	$R_{477} B_{476} G_{476} R_{476}$
FB-add + 14392	$G_{478} R_{478} B_{477} G_{477}$
FB-add + 14396	$B_{479} G_{479} R_{479} B_{478}$

Note that the above frame buffer structure is for display controller receiving R component first, then followed by G and B components.

13.4 ASCII Character Display

- To display ASCII characters on screen, the character must be mapped to a dot matrix pattern with appropriate on/off pixel definition. The following figure shows the bit map pattern for 6×8 characters “S” and “T”:



- For hardware approach, all ASCII characters’ bit maps are stored inside a Character ROM Generator.
- When displaying a particular character, the ASCII code will be translated to an address corresponding to the storage address of that character in the Character ROM.
- A hardware circuit will scan the bit map content and output it to the display device.
- For CPU equipped with display controller, Character ROM will NOT be used.
- The bit maps are stored in the main memory and their starting address is associated with their ASCII code.
- When displaying a character, its bit map will be copied to the frame buffer locations corresponding to the screen display position.

13.5 Graphic mode and text mode

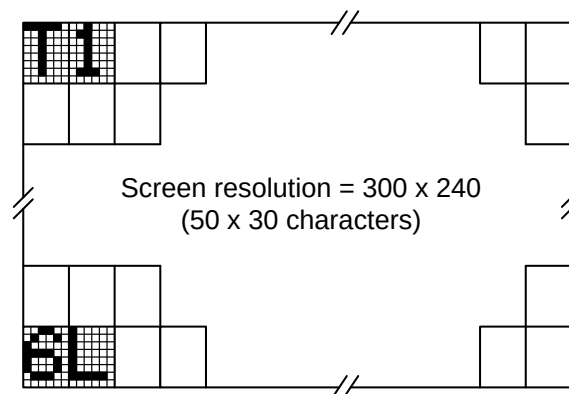
- Computer may employ graphic mode GUI (Graphic User Interface) or traditional text mode for human-machine interface.
- GUI requires to display graphic icons on screen and the screen background may well be a photograph or any graphic images.
- In graphic mode, all graphic images are represented by pixels and stored in the appropriate memory locations inside the frame buffer according to their screen position.
- In text mode, the screen is used to display ASCII characters exclusively.
- The screen is divided into “boxes” and the box size is equal to the size of the character map.

Example: For a screen resolution of 300×240 with character bit map size of 6×8 , we have

No of character/line = $300/6 = 50$ char/line

No of lines = $240/8 = 30$ lines

Therefore, the screen can display $50 \times 30 = 1500$ characters



- Displaying ASCII character in graphic mode is simply achieved by copying the character's bit map to the frame buffer location corresponding to the screen position.

13.6 Color palette

- The number of colors that can be displayed on the display screen is dependent on the design of the display device and the display controller.
- CRT receives **analog** video signal and thus may be considered to display infinite number of colors.
- However, if the analog video signal is generated from digital format, then the number of colors is dependent on the color data representation.
- Generally, “true color” is well accepted to be 24-bit (8-bit for each R, G and B components), i.e., 2^{24} colors.
- Color is also commonly represented in 16-bit, 12-bit and 8-bit, i.e., only a subset of the true color.
- Generally, TFT LCD panel is available for display 16-bit and 24-bit colors; and STN is for display 8-bit colors.
- Color selection is limited.
- Color palette allows users to select a subset of color from the full range of colors.

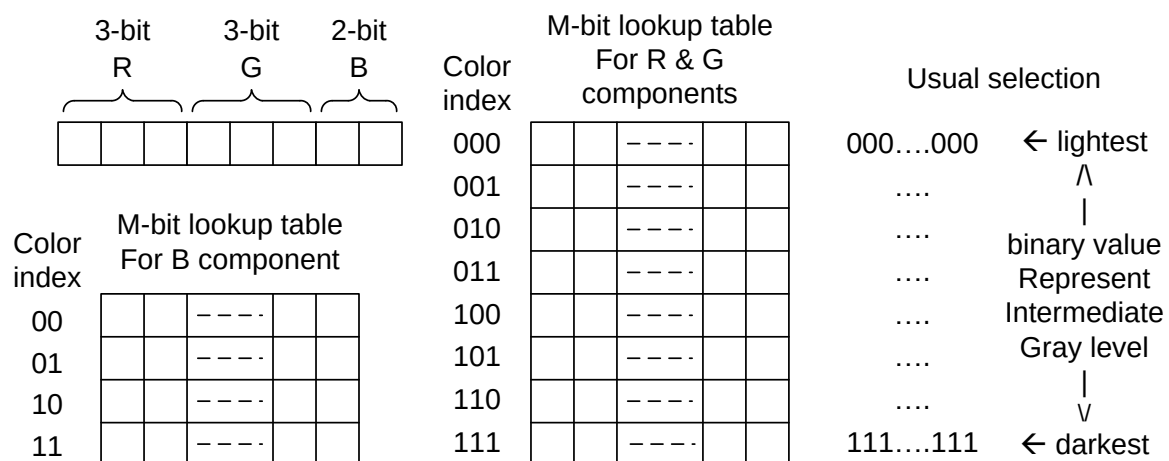


Full colors



Palette

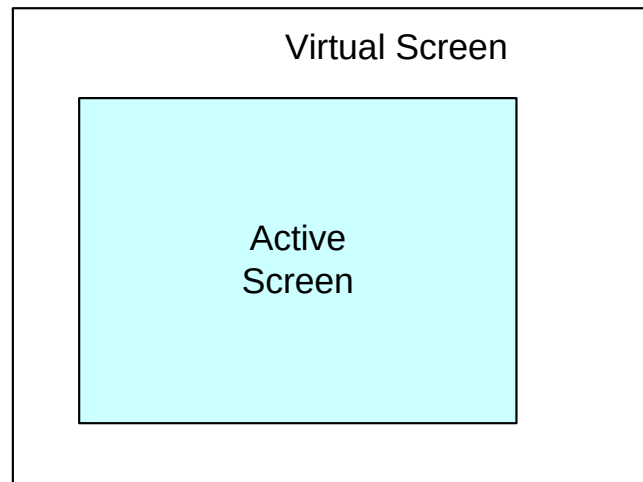
- Adopting color palette can increase choices of color.
- By means of a lookup table.
- For example, 8-bit color is composed of 3-bit R, 3-bit G and 2-bit B, these R, G and B colors will be used as a color index which points at a particular location of the lookup table.
- The color stored in the lookup table will be sent to the display device.
- **Note that the number of available colors is still limited by the original color format, say 256 for 8-bit and 2^{12} for 12-bit.**
- However, more choices on color are available simply by altering the lookup table content.



- The example shown above allows 2^M choices for each color index, 8 choices for R and G, 4 choices for B
- The bit size M of lookup table must match the design of the display controller.

13.7 Virtual screen

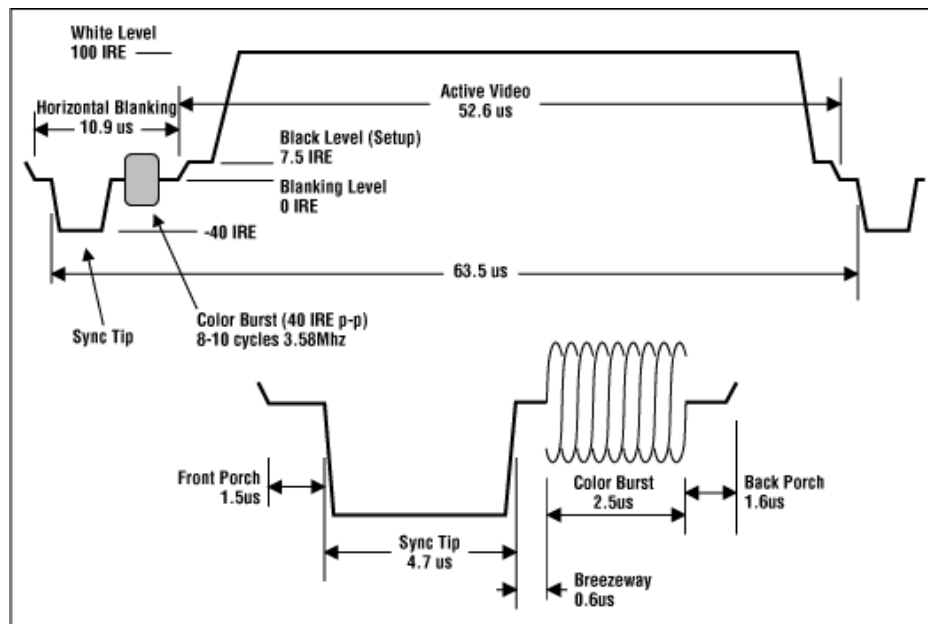
- Some display controllers support virtual screen, i.e., the actual display seen on screen is only a portion of “full screen” display.



- Two buffers will be used: one for virtual screen and one for active screen.
- For synchronization purpose, program should always update the virtual screen buffer and only copy the contents corresponding to the active screen to the active frame buffer (via DMA for fast transfer rate).
- The display controller will then output the video data from the active frame buffer to display device.

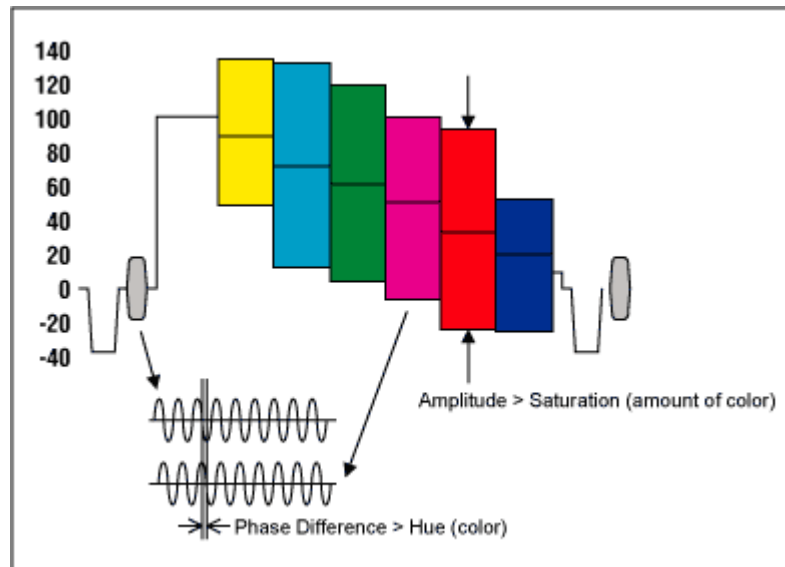
13.8 Video signal format

- Analogue TV video signal formats
 - NTSC (National Television Systems Committee)
 - PAL: phase alternating line
 - SECAM: sequential couleur avec memoire
- Computer video signal is basically modeled from TV video signal
- A typical waveform of an all-white NTSC composite video signal for one scan line is shown in the figure below:

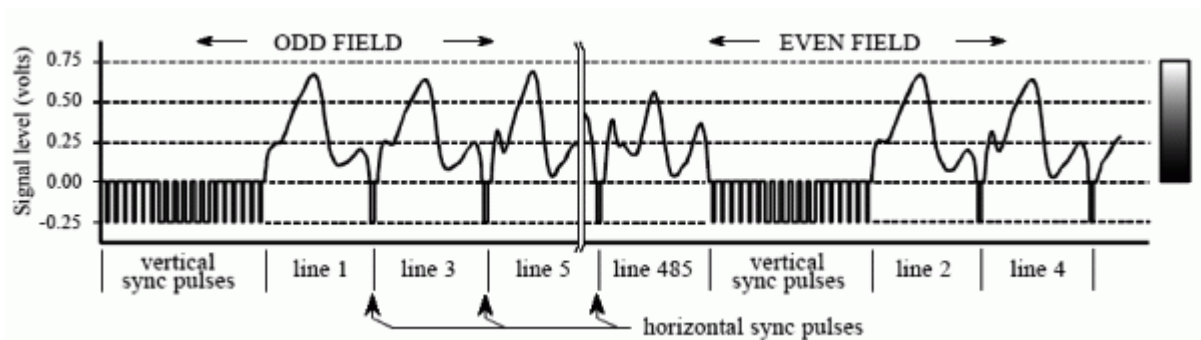


- Each line is made up of the active video portion and the horizontal blanking portion.
- The active video portion contains the picture brightness (luma) and color (chroma) information.
- The brightness information is the instantaneous amplitude at any point in time.
- The horizontal blanking portion would be displayed as black and therefore not seen on the screen.

- Color information is added on top of the luma signal and is a sine wave with the colors identified by a specific phase difference between it and the color-burst reference phase.

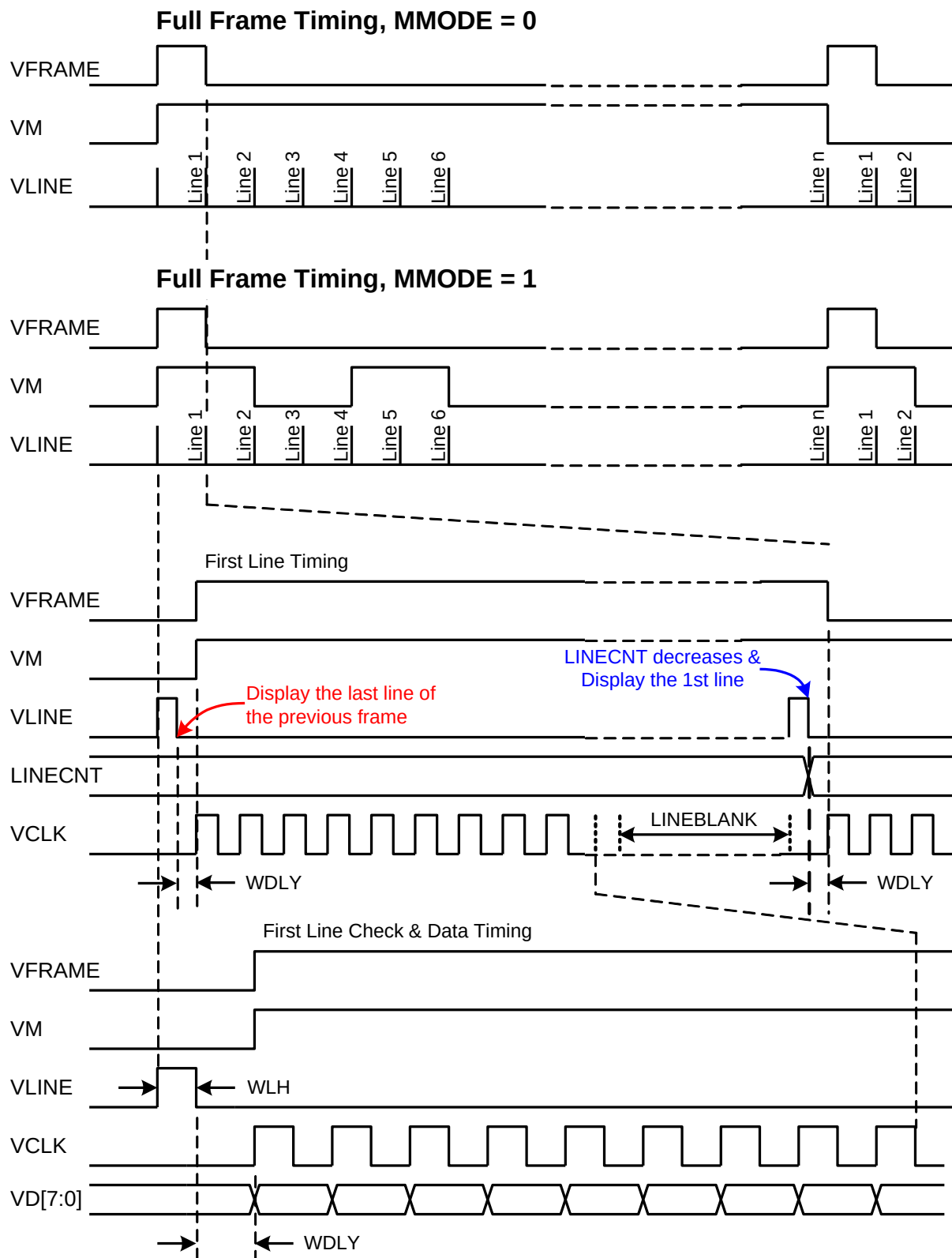


- The following figure shows a frame of video signal.



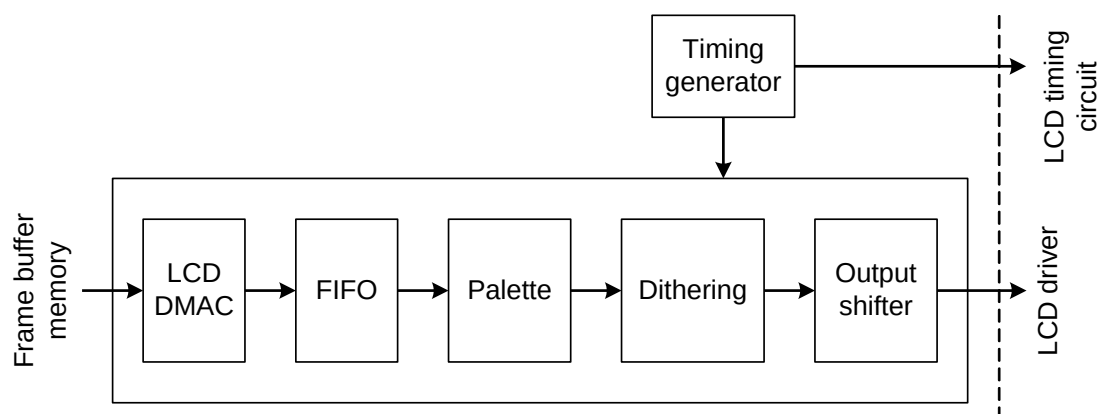
- It involves a lot of redundant sync signals that LCD monitor does NOT require.

- The following figure shows the LCD timing signal for S3C44B0X.



13.9 Video display controller

- Design must consider the display device.
- CRT monitor: DAC converts the data to analog signal.
- LCD panel: controller serializes the data to drive LCD.
- Design is much simpler for one single display mode.
- Complicated design for multiple display modes and programmability makes configuration much easier.
- Monochrome: direct mapping of frame buffer
- Gray level: direct mapping or lookup table with time-based dithering.
- Color STN: color palette selection via lookup table with time-based dithering.
- Color TFT: direct mapping or use color palette.
- Integrated with a timing signal generator to produce horizontal, vertical and frame synchronization pulses; and pixel clock.
- Optional DMA circuit is for speeding up the data transfer from frame buffer to controller.
- A generalized datapath structure of a display controller is shown below.



13.10 S3C44B0X LCD controller

13.10.1 Features

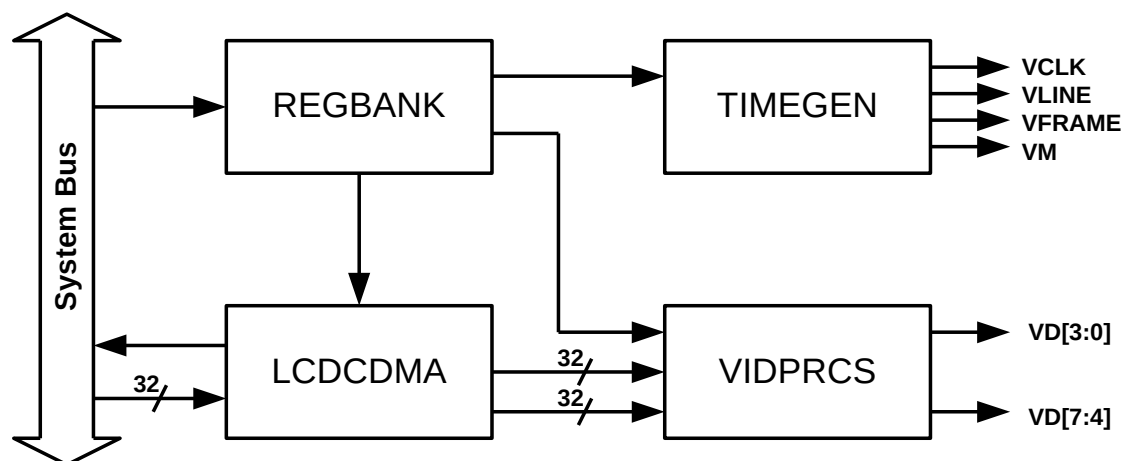
- Supports monochrome LCD panel
- Supports 4 and 16 gray levels LCD panel, using a time-based dithering algorithm and FRC (Frame Rate Control) method.
- Supports 256 level colors STN LCD panel, using TLU (Table Look Up), dithering and FRC method.
- Supports multiple screen size.
Typical actual screen sizes: 640x480, 320x240, 160x160
- Supports Multiple Virtual Display Screen.
Maximum virtual screen sizes (color mode): 4096x1024, 2048x2048, 1024x4096, etc
- Supports 4-bit dual scan, 4-bit single scan, 8-bit single scan LCD panel.
- Uses system memory as the display memory.
- Dedicated DMA to fetch data from video buffer.

13.10.2 Hardware interface signals

- VFRAME: This is the frame synchronous signal between the LCD controller and LCD driver. It signals the LCD panel of the start of a new frame.
- VLINE: This is the line synchronous pulse signal between LCD controller and LCD driver, and it is used by the LCD driver to transfer the contents of it's horizontal line shift register to the LCD panel for display.
- VCLK: This pin is the pixel clock signal between the LCD controller and LCD driver, and data is sent by the LCD controller on the rising edge of VCLK and sampled by LCD driver on the falling edge of VCLK.

- VM: The VM signal is used by the LCD driver to alternate the polarity of the row and column voltage used to turn the pixel on and off.
- VD[3:0]: For a 4-bit or 8-bit single scan display, these 4-bit pixel data are used as the display data. In case of 4-bit dual scan display, these 4-bit plays into its role of the upper display data.
- VD[7:4]: For a 8-bit single scan display, these data are used as upper display data. For a 4-bit dual scan display, these data are used as lower display data.

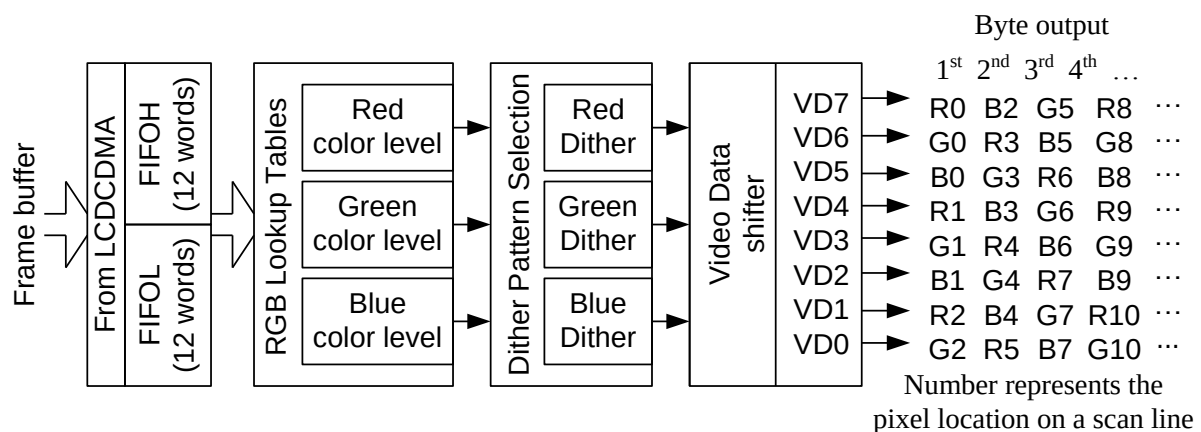
13.10.3 Controller Block diagram



- LCDCDMA is equipped with internal FIFO.
- LCDCDMA fetches data from the frame buffer in burst mode (**4 words at a time**) the FIFO when FIFO is empty or partially empty,
- Two FIFOs, FIFOL and FIFOH, each of 12 words.
- Two FIFOs can support dual scan display mode.
- Only one of the FIFO will be used for single scan mode.
- TIMEGEN generates all timing synchronization signal for driving the LCD panel.
- VIDPRCS is responsible for processing the video data before sending it to the LCD driver.

13.10.4 Video operation

- The VIDPRCS reads the video data from the LCDCDMA and then process them to generate monochrome, gray level and color data stream that will be sent to LCD panel via video data shifter.
- In monochrome (B&W) mode, the video data bypasses the lookup tables and FRC and is directly sent to LCD via video data shifter.
- The following block diagram shows the controller output for 8-bit color STN LCD panel.



- In order to produce good color quality, the frame rate for STN LCD should be, say, in the order of 100 frames/sec.
- Whereas TFT only requires at least about 30 frames/sec.
- Note that TFT does not require dithering and FRC. However, it may go through lookup table if the LCD panel cannot support the color levels dictated by the RGB bit length.

Note that S3C44B0X does not support TFT LCD panel.

13.10.5 An example of interfacing a 8-bit CSTN Panel

NAN YA STN 8-bit color LCD Panel - LCBKET302M2C

Resolution: 640×480

PIN NO.	SYMBOL	FUNCTION
1	FLM	Scan start-up signal
2	VSS	GND
3	CL1	Input data latch signal
4	VSS	GND
5	CL2	Data input clock
6	VSS	GND
7	D0	Display data
8	D1	Display data
9	D2	Display data
10	D3	Display data
11	D4	Display data
12	D5	Display data
13	D6	Display data
14	D7	Display data
15	DISP	Display control signal H: ON , L: OFF
16	VDD	Power supply voltage for logic
17	VDD	Power supply voltage for logic
18	VSS	GND
19	VEE	Power supply voltage for LCD(+)
20	VSS	GND
21	TS1	Temperature sensor pin1
22	TS2	Temperature sensor pin2

FLM: VFRAME (S3C44B0X)

CL1: VLINE (S3C44B0X)

CL2: VCLK (S3C44B0X)

D0-D7: VD[7-0] (S3C44B0X)

The timing diagram illustrates the relationship between clock signals and data bus activity. CL1 is a high-frequency clock, while CL2 is a lower-frequency clock. The data bus (D0-D7) shows a sequence of data transfers, each consisting of a read (R) and a write (B) operation. The data values are shown in hexadecimal format. The diagram is divided into two sections by a dashed line, indicating a continuation of the sequence.

Signal	Time Interval	Value
CL1	0 to 10	High
CL1	10 to 11	Low
CL1	11 to 12	High
CL1	12 to 13	Low
CL1	13 to 14	High
CL1	14 to 15	Low
CL1	15 to 16	High
CL1	16 to 17	Low
CL1	17 to 18	High
CL1	18 to 19	Low
CL1	19 to 20	High
CL1	20 to 21	Low
CL1	21 to 22	High
CL1	22 to 23	Low
CL1	23 to 24	High
CL1	24 to 25	Low
CL1	25 to 26	High
CL1	26 to 27	Low
CL1	27 to 28	High
CL1	28 to 29	Low
CL1	29 to 30	High
CL1	30 to 31	Low
CL1	31 to 32	High
CL1	32 to 33	Low
CL1	33 to 34	High
CL1	34 to 35	Low
CL1	35 to 36	High
CL1	36 to 37	Low
CL1	37 to 38	High
CL1	38 to 39	Low
CL1	39 to 40	High
CL1	40 to 41	Low
CL1	41 to 42	High
CL1	42 to 43	Low
CL1	43 to 44	High
CL1	44 to 45	Low
CL1	45 to 46	High
CL1	46 to 47	Low
CL1	47 to 48	High
CL1	48 to 49	Low
CL1	49 to 50	High
CL1	50 to 51	Low
CL1	51 to 52	High
CL1	52 to 53	Low
CL1	53 to 54	High
CL1	54 to 55	Low
CL1	55 to 56	High
CL1	56 to 57	Low
CL1	57 to 58	High
CL1	58 to 59	Low
CL1	59 to 60	High
CL1	60 to 61	Low
CL1	61 to 62	High
CL1	62 to 63	Low
CL1	63 to 64	High
CL1	64 to 65	Low
CL1	65 to 66	High
CL1	66 to 67	Low
CL1	67 to 68	High
CL1	68 to 69	Low
CL1	69 to 70	High
CL1	70 to 71	Low
CL1	71 to 72	High
CL1	72 to 73	Low
CL1	73 to 74	High
CL1	74 to 75	Low
CL1	75 to 76	High
CL1	76 to 77	Low
CL1	77 to 78	High
CL1	78 to 79	Low
CL1	79 to 80	High
CL1	80 to 81	Low
CL1	81 to 82	High
CL1	82 to 83	Low
CL1	83 to 84	High
CL1	84 to 85	Low
CL1	85 to 86	High
CL1	86 to 87	Low
CL1	87 to 88	High
CL1	88 to 89	Low
CL1	89 to 90	High
CL1	90 to 91	Low
CL1	91 to 92	High
CL1	92 to 93	Low
CL1	93 to 94	High
CL1	94 to 95	Low
CL1	95 to 96	High
CL1	96 to 97	Low
CL1	97 to 98	High
CL1	98 to 99	Low
CL1	99 to 100	High
CL1	100 to 101	Low
CL1	101 to 102	High
CL1	102 to 103	Low
CL1	103 to 104	High
CL1	104 to 105	Low
CL1	105 to 106	High
CL1	106 to 107	Low
CL1	107 to 108	High
CL1	108 to 109	Low
CL1	109 to 110	High
CL1	110 to 111	Low
CL1	111 to 112	High
CL1	112 to 113	Low
CL1	113 to 114	High
CL1	114 to 115	Low
CL1	115 to 116	High
CL1	116 to 117	Low
CL1	117 to 118	High
CL1	118 to 119	Low
CL1	119 to 120	High
CL1	120 to 121	Low
CL1	121 to 122	High
CL1	122 to 123	Low

[illegible]

13.10.6 Bus load

- A dedicated DMA for LCD controller is used to transfer video data from frame buffer (main memory) to the FIFO of the LCDDMA when the FIFO is not full.
- LCDDMA will transfers 4 words (16 bytes) each time
- DMA burst length (BL) depends on data bus width
 - 8-bit (equivalent to 1 byte) : $BL = 16/1 = 16$
 - 16-bit (equivalent to 2 bytes) : $BL = 16/2 = 8$
 - 32-bit (equivalent to 4 bytes) : $BL = 16/4 = 4$
- When DMA occurs, system bus cannot be used by other devices.
- CPU needs to refresh the LCD screen continuously according to the refresh rate and this creates bus loading and consumes CPU processing time.
- The higher the bus load, the slower the CPU performance.
- The bus load is the percentage of time occupied by the bus to transfer the video data.
- Since the screen the being continuously refreshed and it is natural to measure this index in an interval related to the frame rate.

$$\text{bus load} = \frac{\text{time required to transfer the video data}}{\text{time interval}}$$

Example:

160 x 160pixel, 4-level gray, 80 frame/sec,
 4-bit single scan display, system clock frequency = 66 MHz,
 LCD frame buffer = SDRAM, Bus width = 16-bit.

4-level gray → 2 bits/pixel

Video data per frame:

$$160 \times 160 \times 2 = 51200 \text{ bits} = 6400 \text{ bytes}$$

Data from SDRAM to LCD controller in 1 second for FR=80:

$$6400 \times 80 = 512000 \text{ bytes/s} = 256000 \text{ hws/s} = 128000 \text{ words/s}$$

For 8-bit data bus, the burst length for each DMA transfer is 16 and the no. of DMA transfer required for 1 second is:

$$512000/16 = 32000$$

No. of SCLK required for each DMA transfer:

$$\text{Trp}(=2\text{clk}) + \text{Trcd}(=2\text{clk}) + \text{CL}(=2\text{clk}) + \text{LCDDMABL}(=16\text{clk}) \\ = 22 \text{ cycles}$$

$$\text{No. of SCLK clock cycles required for 1 second} = 32000 \times 22 \\ = 704000$$

SCLK is same bus clock (66 MHz), therefore:

$$\text{bus load} = \frac{704000}{66 \times 10^6} \times 100\% = 1.07\%$$

For 16-bit data bus, the burst length for each DMA transfer is 8 and the no. of DMA transfer required for 1 second is:

$$256000/8 = 32000$$

No. of SCLK required for each DMA transfer:

$$\text{Trp}(=2\text{clk}) + \text{Trcd}(=2\text{clk}) + \text{CL}(=2\text{clk}) + \text{LCDDMABL}(=8\text{clk}) \\ = 14 \text{ cycles}$$

$$\text{No. of SCLK clock cycles required for 1 second} = 32000 \times 14 \\ = 448000$$

SCLK is same bus clock (66 MHz), therefore:

$$\text{bus load} = \frac{448000}{66 \times 10^6} \times 100\% = 0.68\%$$

For 32-bit data bus, the burst length for each DMA transfer is 4 and the no. of DMA transfer required for 1 second is:

$$128000/4 = 32000$$

No. of SCLK required for each DMA transfer:

$$\text{Trp}(=2\text{clk}) + \text{Trcd}(=2\text{clk}) + \text{CL}(=2\text{clk}) + \text{LCDDMABL}(=4\text{clk}) \\ = 10 \text{ cycles}$$

$$\text{No. of SCLK clock cycles required for 1 second} = 32000 \times 10 \\ = 320000$$

SCLK is same bus clock (66 MHz), therefore:

$$\text{bus load} = \frac{320000}{66 \times 10^6} \times 100\% = 0.48\%$$

Note: the no of BL is NOT equal to the BL of the SDRAM, it is actually dependent on the data bus width of the system, i.e. 8, 16 or 32 bit.

The BL value is stored to the count register of the LCDDMA controller.

LCDDMA always transfer 4 words (8 hwords or 16 bytes) at a time, thus:

From the above example, it is shown that the no of LCDDMA transfer for one second remains unchanged and only the time taken (BL) for each DMA transfer mastership is different.

Since the bus load is directly related to the screen size, and the CPU performance will be degraded if a higher resolution screen is used with the same refresh rate.

Reducing the refresh rate helps improving the performance, screen flickering may however appear.

In addition, the system data bus width also affects the CPU performance as well.