

Chapter 10 Memory System - Timing Design

Computer system requires a memory system to store program and data for operation and it generally consists of main memory and secondary system.

Main memory system is usually consists of read only memory devices and read/write memory device; and the memory location can be randomly accessible – any byte of memory can be accessed without touching the preceding bytes.

Read only memory:

- Nonvolatile memory - hold data without power supply.
- ROM, EPROM and EEPROM – old generation devices.
- Usually for storing a boot-up program to initialize the system.
- Flash ROM (NOR Flash) is a common replacement for its on-line re-programmable convenience.

Read only memory = RAM

Read/write memory:

- Volatile memory – cannot hold data without power supply.
- CPU will access instruction store in memory and read/write data from/to memory directed by the application program.
- Static Random Access Memory (SRAM), dynamic RAM (DRAM) and synchronous DRAM (SDRAM)

Note that ROM, EPROM, EEPROM and NOR Flash are also randomly access memory devices, but they are read only devices. Read/write memory devices are traditionally called RAM.

This chapter deals with the timing design of read/write random access based memory system including SRAM and SDRAM.

need high power to keep awake

10.1 Random Access Memory (RAM) devices

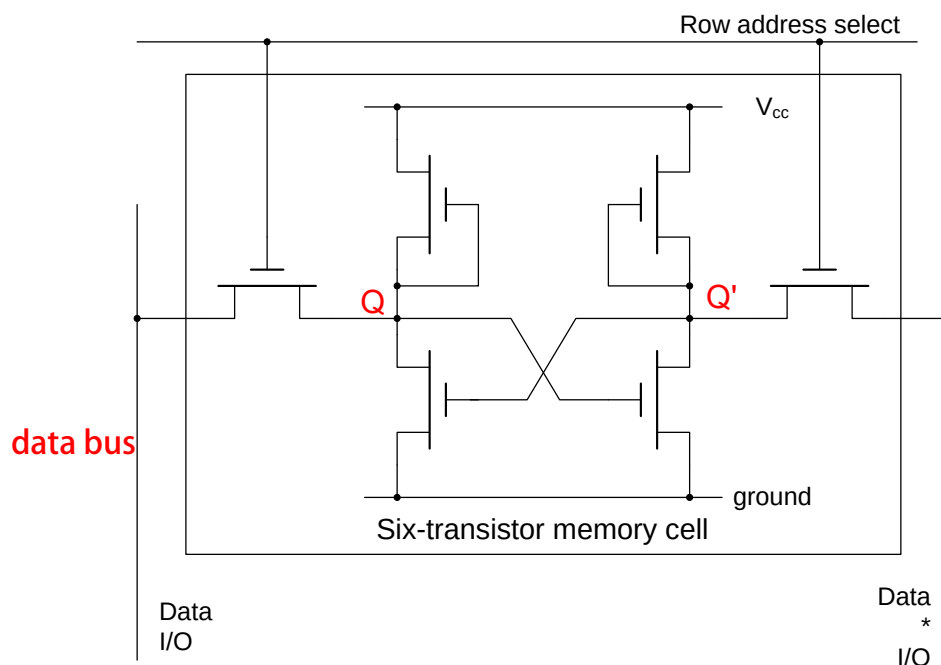
There are two basic types of RAM:

Static RAM (SRAM): use a six-transistor bistable circuit to store data.

Advantages: high speed and simple interface circuit.

Disadvantages: high power dissipation and lower memory density.

Application: high speed data access such as cache for its fast access time.



Circuit of a SRAM memory cell

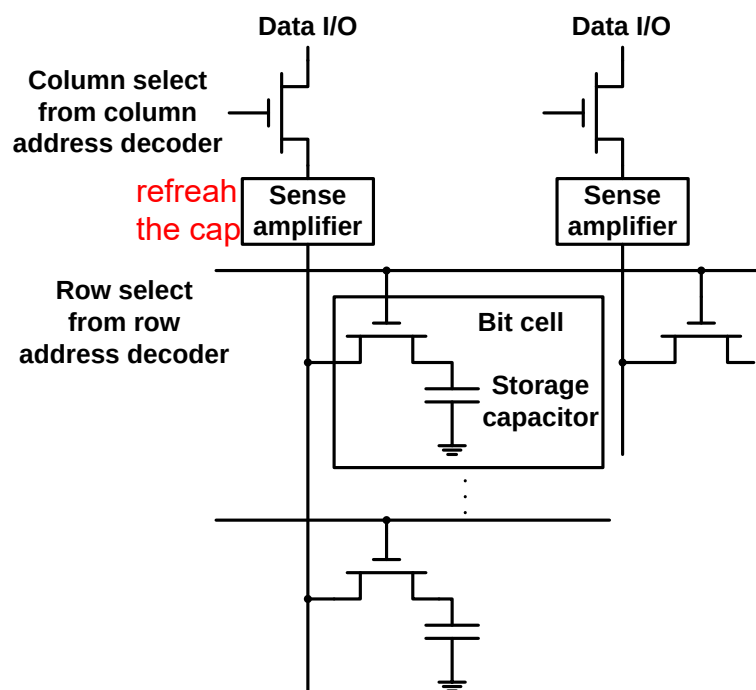
need very low power
but slow

Dynamic RAM (DRAM): use a single transistor cell together with a storage capacitor to store data.

Advantages: low power dissipation and higher memory density.

Disadvantages: low speed and require refresh circuit to maintain the data.

Application: system with a large memory size requirement due to its relatively low cost.



Circuit of a DRAM memory cell

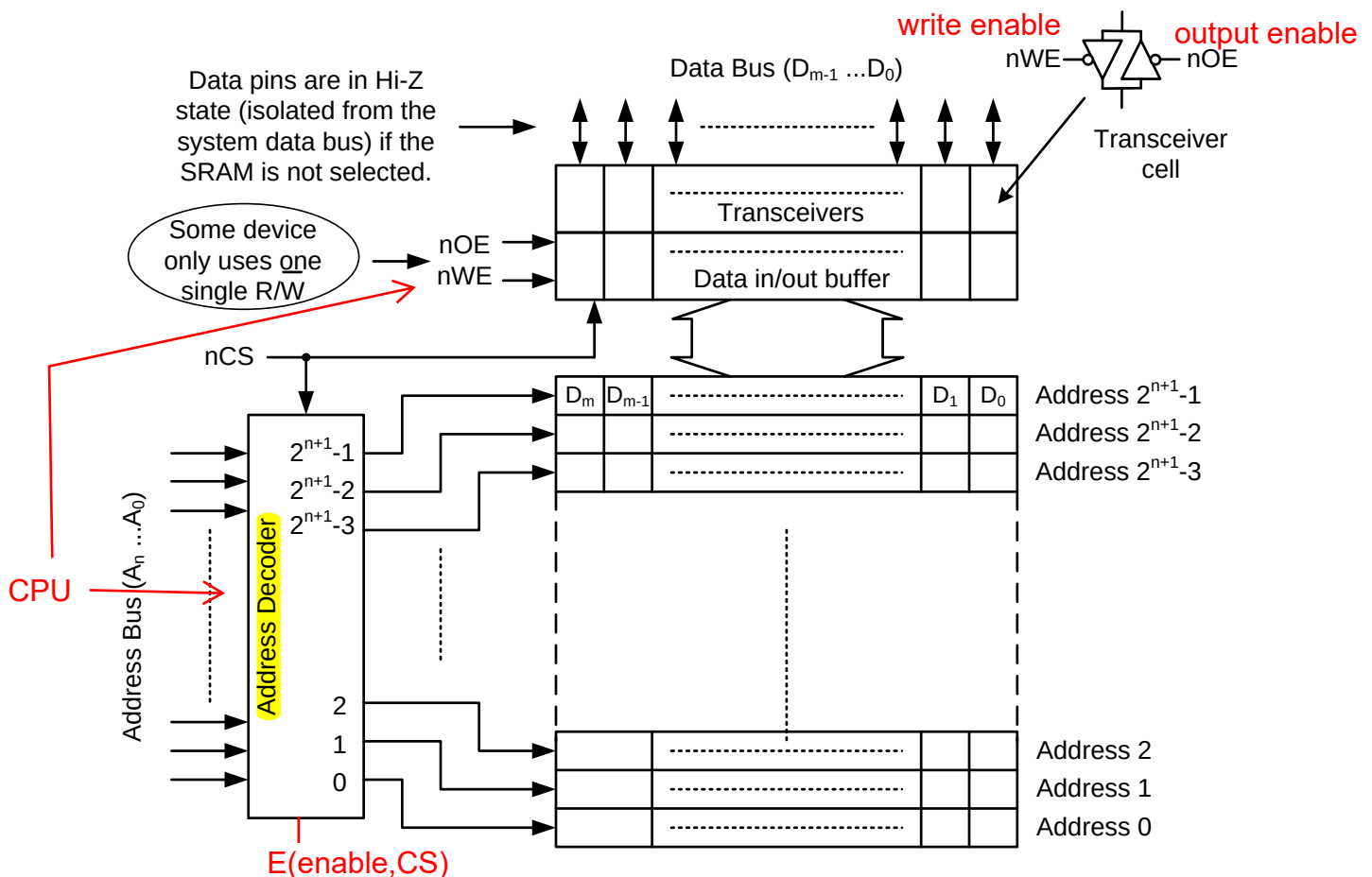
It uses nRAS Row Address Strobe signal to select a page (a entire row of bit cells), and the uses a column address strobe signal to select the bit cell.

Since the charge stored in the storage capacitor fades as time goes by, the memory cell must be refreshed periodically.

The sense amplifier will recharge the capacitor when the cell is refreshed (basically a read operation of a row address to increase the number of cell being recharged).

10.2 Read/Write process of SRAM

The general structure of a SRAM is shown below:



Read process:

- SRAM receives the address from the system address bus and decodes for the required memory location;
- When the nCS is asserted "0", then the data stored in the corresponding address will be placed onto the data I/O buffer;
- When nOE is asserted to "0", the data will be placed onto the system data bus;
- After CPU read the data, nOE and nCS will be de-asserted followed by the removal of address information from the system address bus.

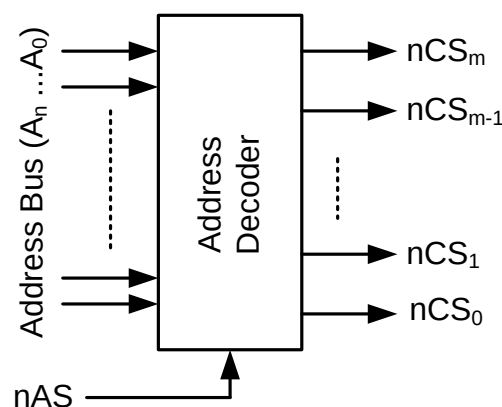
Write process:

- SRAM receives the address from the system address bus and decodes for the memory location;
- CPU may place data onto the system data bus soon after placing the address onto the system address bus;
- When the nCS is asserted “0”, then the corresponding memory location will be connected to the data in/out buffer;
- When nWE is asserted “0”, the data will be placed onto the data in/out buffer;
- After a prescribed time, the data is latched to the corresponding memory location;
- CPU removes the nWE, nCS followed by the data and address control signal, data and address information from the system buses.

NOTE:

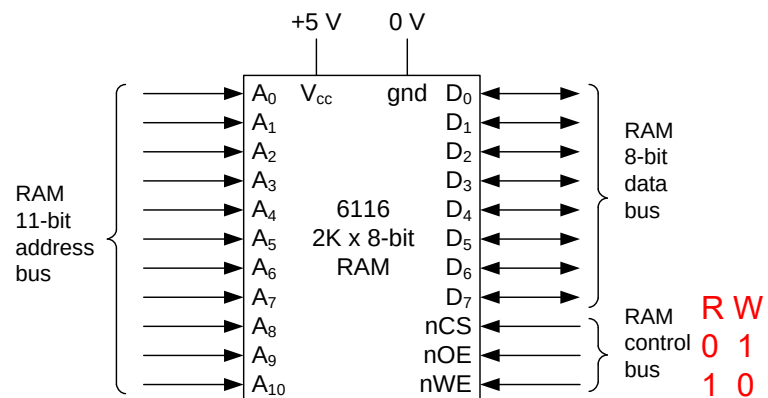
CPU **DOES NOT** usually generate the nCS signal and it only provides some kinds of address valid signal, may be called Address Strobe (nAS).

The nCS is usually generated as a combination of nAS and address ($A_{n-1}A_{n-2} \cdots A_1A_0$).

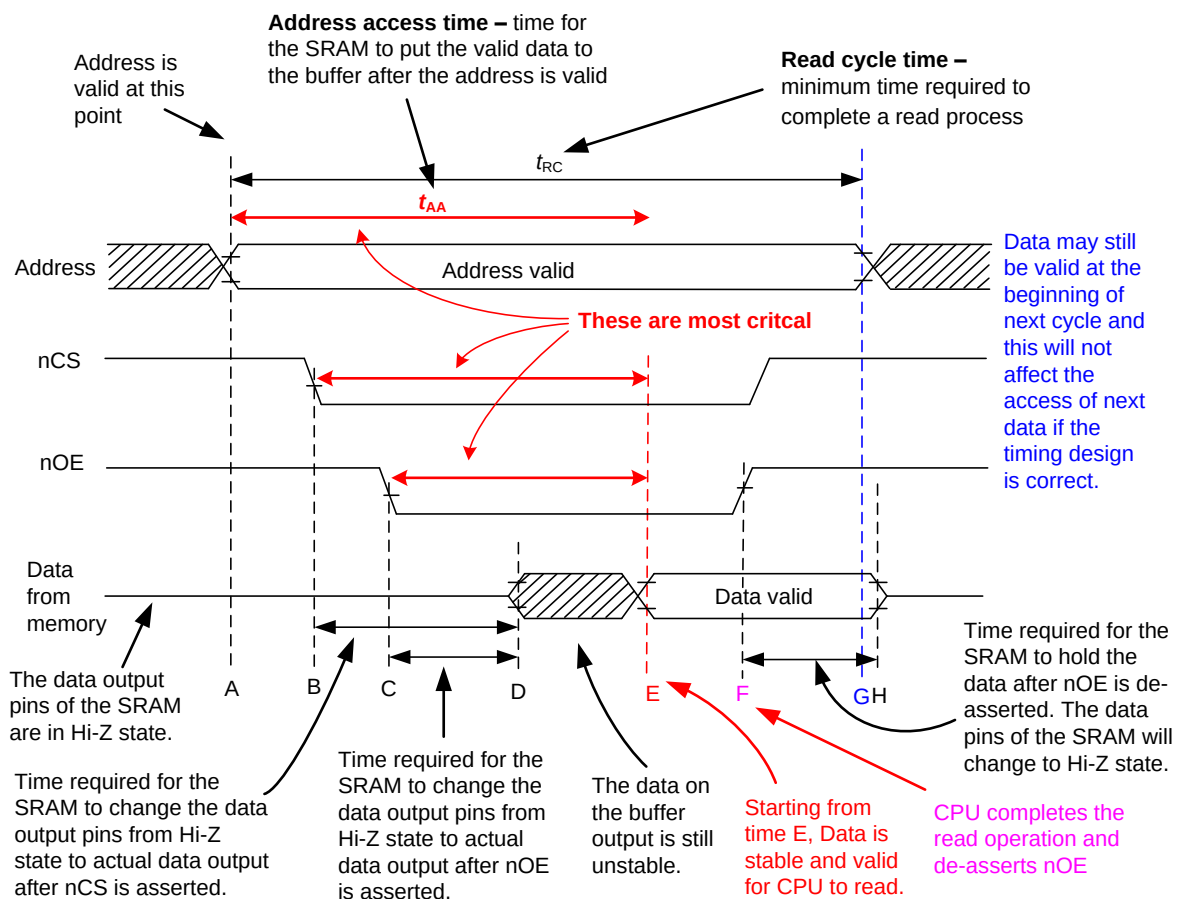


10.3 Access Timing of SRAM – An example

Static RAM 6116
(2 K x 8-bit)



Read cycle timing

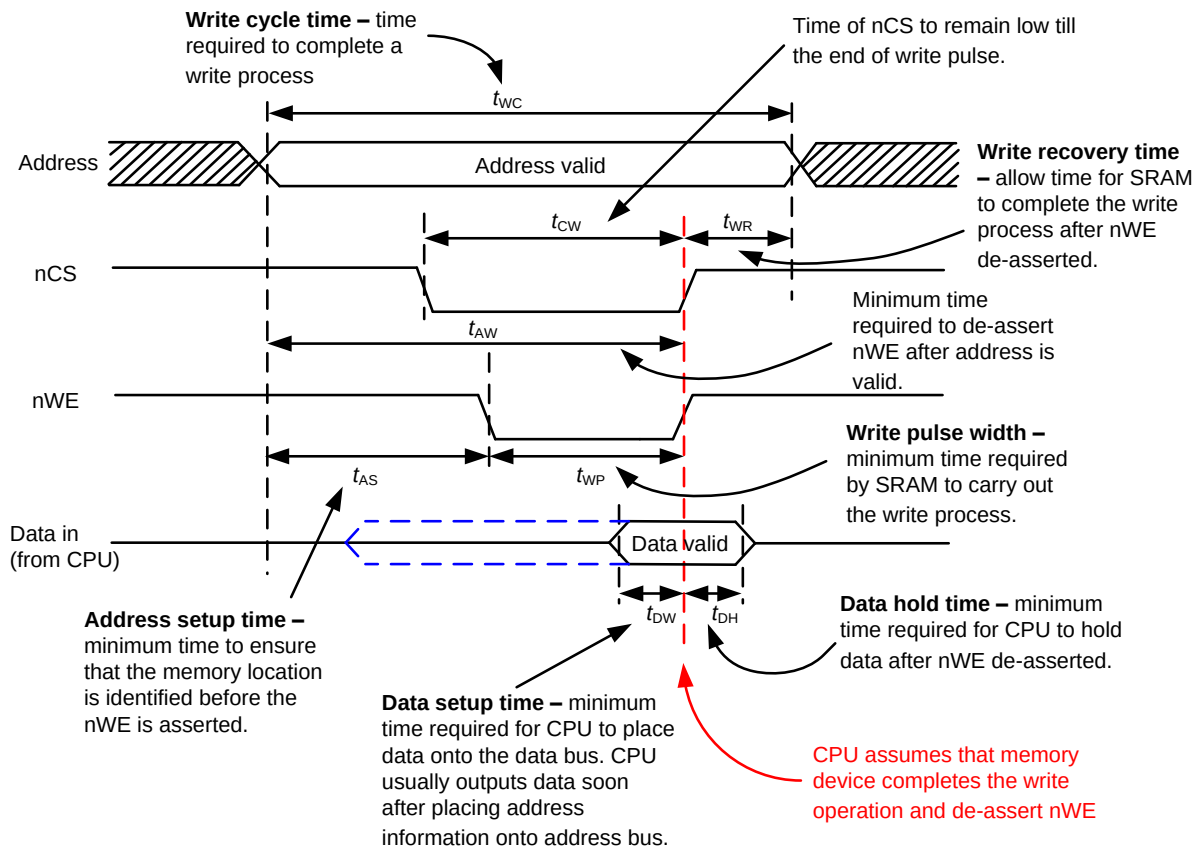


The speed of the SRAM is largely depends on how fast is the address access time: t_{AA} .

Valid Data is only available at point **E** for CPU to read and nOE **MUST NOT** be de-asserted before this point.

CPU ends the READ operation at point **F**.

Write cycle timing



Most important points:

Write pulse – CPU cannot de-assert nWE if SRAM has not latched the data into the memory location.

Data setup time – minimum time required for CPU to present valid data to SRAM prior to the end of the write pulse.

Most SRAM timing diagrams are very similar, but with different labels for various timing parameters. The key is to determine the reference points in the read and write cycle timing diagrams.

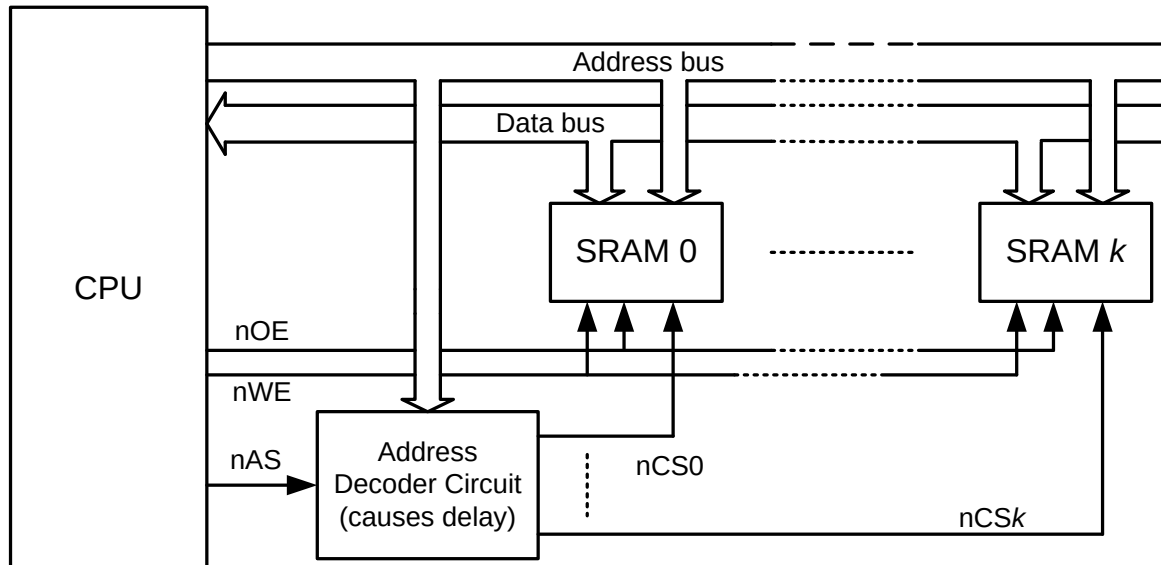
Read cycle: the time point when data is valid for CPU to read.

Write cycle: the time point (end of write pulse) that the SRAM already latches the data into memory location.

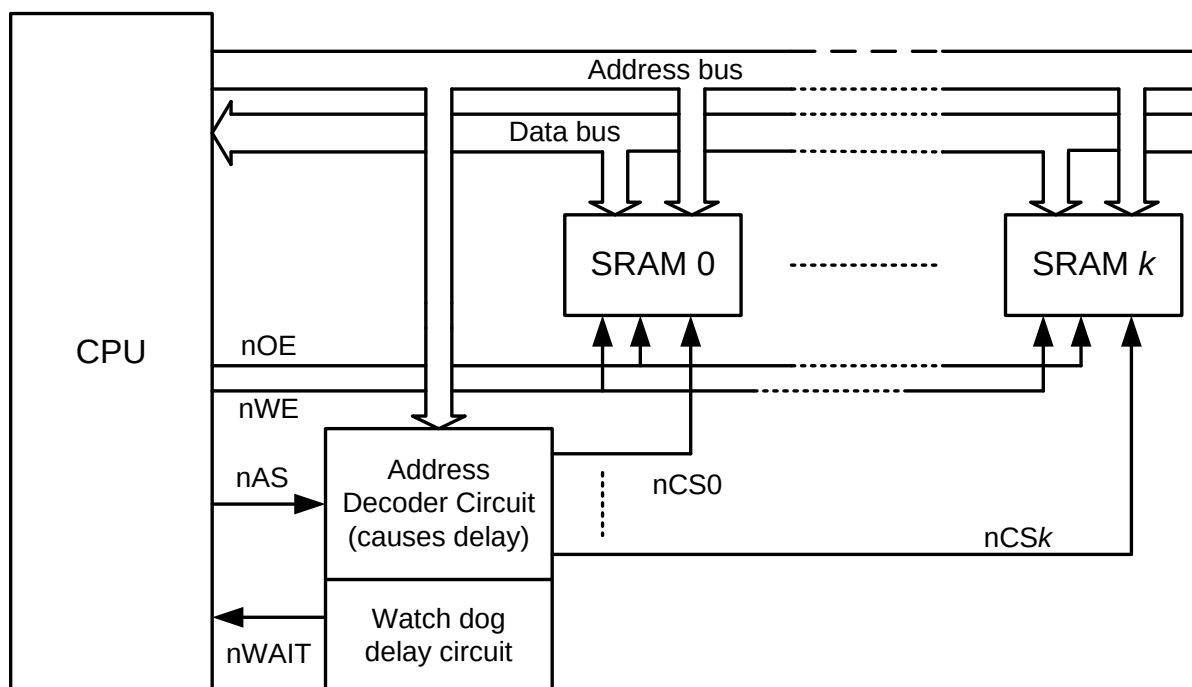
To ensure valid transfer between CPU and memory devices, the timing design **MUST** fulfill **BOTH** the read and write timing requirement.

10.4 Synchronous bus and asynchronous bus design

Synchronous bus design: the read/write operation must be completed within a specific number of clock cycles.

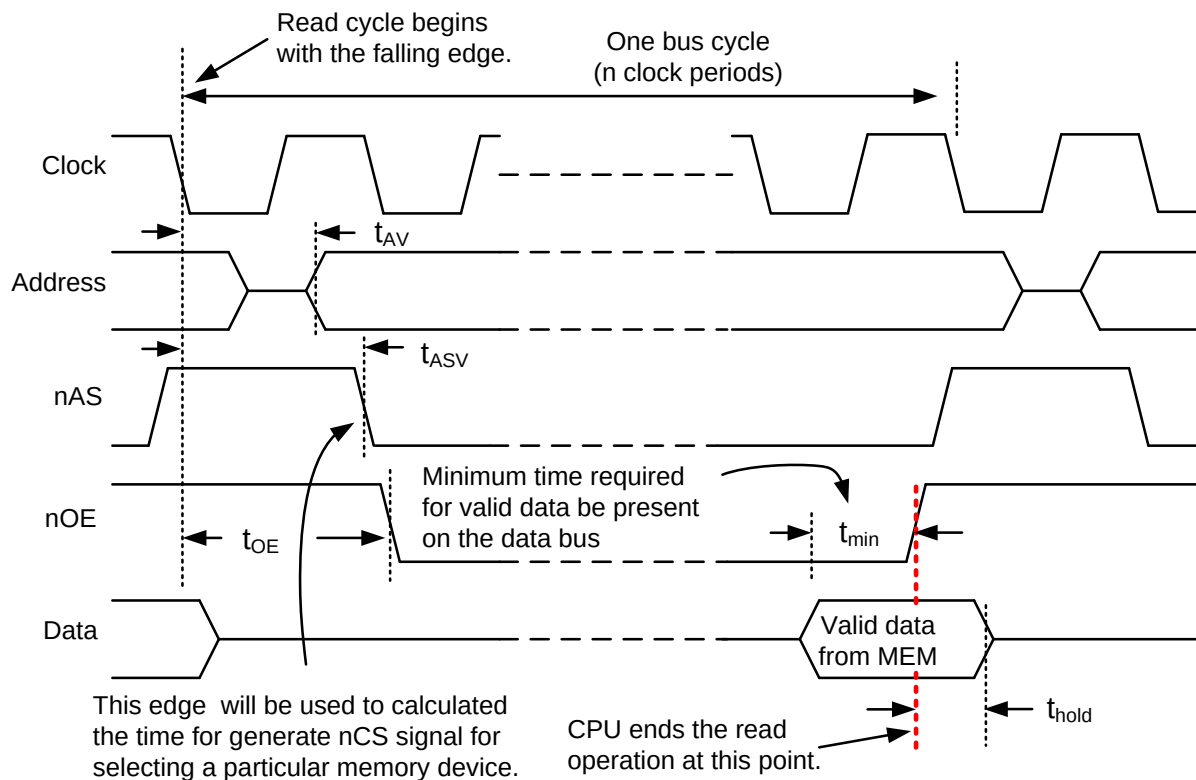


Asynchronous bus design: memory system must inform CPU upon completion of the read/write operation by an additional signal, e.g. nWAIT (memory wait signal) generated by a delay circuit and the delay is sufficient to warrant the read/write operation.



10.5 Typical CPU read cycle timing – An example

Read cycle timing for synchronous operation:



The read cycle takes n clock cycles to complete.

t_{av} : time for address becomes valid

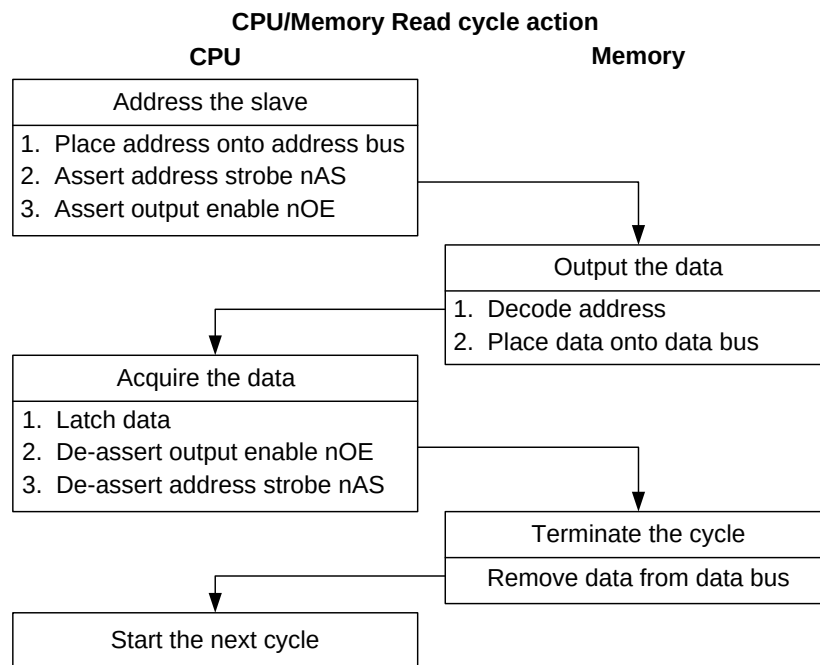
t_{asv} : time for address strobe becomes valid

t_{OE} : time for nOE becomes valid

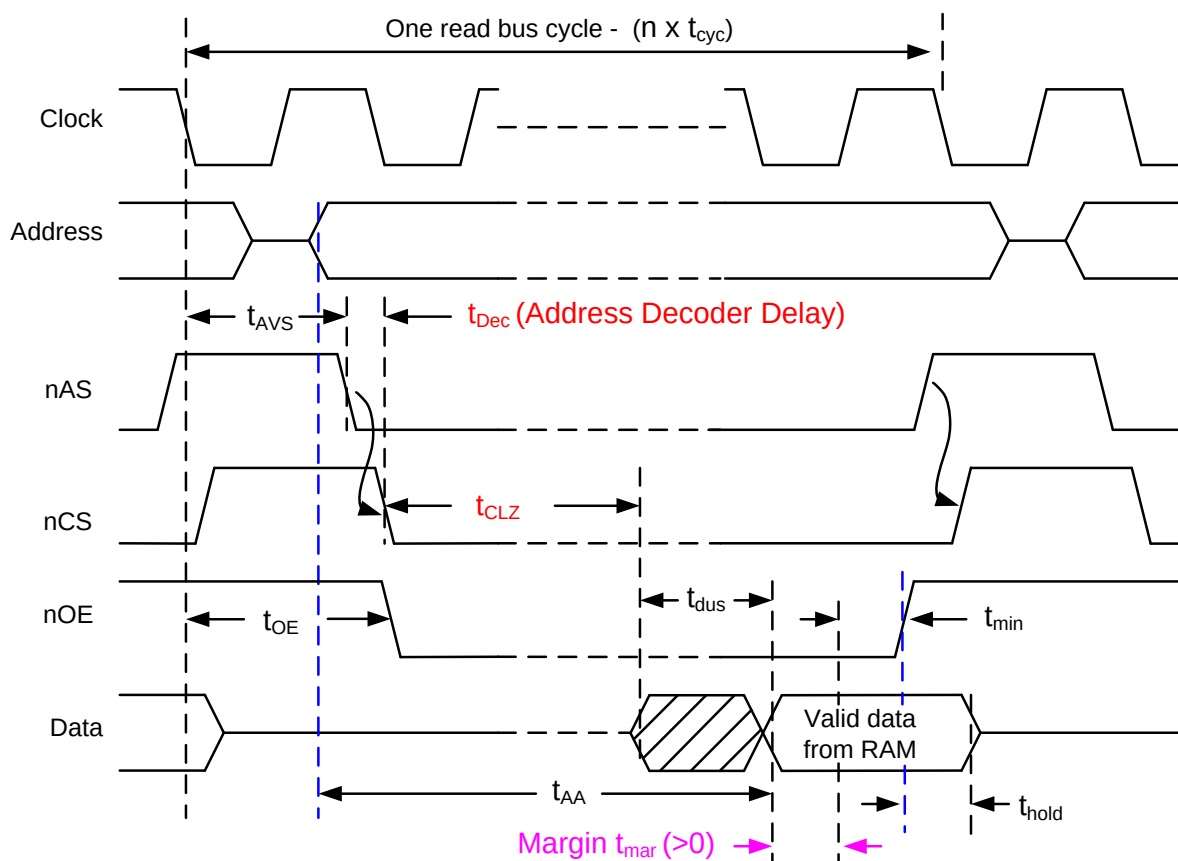
t_{min} : minimum time for valid data before CPU reads it (kind of data set-up time for CPU)

The timing design must guarantee that memory device places valid data onto the data bus for t_{min} prior to the end of nOE.

t_{hold} : hold time for data after CPU reads it



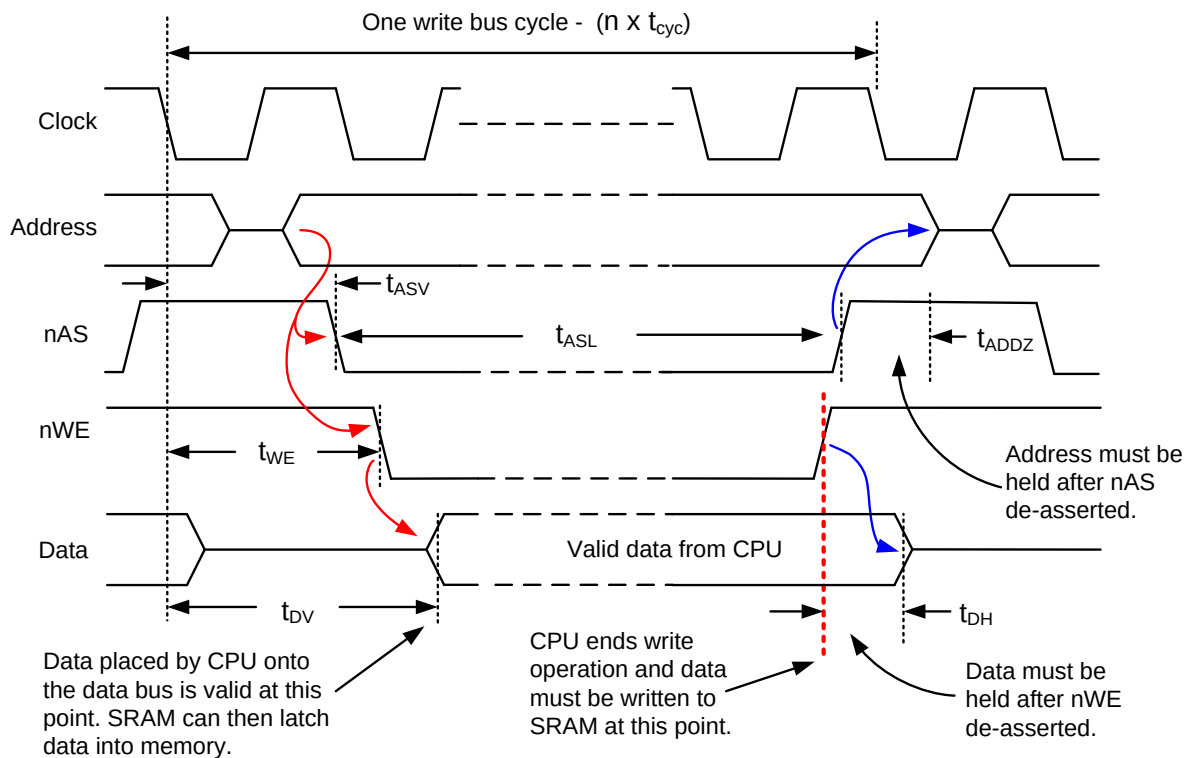
Combined CPU – SRAM synchronous read cycle timing:



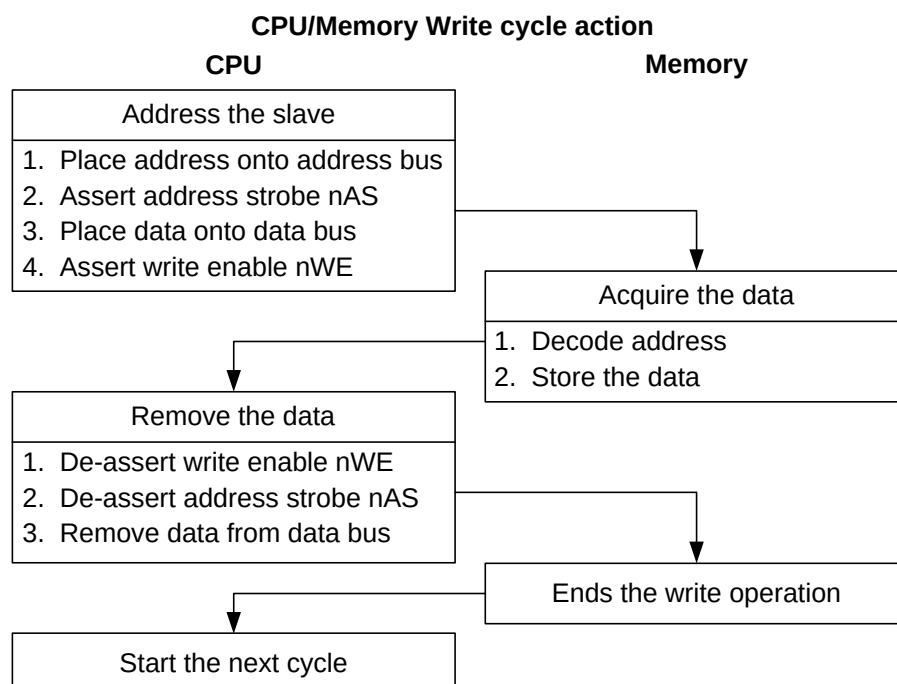
t_{Dec} is the address decoder circuit delay.

The goal is to design an interface circuit such that the margin t_{mar} should be > 0 .

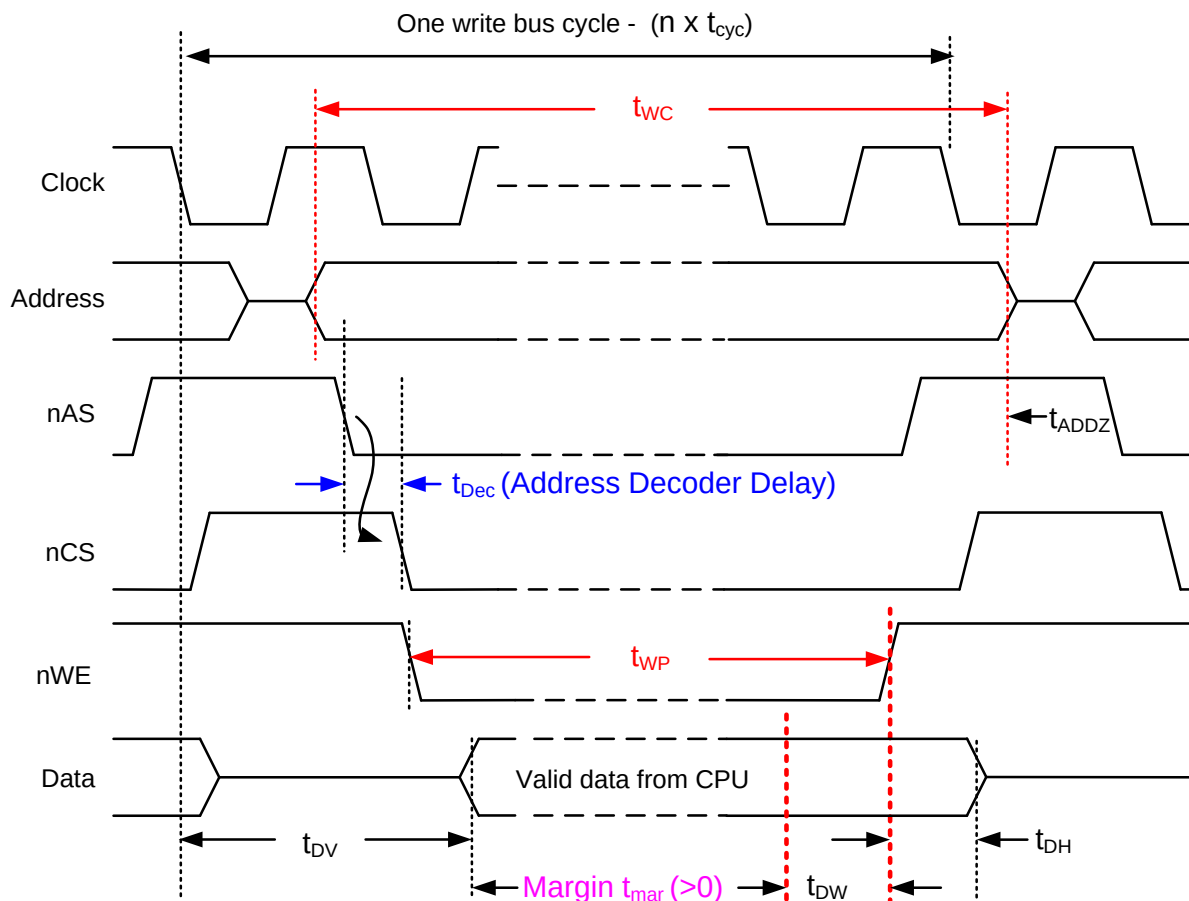
10.6 Typical CPU write cycle timing – An example



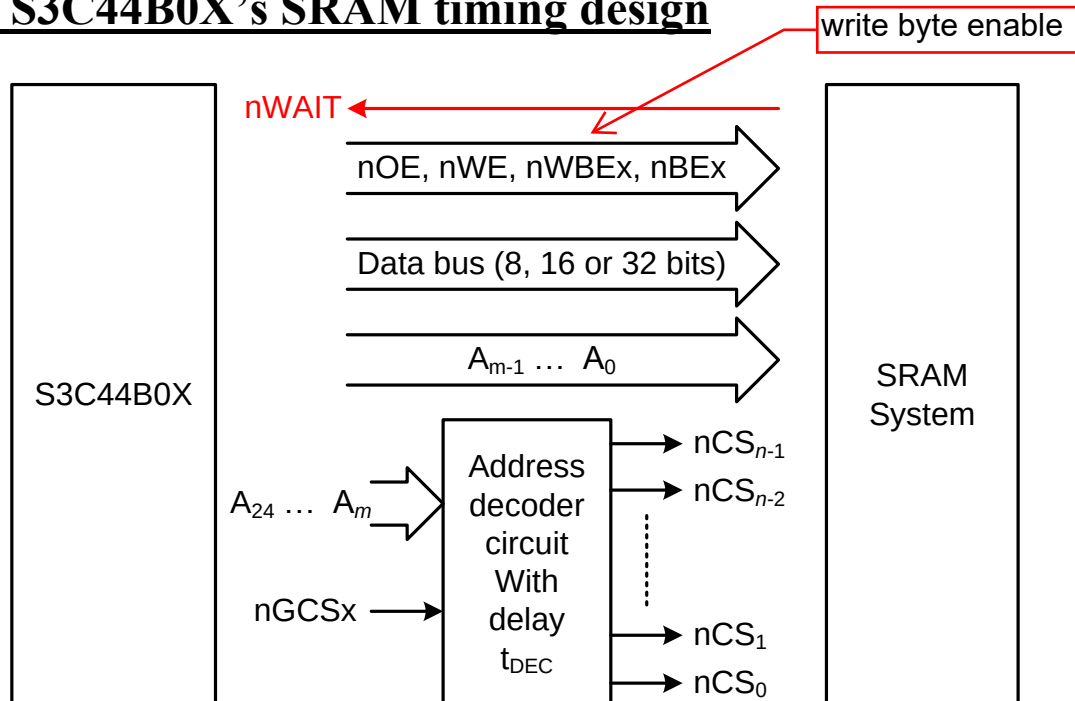
The timing design needs to ensure that data **MUST** be written into the memory location at the end of the write pulse, i.e., when nWE is de-asserted.



Combined CPU – SRAM synchronous write cycle timing:

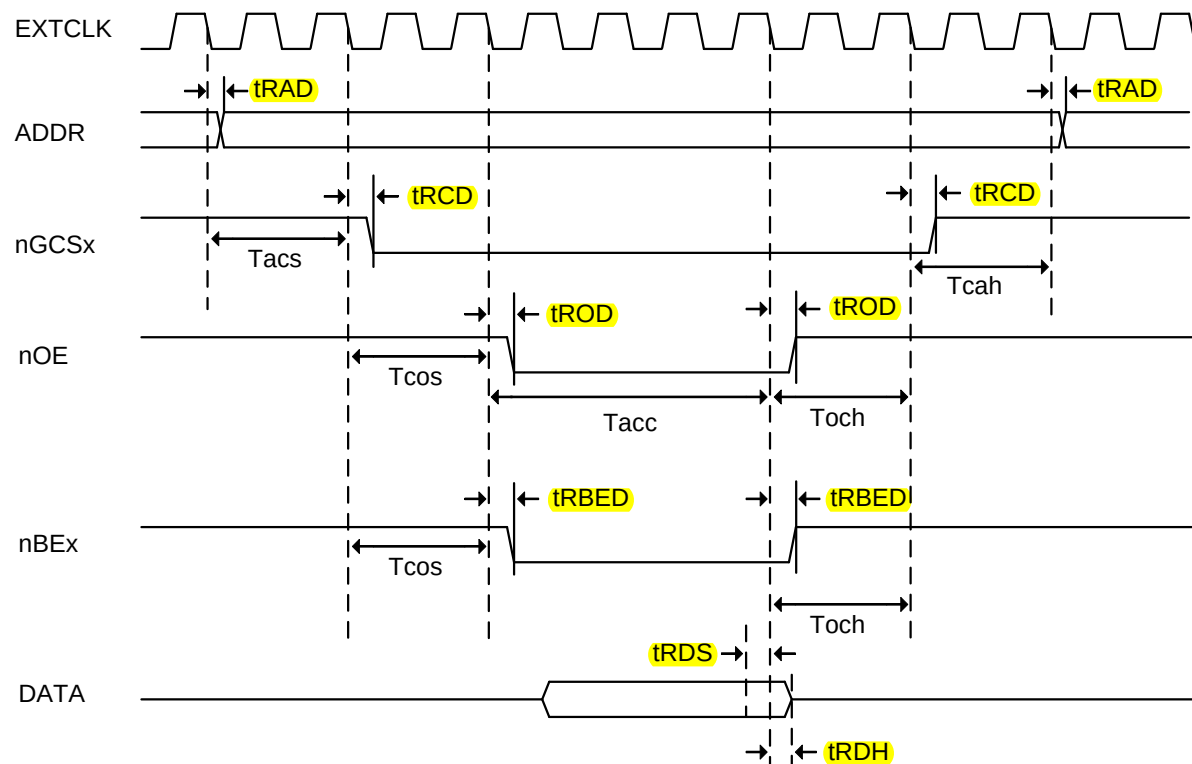


10.7 S3C44B0X's SRAM timing design



nWAIT is for asynchronous bus design for very slow memory devices and is not used for synchronous bus design.

10.7.1 Read cycle

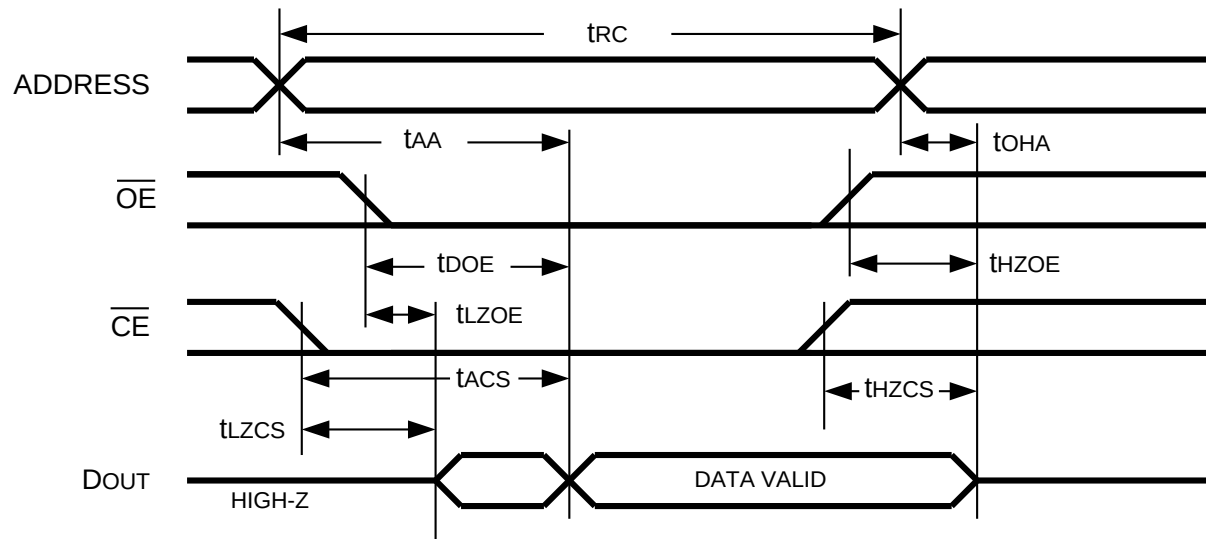


ROM/SRAM READ Timing (I)
 (Tacs=2, Tcos=2, Tacc=4, Toch=2, Tcah=2, PMC=0, ST=0)

ROM/SRAM Bus Timing Constants

(VDDP: 3.3V, VDDI: 2.5V, Ta = 25°C, PLCAP = 70pf, **max/min = typ ± 30%**)

Parameter	Symbol	Min	Typ (ns)	Max
ROM/SRAM Address Delay	tRAD	–	12	–
ROM/SRAM Chip select Delay	tRCD	–	11	–
ROM/SRAM Output enable Delay	tROD	–	11	–
ROM/SRAM read Data Setup time.	tRDS	–	1	–
ROM/SRAM read Data Hold time.	tRDH	–	5	–
ROM/SRAM Byte Enable Delay	tRBED	–	13	–
ROM/SRAM Write Byte Enable Delay	tRWBED	–	14	–
ROM/SRAM output Data Delay	tRDD	–	14	–
ROM/SRAM external Wait Setup time	tWS	–	1	–
ROM/SRAM external Wait Hold time	tWH	–	5	–
ROM/SRAM Write enable Delay	tRWD	–	14	–



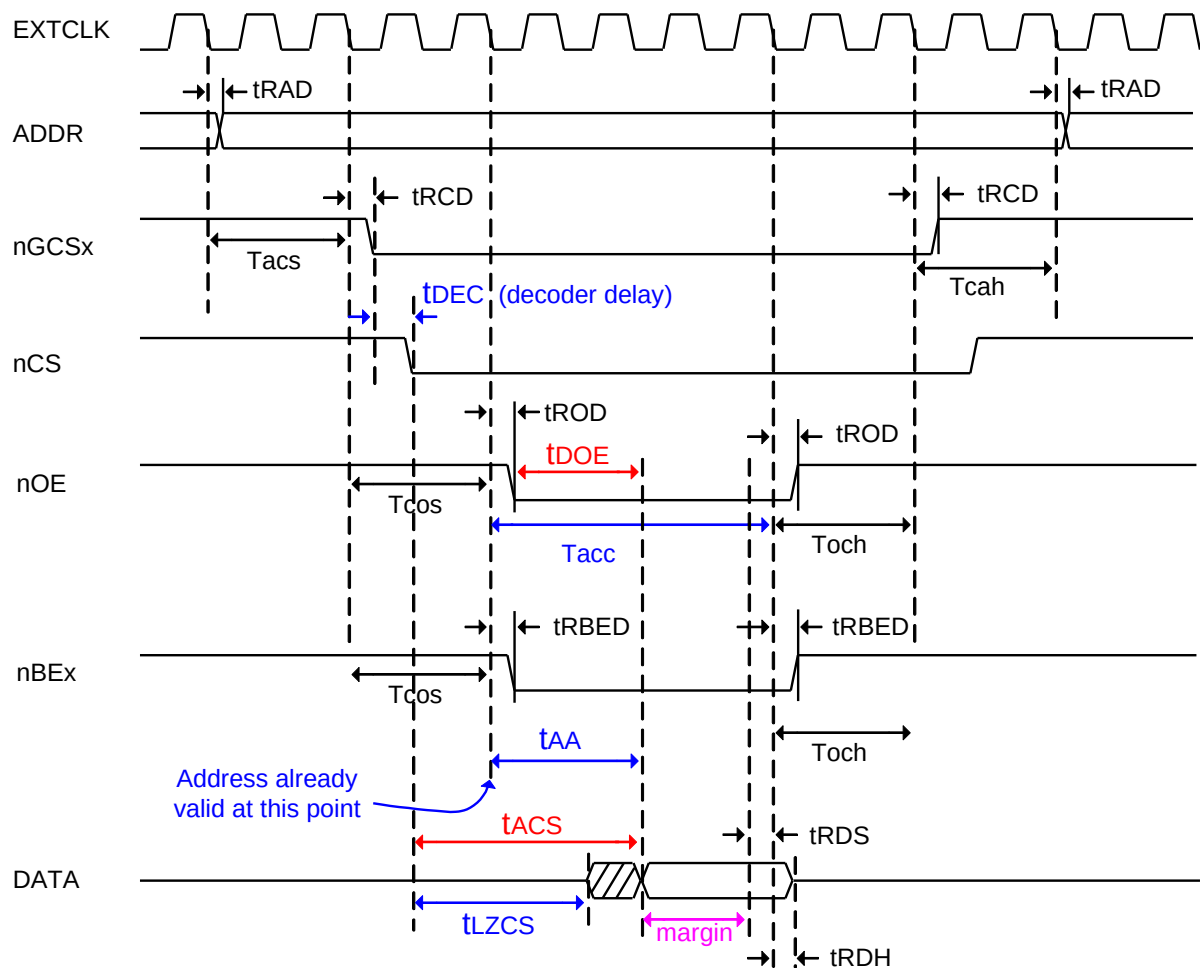
IS65C256AL SRAM read cycle timing diagram

Symbol	Parameter	25 ns		45 ns	
		Min.	Max.	Min.	Max.
tRC	Read Cycle Time	25	—	45	—
tAA	Address Access Time	—	25	—	45
tOHA	Output Hold Time	2	—	2	—
tACS	CE Access Time	—	25	—	45
tDOE	OE Access Time	—	13	—	25
tLZOE(2)	OE to Low-Z Output	0	—	0	—
tHZOE(2)	OE to High-Z Output	0	12	0	20
tLZCS(2)	CE to Low-Z Output	3	—	3	—
tHZCS(2)	CE to High-Z Output	0	12	0	20
tPU(3)	CE to Power-Up	0	—	0	—
tPD(3)	CE to Power-Down	—	20	—	30

IS65C256AL 32K x 8 SRAM read cycle timing parameters

First Design: Not preferable – longer access time

Combined CPU-SRAM read cycle timing diagram



We don't need to consider t_{ACS} and t_{LZCS} if chip select signal nCS is asserted before nOE is asserted (this is to say the decoder delay must be short enough to guarantee this condition). For memory access time, we have

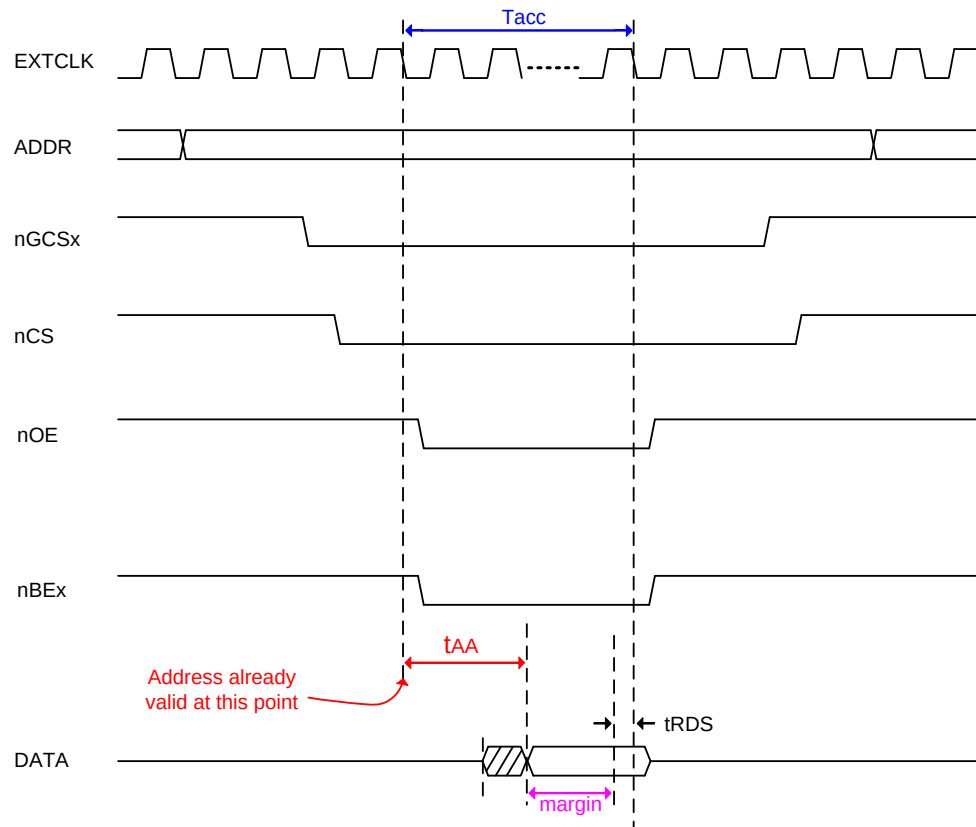
$$t_{AA} + \text{margin} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$\text{i.e., } T_{acc} \geq (t_{AA} + t_{RDS}) / t_{cyc} \quad (\text{Margin}_{\min} = 0)$$

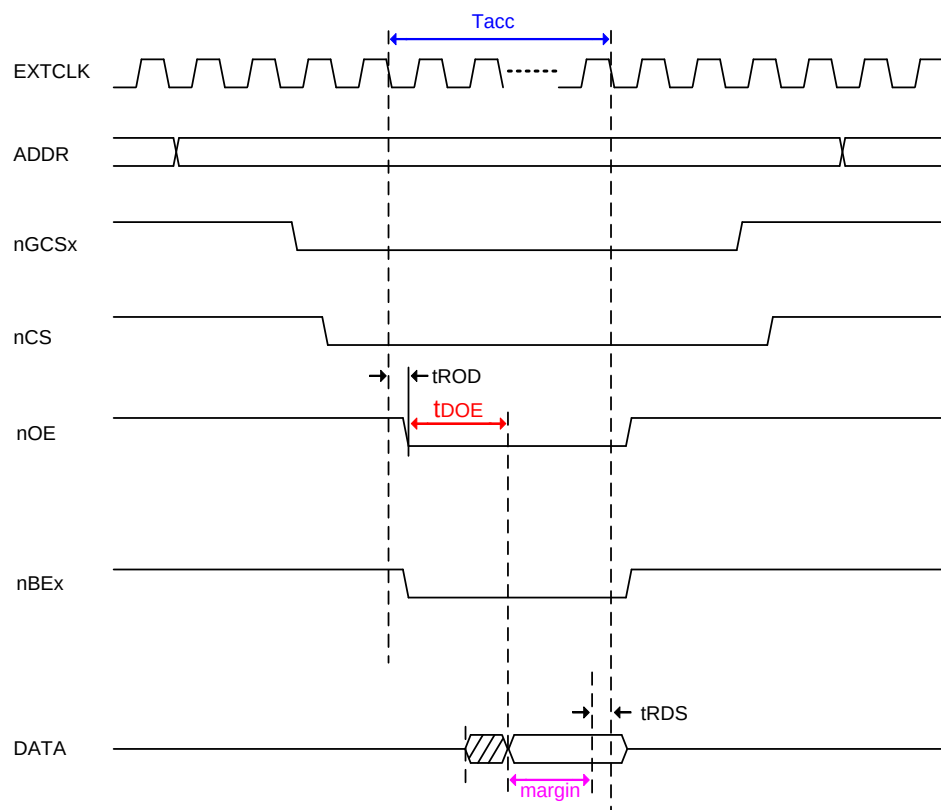
with condition:

$$t_{ROD} + t_{DOE} + \text{margin} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$t_{AA} + \text{margin} + t_{RDS} \leq T_{acc} \times t_{cyc}$$



$$t_{ROD} + t_{DOE} + \text{margin} + t_{RDS} \leq T_{acc} \times t_{cyc}$$



For 25 ns SRAM and CPU running at 66 MHz ($t_{cyc} = 15.15$ ns):

$$T_{acc_{min}} \geq (25 + 1)/15.15 \geq 1.72 = 2$$

Condition checking

$$11 + 13 + 1 = 25 < 30.3 (= 2 \times 15.15),$$

Therefore $T_{acc_{min}} = 2$ for read cycle for 25 ns SRAM.

$$\text{Margin} = 30.3 - 25 - 1 = 4.3 \text{ ns}$$

For 45 ns SRAM and CPU running at 66 MHz ($t_{cyc} = 15.15$ ns):

$$T_{acc_{min}} \geq (45 + 1)/15.15 \geq 3.07 = 4$$

Condition checking

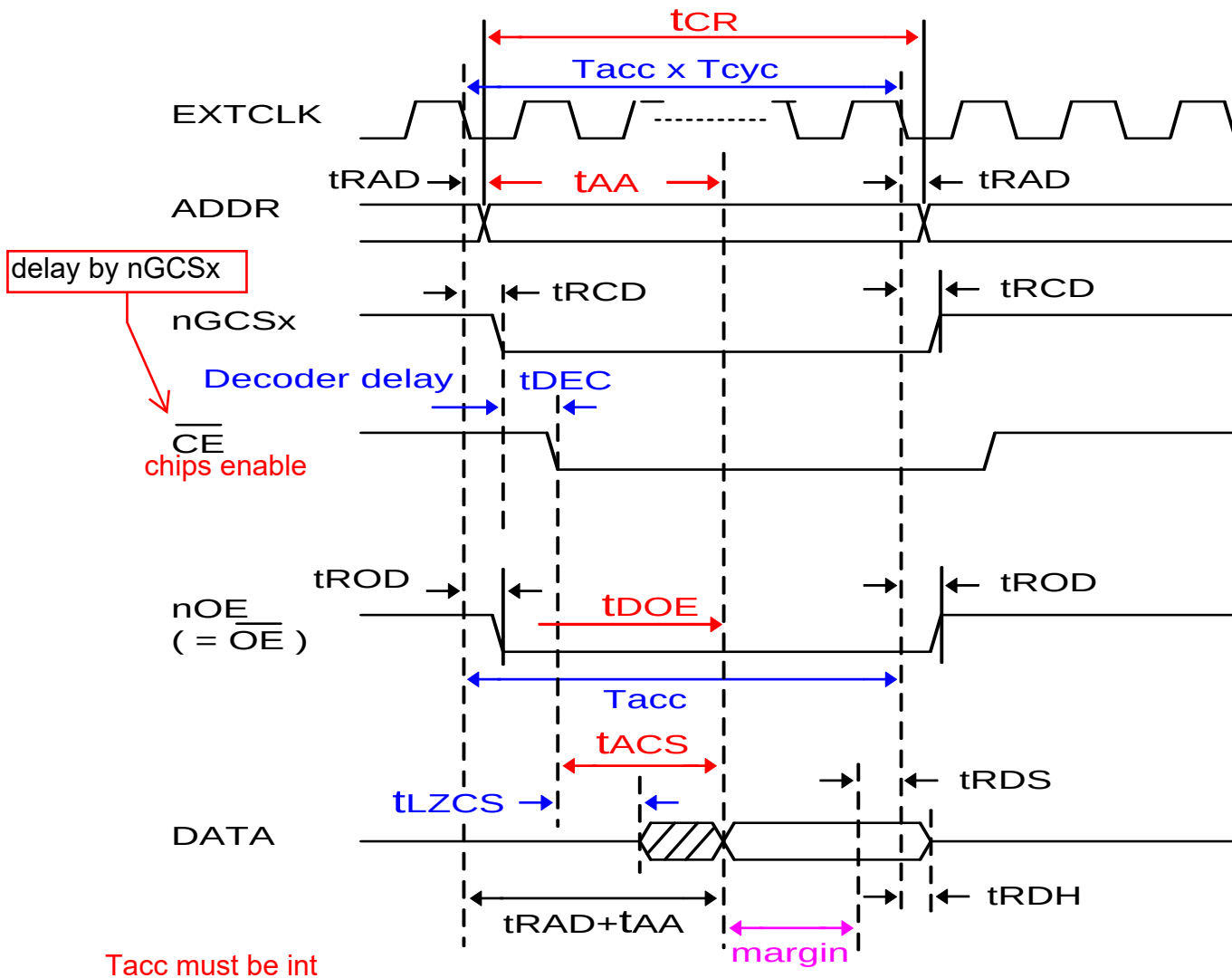
$$11 + 25 + 1 = 37 < 60.6 (= 4 \times 15.15),$$

Therefore $T_{acc_{min}} = 4$ for read cycle for 45 ns SRAM.

$$\text{Margin} = 60.6 - 45 - 1 = 14.6 \text{ ns}$$

Preferable Design – shortest access time

Setting Tacs, Tcos, Toch and Tcah to ZERO value to achieve highest speed of read/write bus cycle and the corresponding timing diagram is shown as follow:



$$t_{RAD} + t_{AA} + \text{margin} + t_{RDS} \leq t_{RC} (=T_{acc} \times t_{cyc})$$

$$\text{i.e., } T_{acc} \geq (t_{RAD} + t_{AA} + t_{RDS}) / t_{cyc} \quad (\text{Margin}_{\min} = 0)$$

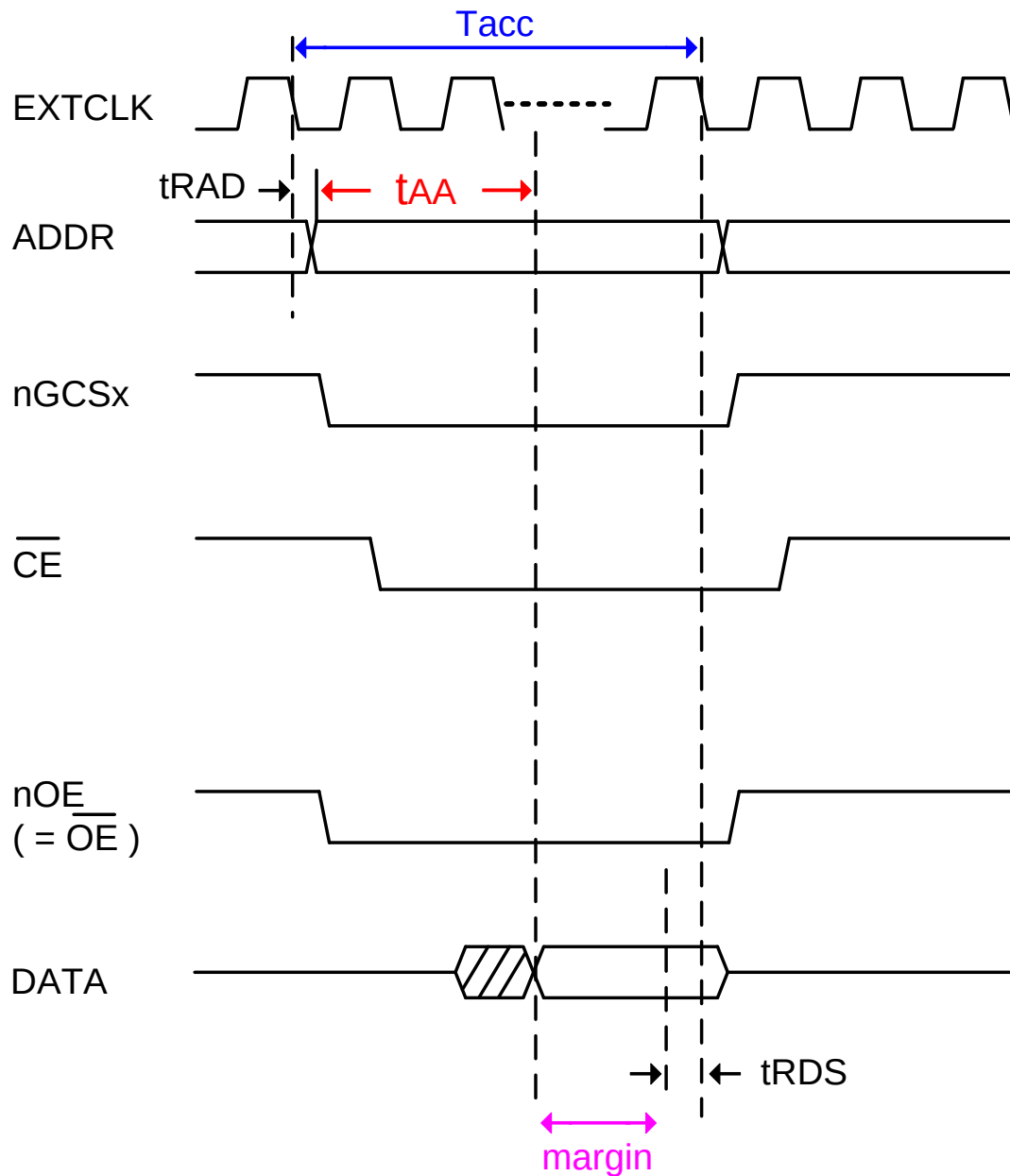
with conditions:

$$(i) \quad t_{RCD} + t_{DEC} + t_{ACS} + \text{margin} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$(ii) \quad t_{ROD} + t_{DOE} + \text{margin} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

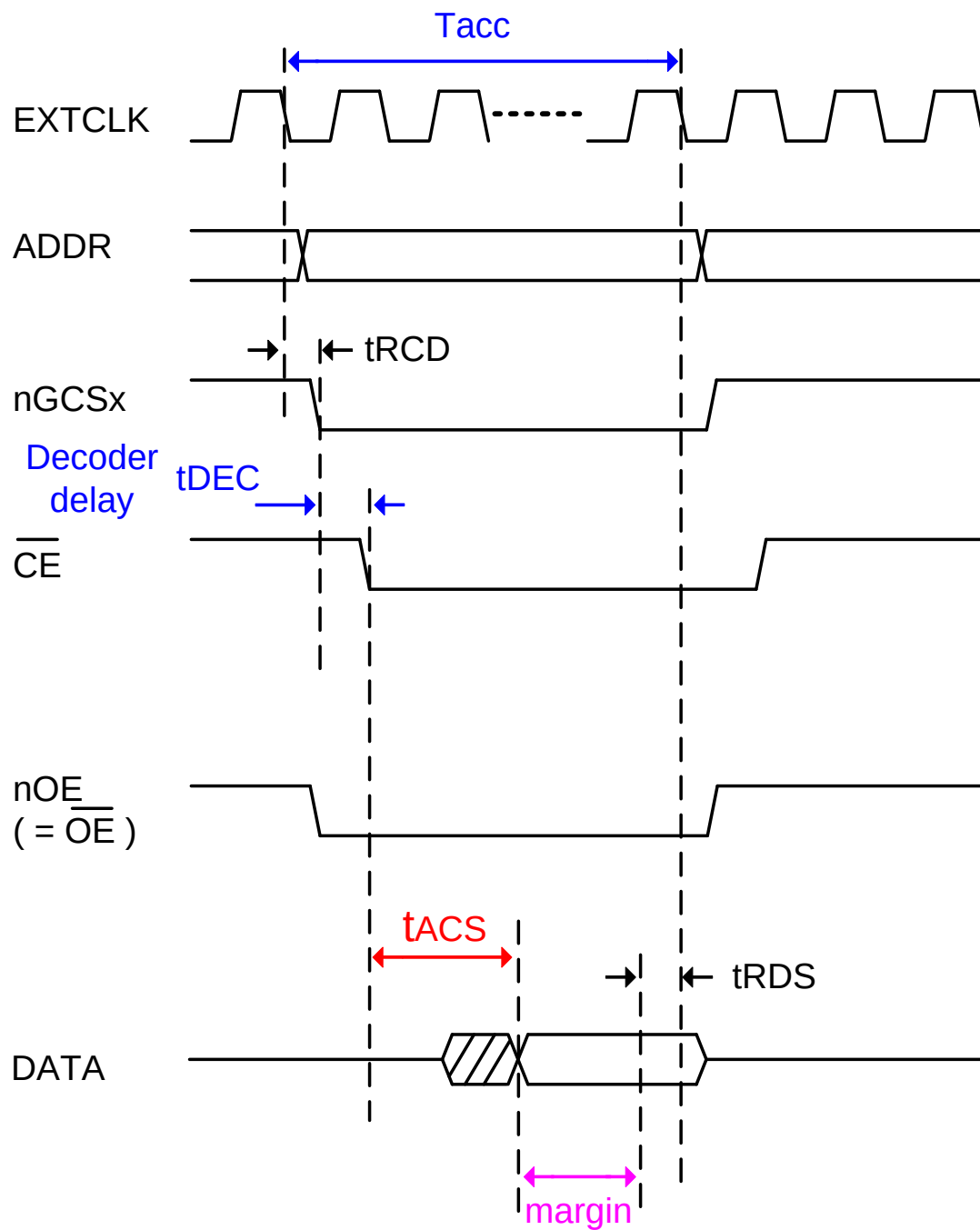
Final initial T_{acc} with is equation:

$$t_{RAD} + t_{AA} + \text{margin} + t_{RDS} \leq T_{acc} \times t_{cyc}$$



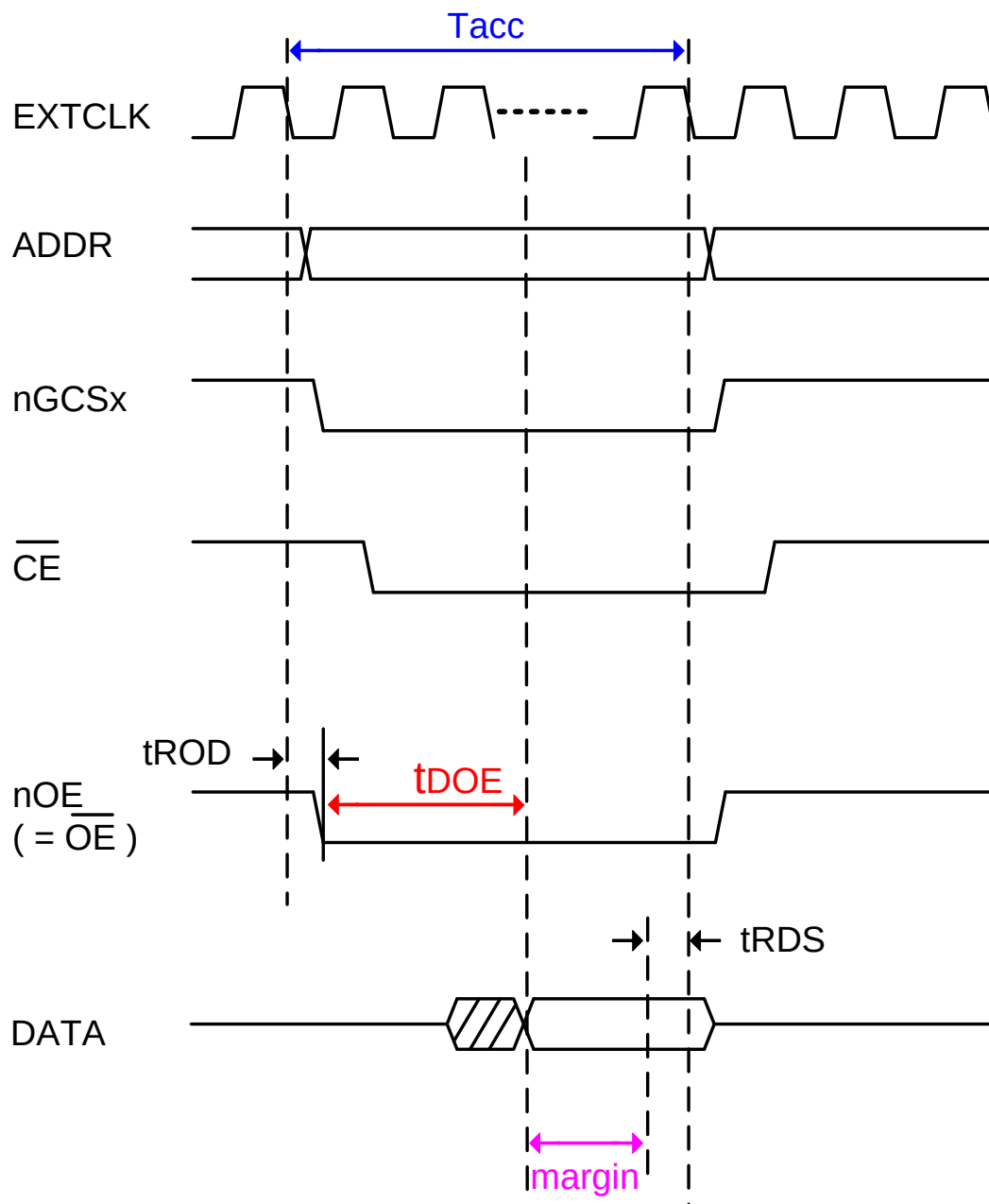
Condition due to chip select signal (i):

$$t_{\text{RCD}} + t_{\text{DEC}} + t_{\text{ACS}} + \text{margin} + t_{\text{RDS}} \leq T_{\text{acc}} \times t_{\text{cyc}}$$



Condition due to output enable signal (ii):

$$t_{\text{ROD}} + t_{\text{DOE}} + \text{margin} + t_{\text{RDS}} \leq T_{\text{acc}} \times t_{\text{cyc}}$$



For 25 ns SRAM and CPU running at 66 MHz ($t_{cyc} = 15.15$ ns):

$$T_{acc} \geq (t_{RAD} + t_{AA} + t_{RDS}) / t_{cyc}$$

$$T_{acc_{min}} \geq (12 + 25 + 1) / 15.15 \geq 2.51 = 3$$

Condition checking (i):

Assuming that the decoder delay t_{DEC} is 20ns

$$t_{RCD} + t_{DEC} + t_{ACS} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

$$11 + 20 + 25 + 1 = 57 \implies T_{acc} \geq 57 / 15.15 \implies T_{acc} = 4$$

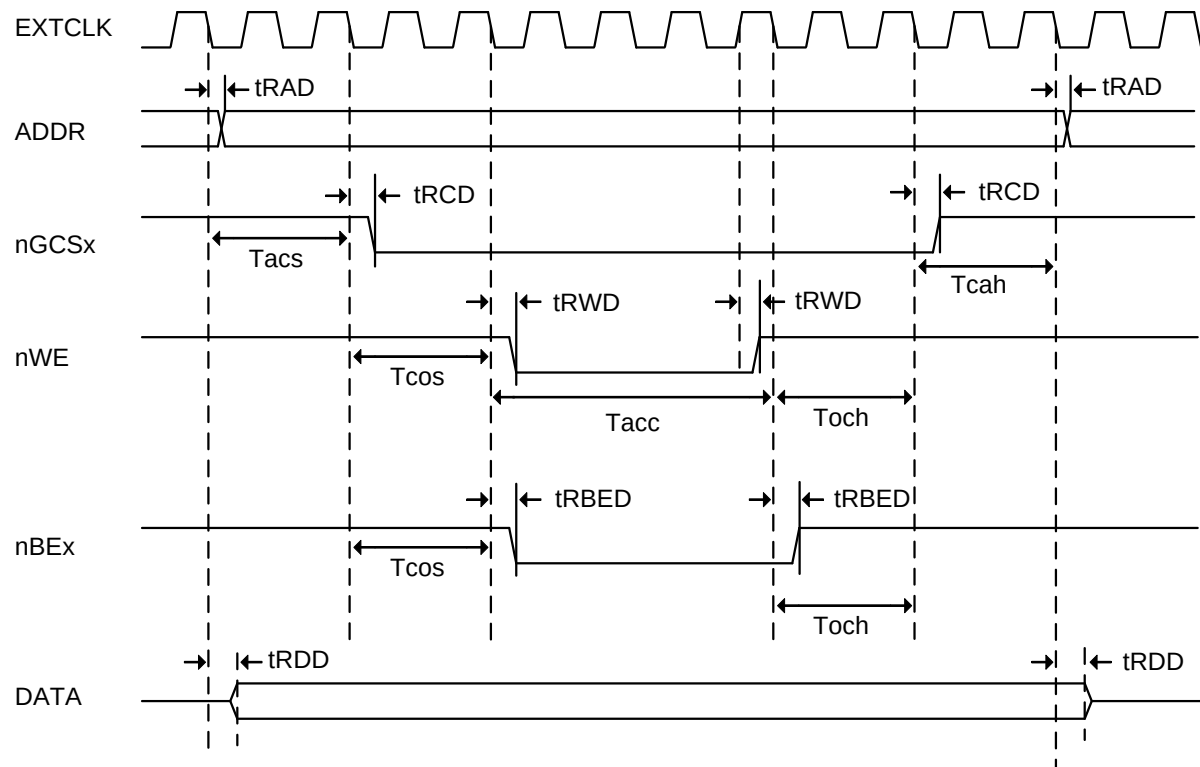
Condition checking (ii):

$$t_{ROD} + t_{DOE} + t_{RDS} \leq T_{acc} \times t_{cyc}$$

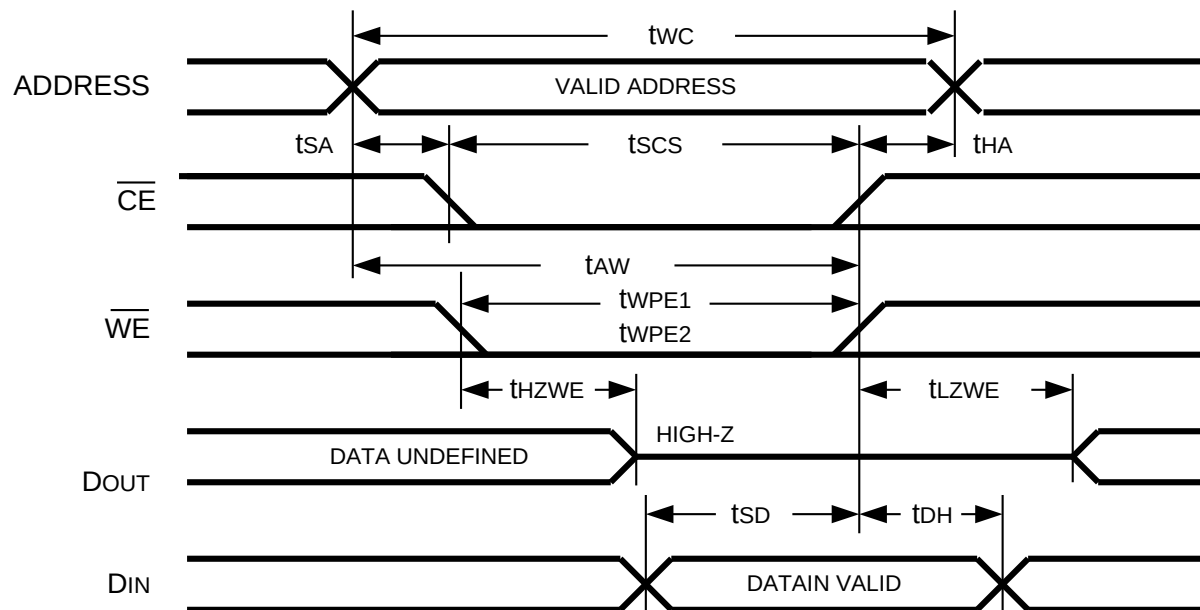
$$11 + 13 + 1 = 25 \implies T_{acc} \geq 25 / 15.15 \implies T_{acc} = 2$$

Therefore $T_{acc_{min}} = \max(3, 4, 2) = 4$ for read cycle with CPU running at 66MHz clock rate.

10.7.2 Write cycle

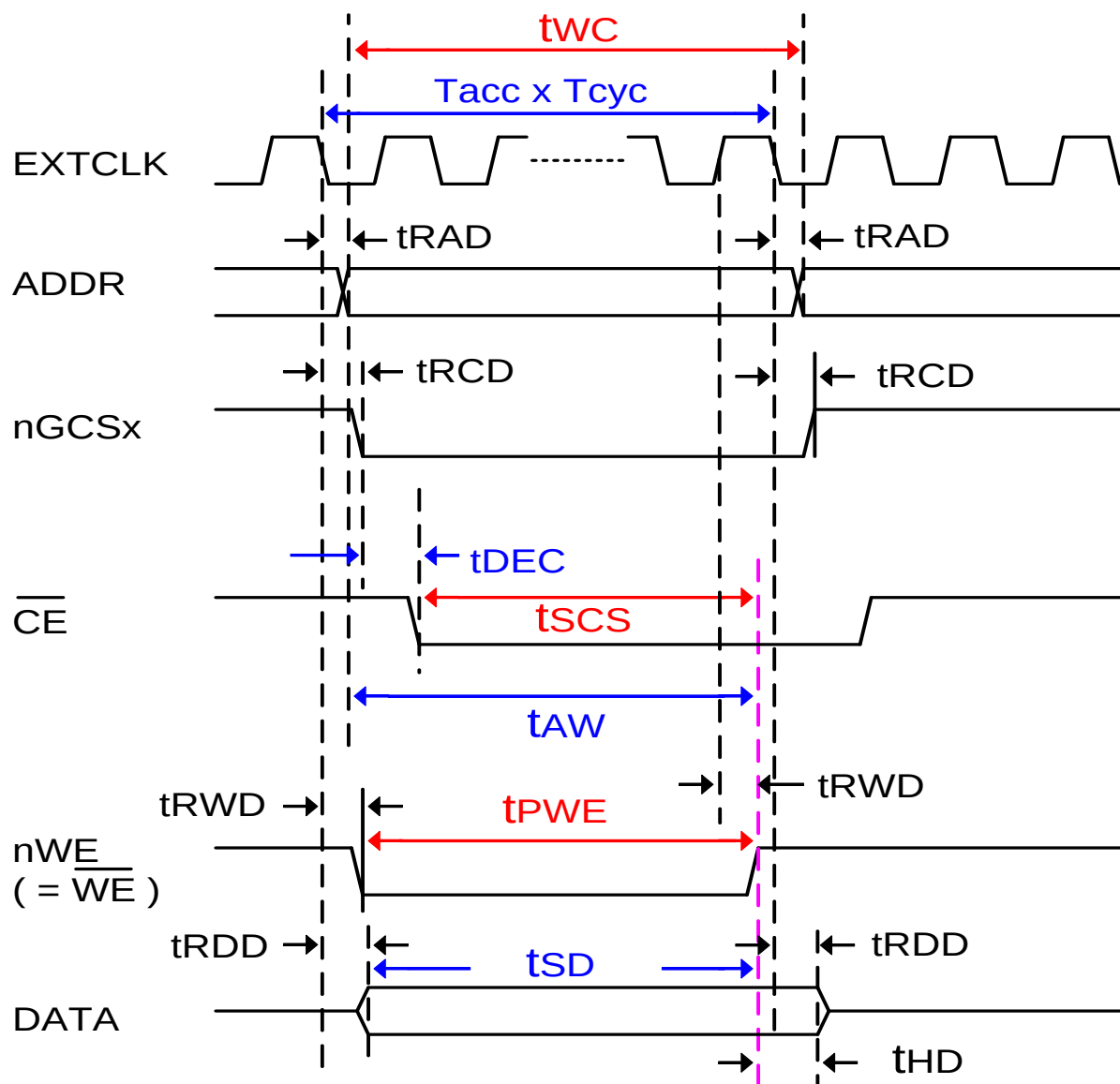


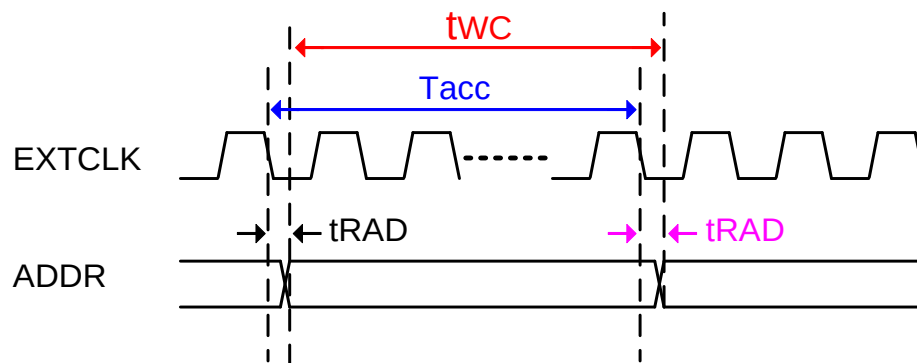
ROM/SRAM WRITE Timing (I)
 ($T_{acs}=2, T_{cos}=2, T_{acc}=4, T_{och}=2, T_{cah}=2, PMC=0, ST=0$)



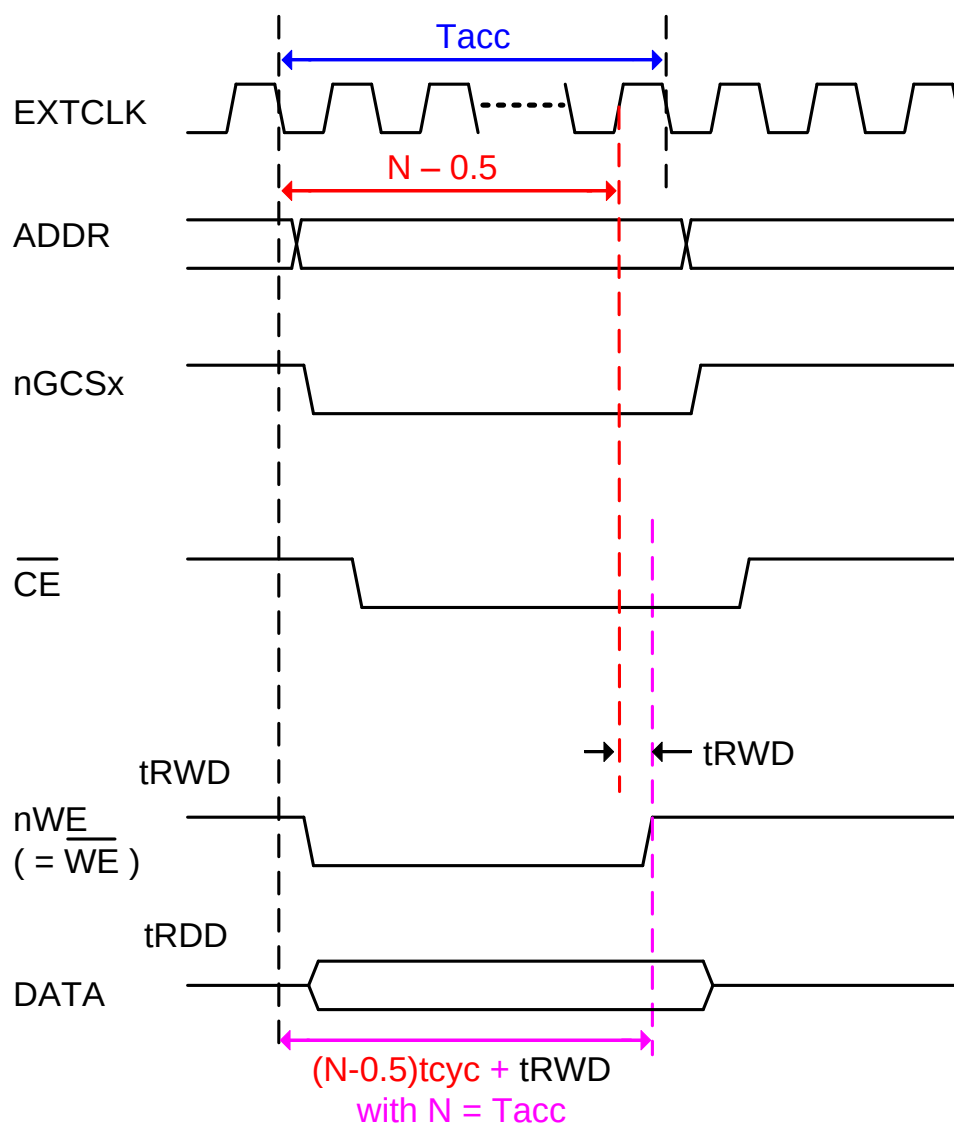
IS65C256AL SRAM write cycle timing diagram

<i>Symbol</i>	<i>Parameter</i>	<i>25 ns</i> <i>Min. Max.</i>		<i>45 ns</i> <i>Min. Max.</i>	
tWC	Write Cycle Time	25	—	45	—
tSCS	CE to Write End	15	—	35	—
tAW	Address Setup Time to Write End	15	—	25	—
tHA	Address Hold from Write End	0	—	0	—
tSA	Address Setup Time	0	—	0	—
tPWE1, tPWE2(4)	WE Pulse Width	15	—	25	—
tSD	Data Setup to Write End	12	—	20	—
tHD	Data Hold from Write End	0	—	0	—



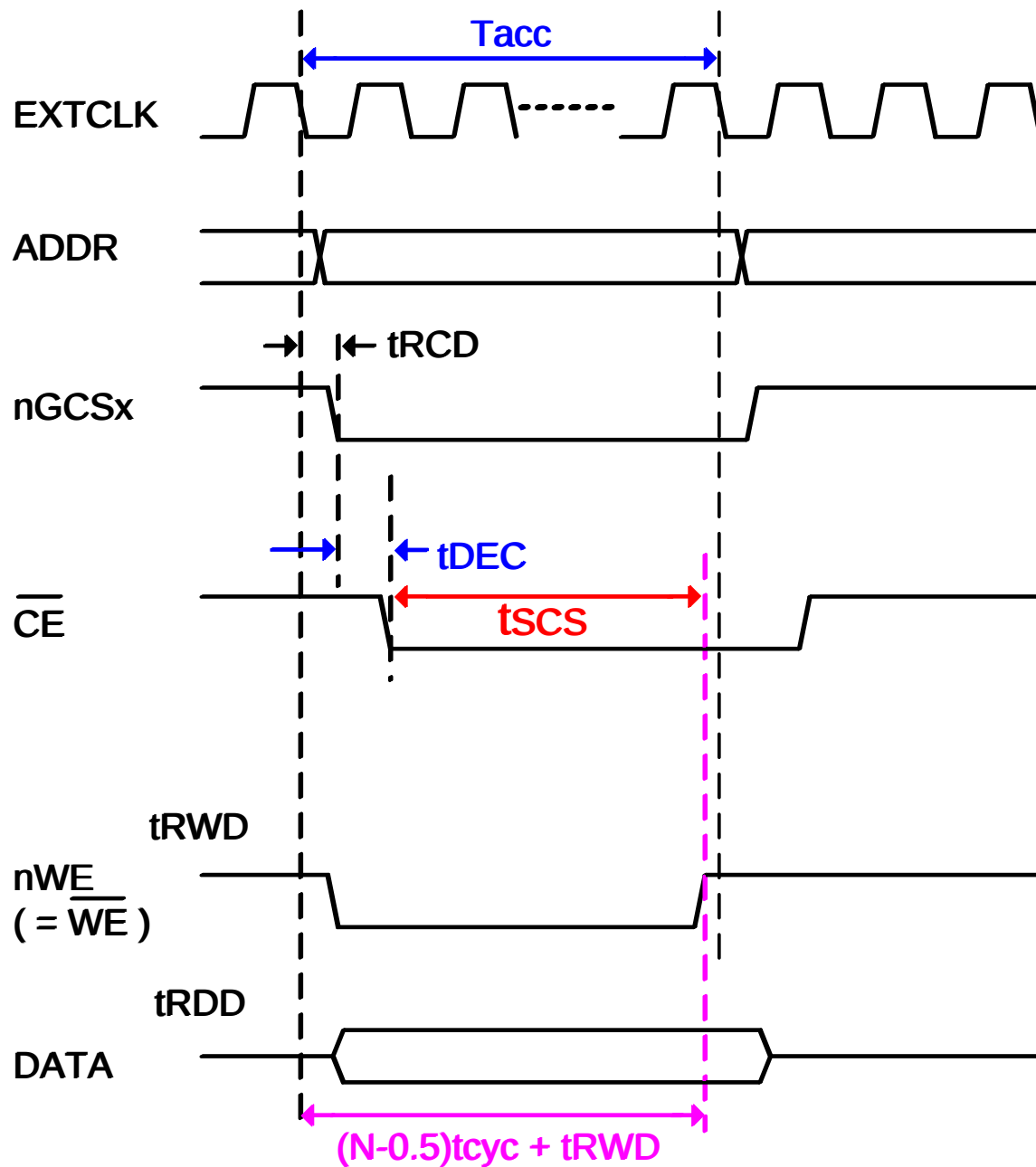
$$tWC = N \times T_{cyc} + tRAD - tRAD$$


(N-0.5)tcyc + tRWD



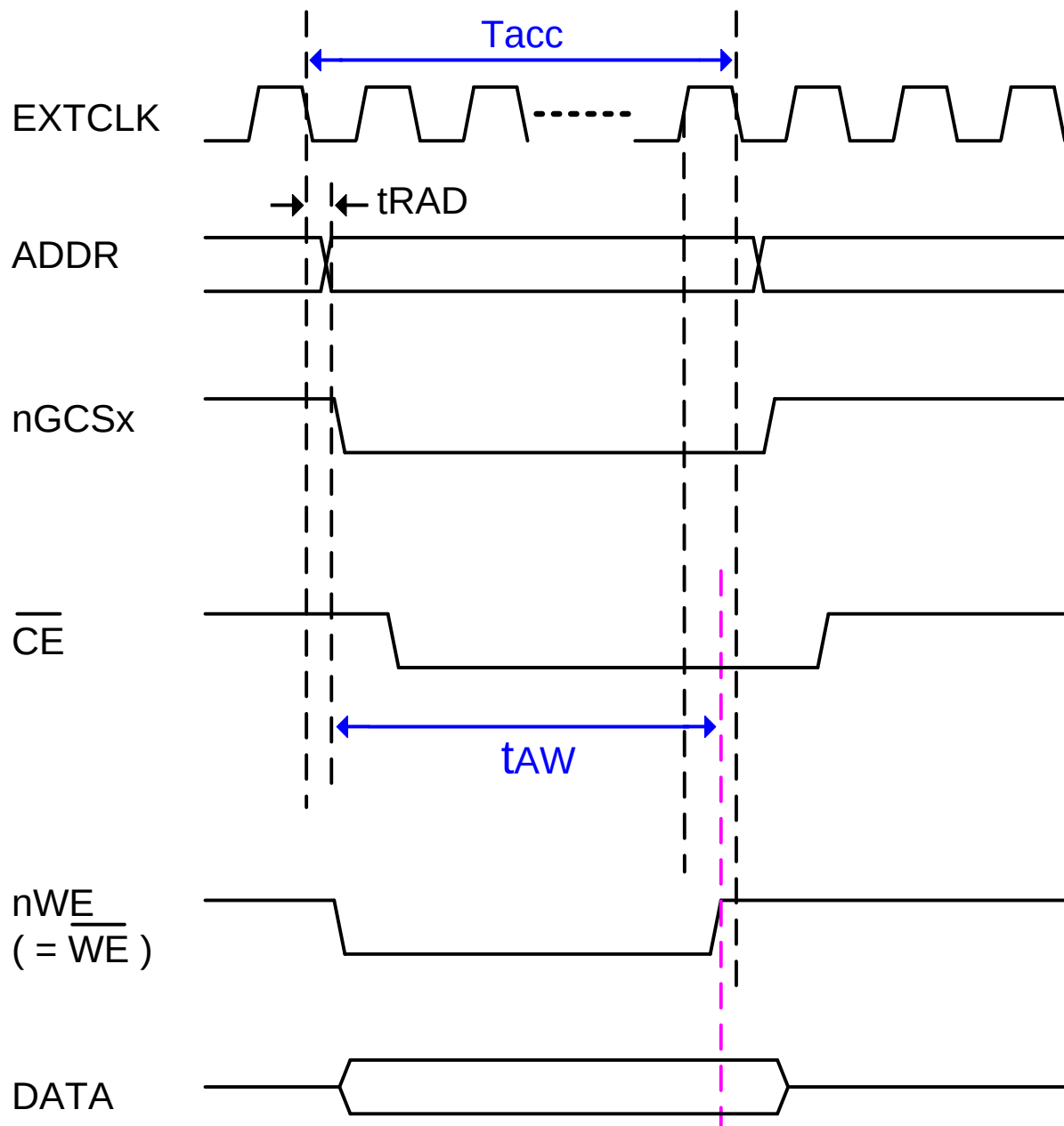
CE to Write End

$$t_{SCS} = (N-0.5) \times T_{cyc} + t_{RWD} - t_{RCD} - t_{DEC}$$



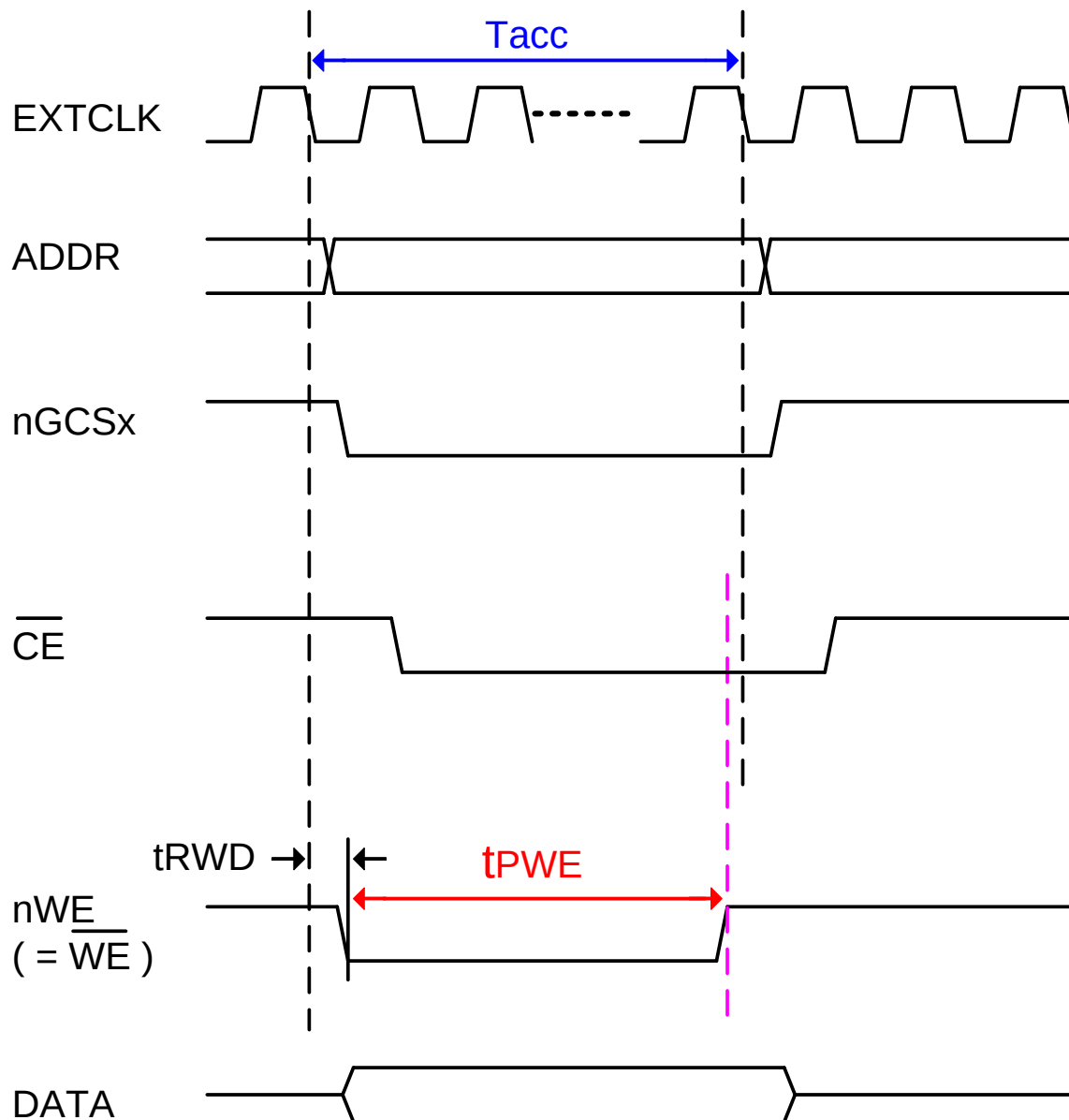
Address Setup Time to Write End

$$t_{AW} = (N-0.5) \times T_{cyc} + t_{RWD} - t_{RAD}$$



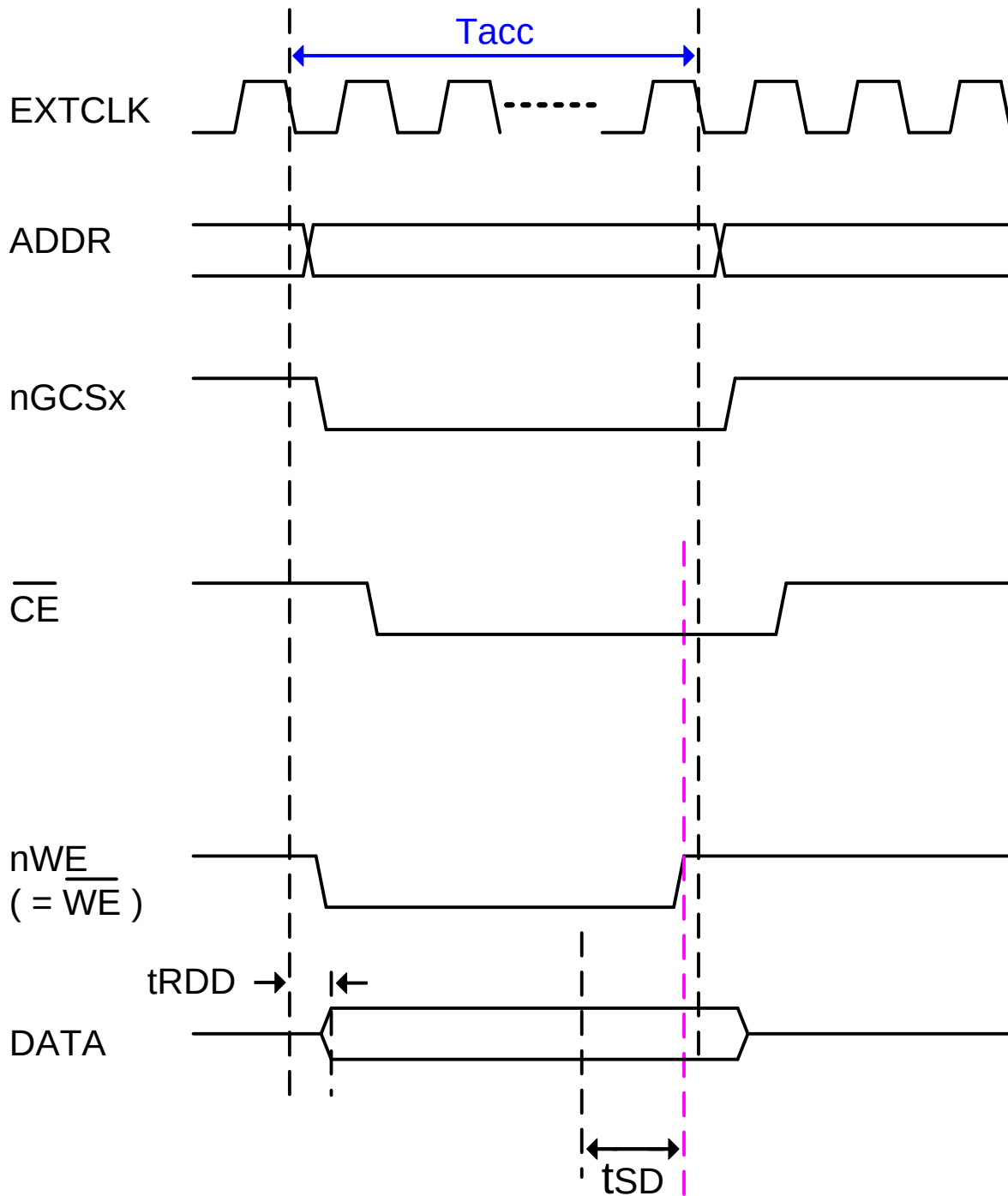
WE Pulse Width

$$t_{PWE} = (N-0.5) \times T_{cyc} + t_{RWD} - t_{RWD}$$

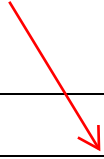


Data Setup to Write End

$$t_{SD} = (N-0.5) \times T_{cyc} + t_{RWD} - t_{RDD}$$



With the preferable design, set $T_{acs}=0$, $T_{cos}=0$, $T_{acc}=N$, $T_{och}=0$ and $T_{cah}=0$, then the conditions for a 66MHz CPU become:



			Req'd
tWC	$N \times T_{cyc} + t_{RAD} - t_{RAD}$	$N \times 15.15$	25
tSCS	$(N-0.5) \times T_{cyc} + t_{RWD} - t_{RCD} - t_{DEC}$	$(N-0.5) \times 15.15 + 14 - 11 - 20$ $= (N-0.5) \times 15.15 - 17$	15
tAW	$(N-0.5) \times T_{cyc} + t_{RWD} - t_{RAD}$	$(N-0.5) \times 15.15 + 14 - 12$ $= (N-0.5) \times 15.15 + 2$	15
tPWE	$(N-0.5) \times T_{cyc} + t_{RWD} - t_{RWD}$	$(N-0.5) \times 15.15$	15
tSD	$(N-0.5) \times T_{cyc} + t_{RWD} - t_{RDD}$	$(N-0.5) \times 15.15 + 14 - 14$ $= (N-0.5) \times 15.15$	12

For READ cycle, $T_{acc_{min}} = 4$

Use $T_{acc} = 4$ to check the validity of the above requirement.

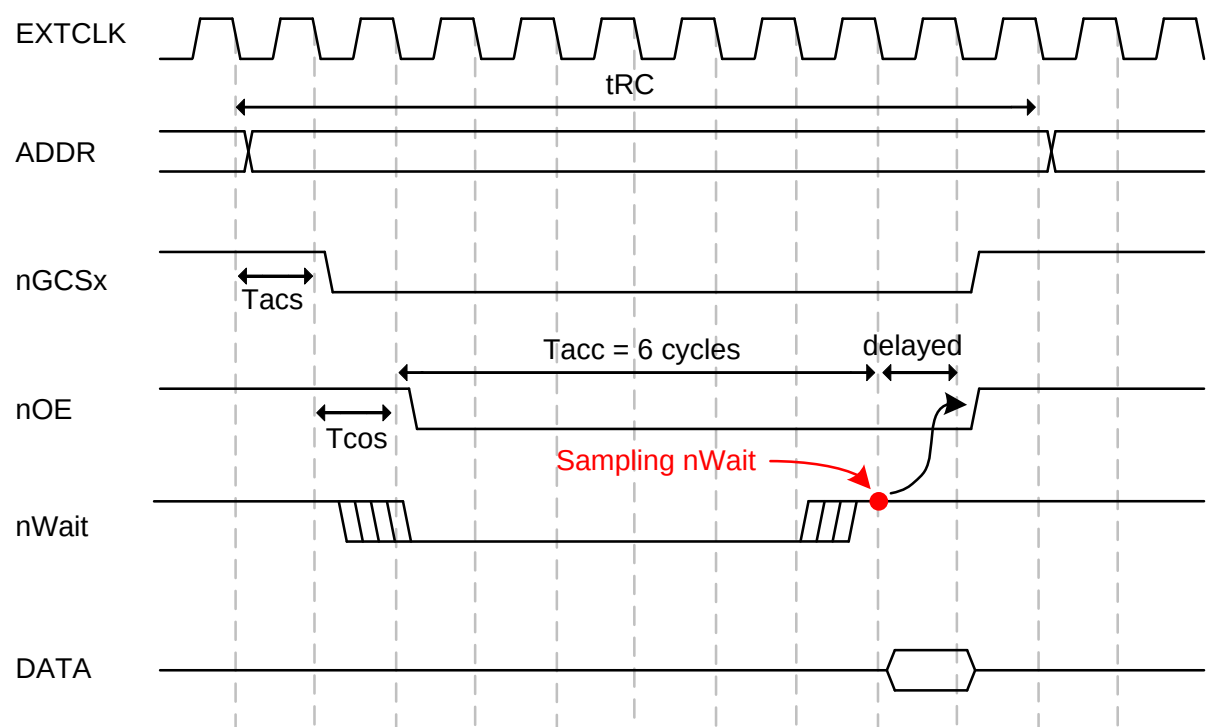
If it does not fit, find a large T_{acc} that fits all – both R and W.

10.8 Memory interface with external wait input

Certain CPU is equipped with an external wait input pin (nWAIT for S3C44B0x) to signal request for a long bus cycle.

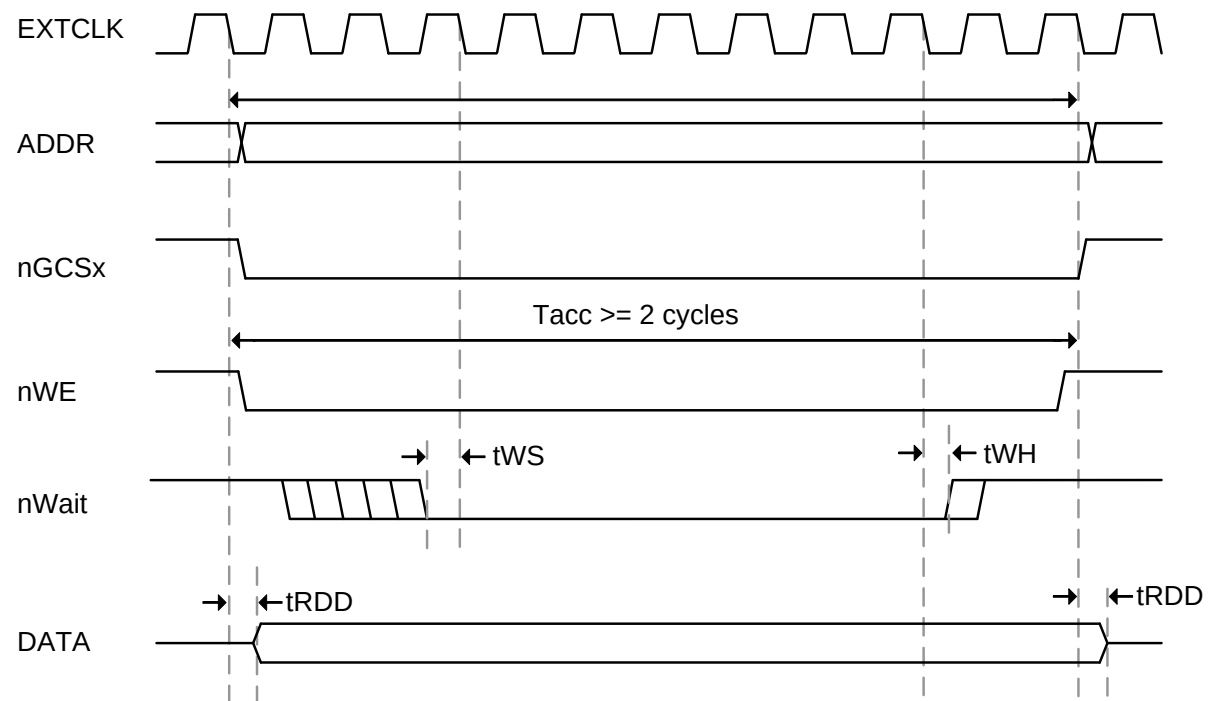
When this signal is asserted, the current bus cycle cannot be completed and CPU must wait for another or more clock cycles to complete the current bus cycle – inserting wait state.

This will be used for accessing very slow memory devices or peripheral devices that the delay time is longer than the standard setting defined in the associated register (e.g. BANKCON6 and BANKCON7 for S3C44B0x).



NOTE : The status of nWait is checked at $(T_{acc}-1)$ cycle.

External nWAIT READ Timing
($T_{acs}=0$, $T_{cos}=0$, $T_{acc}=6$, $T_{och}=0$, $T_{cah}=0$, $PMC=0$, $ST=0$)

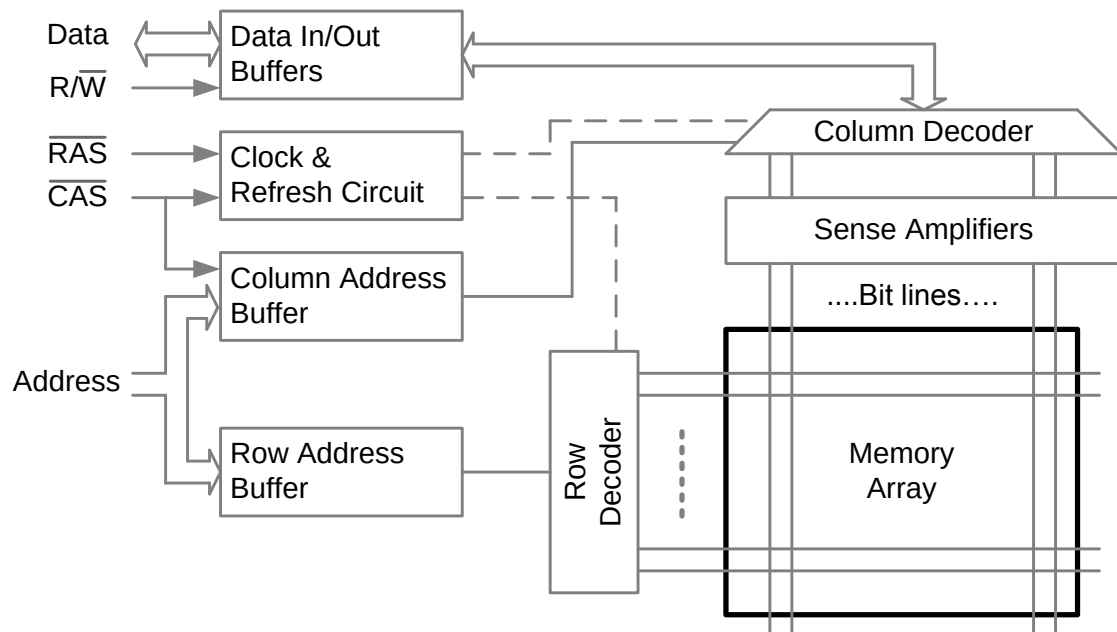


External nWAIT WRITE Timing
($T_{acs}=0$, $T_{cos}=0$, $T_{acc}=4$, $T_{och}=0$, $T_{cah}=0$, $PMC=0$, $ST=0$)

10.9 Asynchronous DRAM

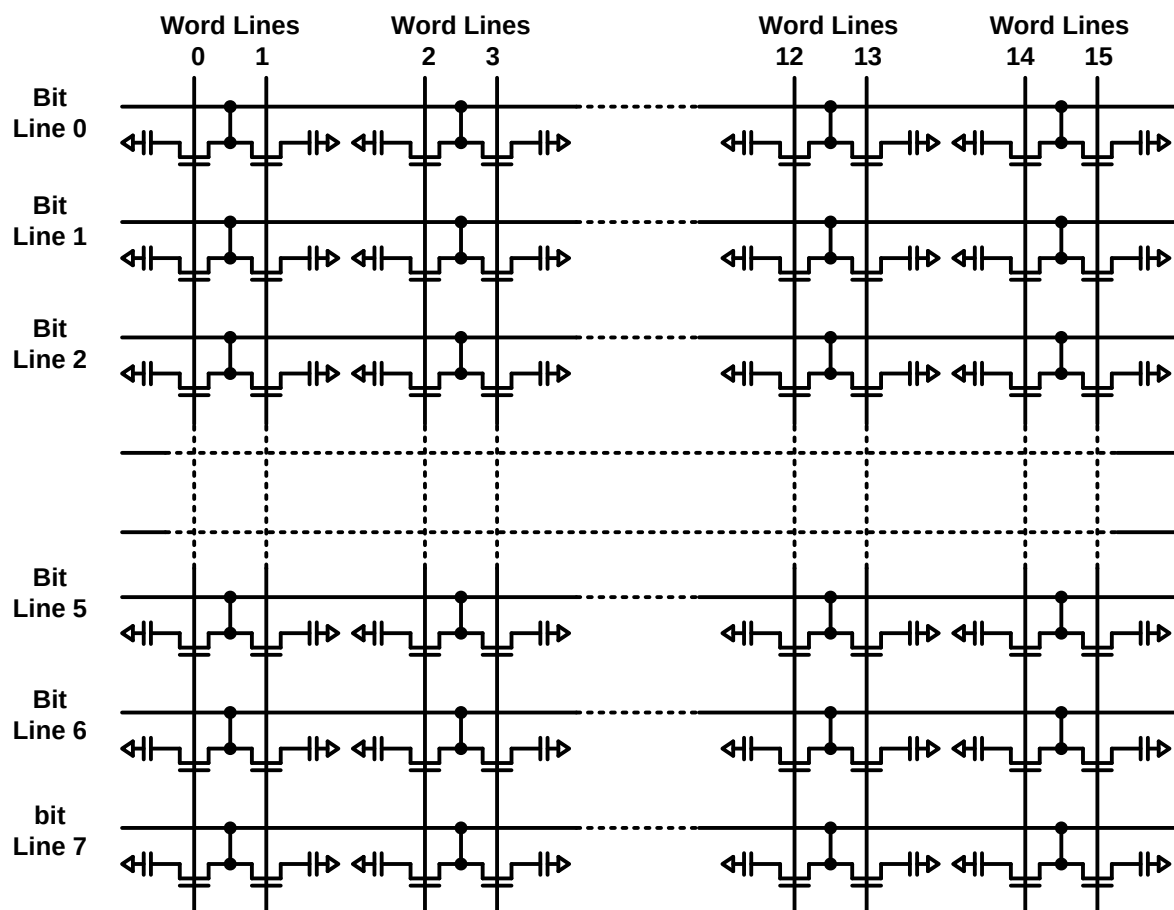
10.9.1 Classical DRAM

- The internal structure of a typical DRAM is shown below:

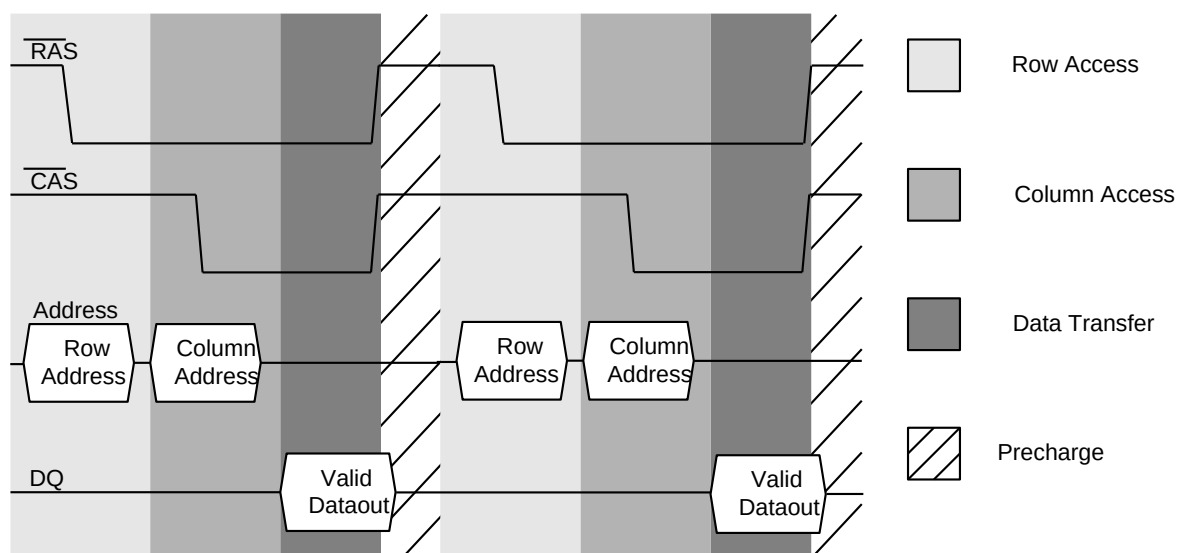
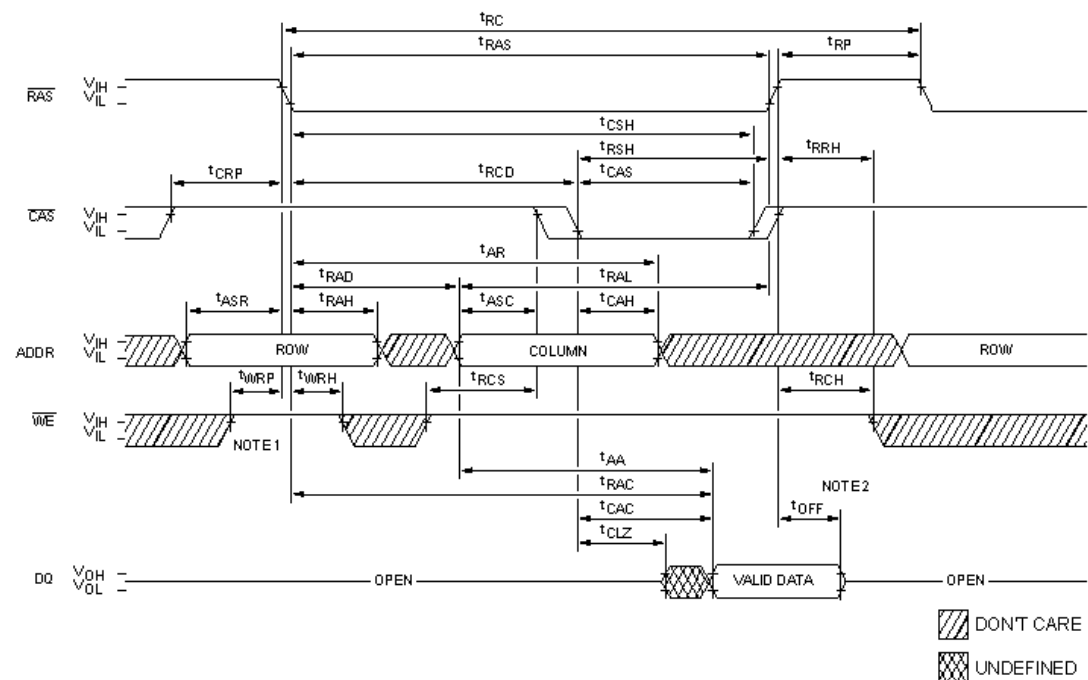


- A DRAM memory array can be thought of as a table of cells arranged in a matrix manner.
- The address bus is multiplexed between row and column components.
- The multiplexed address bus uses two control signals $\overline{\text{RAS}}$ (row address strobe) and $\overline{\text{CAS}}$ (column address strobe) to cause the DRAM to latch the address components.
- The row address causes a complete row of memory cells (or usually a page) to pass data to the bit lines connected to the sense amps.
- The column address selects the data subset from the sense amplifiers and causes it to be driven to the output pins.
- The sense amplifier amplifies the value on the bit line and drives the refreshed value back into the storage cell.

- Due the leakage of the cell capacitor, a periodic refresh cycle is required or data will be lost.
- A refresh controller determines the time between refresh cycles, and a refresh counter ensures that the entire array (all rows) is refreshed. Of course, this means that some bus cycles are used for refresh operations, and has some impacts on performance.
- The cells of a corresponding row are refreshed during a read operation – reading a page of memory.
- The required refresh timing requirement can be found from the data sheet of the memory device, e.g., 1024 refresh cycles in 16 ms standard $\rightarrow$ 15.625 μ s interval.
- The figure below illustrates the internal structure of a DRAM memory array:



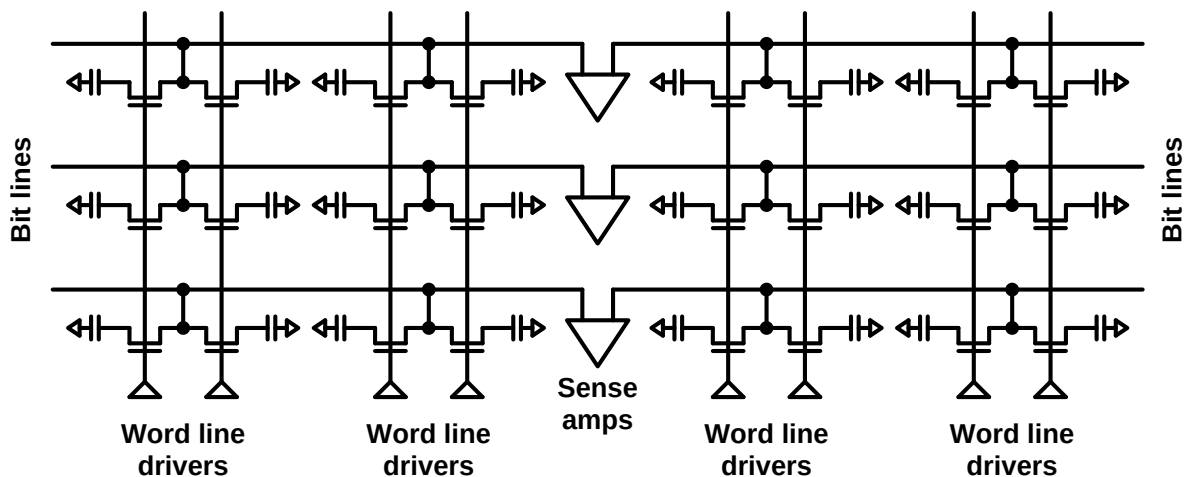
- A typical read cycle timing diagram shown below:



- The DRAM will latch the row address signaled by $\overline{RAS}$ and latch the column address by $\overline{CAS}$ signal, and then place the data onto the data bus. The read cycle is then ended.
- A write cycle is similar, the data will be written in to the DRAM after latching the row and column addresses.

10.9.2 Sense Amplifier

Open Bitline Architecture:



The memory bit cells are organized into two sub-array structure. When accessing the device, only one sub-array is addressed. The other sub-array is for reference only.

A sense amplifier is connected to two bit lines, one from each sub-array.

Before reading the data stored in the memory cell, a **precharge** action is taken.

All bit lines are driven to $V_{cc}/2$.

Word lines are 0V.

All pass transistors are off.

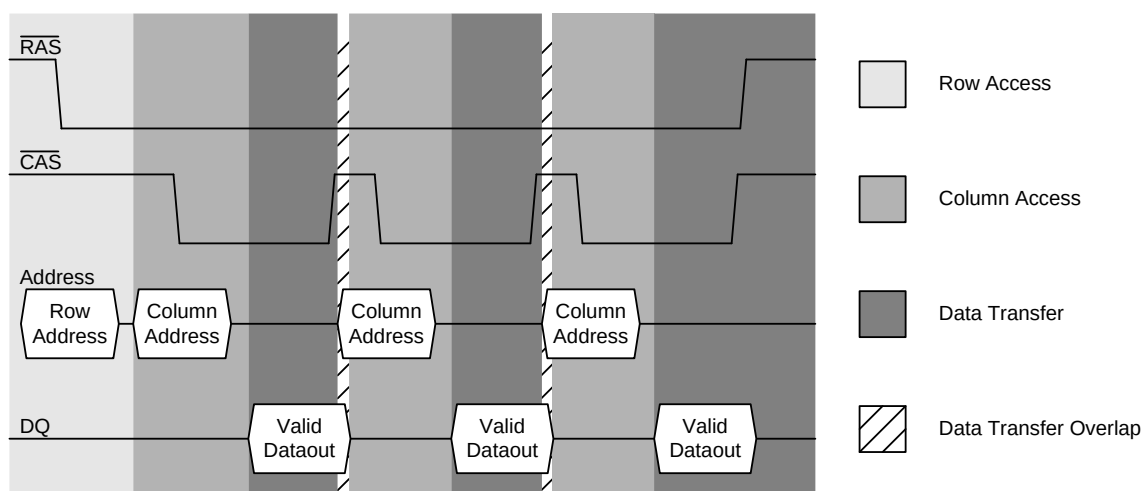
When a bit cell is read, the storage capacitor voltage is compared with the voltage of the bit line of the reference sub-array, $V_{cc}/2$.

The bit is regarded as logic “1” if the voltage is greater than $V_{cc}/2$, or logic “0” if the voltage is less than $V_{cc}/2$.

The sense amplifier will also recharge the “address” bit to its original voltage level.

10.9.3 Fast Page Mode DRAM (FPM DRAM)

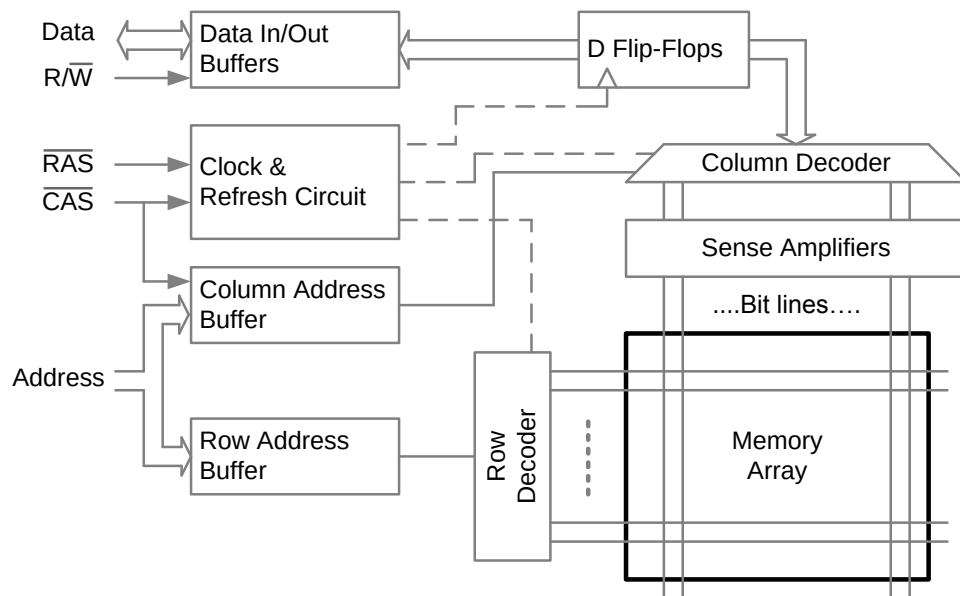
- Each normal DRAM access requires two address cycles, one for row address, and one for column address.
- For most cases, memory access is in sequential manner and the row addresses remain unchanged.
- If one thinks of each row as a page of data, then the access of the next memory location does not require a row address cycle and the access time can be reduced significantly.
- The diagram below illustrates the timing of FPM DRAM.



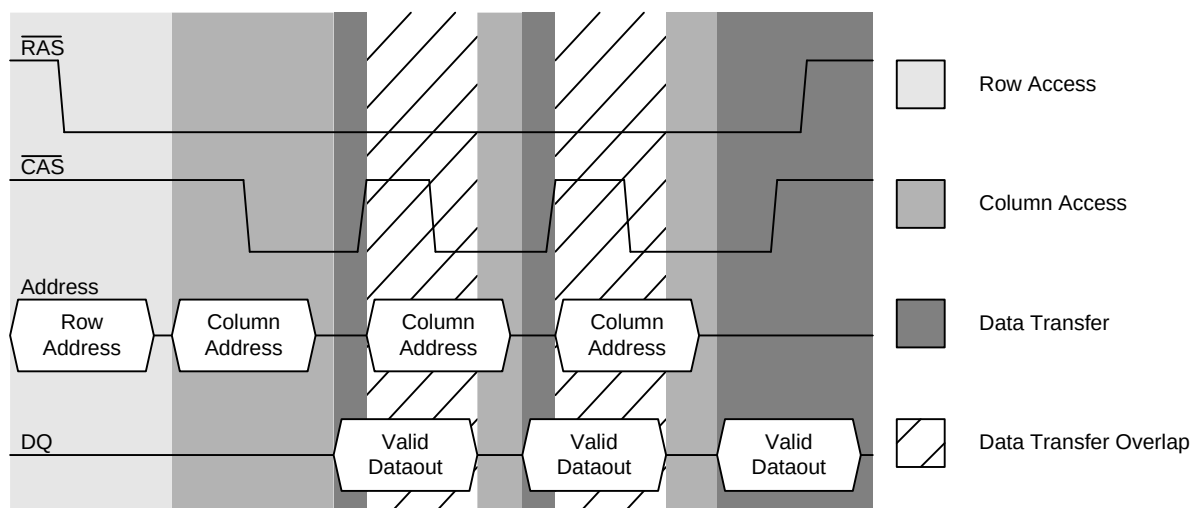
- If the data accessed are stored in random manner, FPM would only perform marginally better than normal DRAM.
- Of course, in order to take advantage of FPM, the CPU or memory controller must be designed to handle FPM. Replacing normal DRAM with FPM DRAM offers no speed improvement without system reconfiguration.

10.9.4 Extended Data Output DRAM (EDO DRAM)

- Extended Data Out DRAM adds a latch between the sense amplifiers and the output pins of the DRAM, as shown in the figure below:

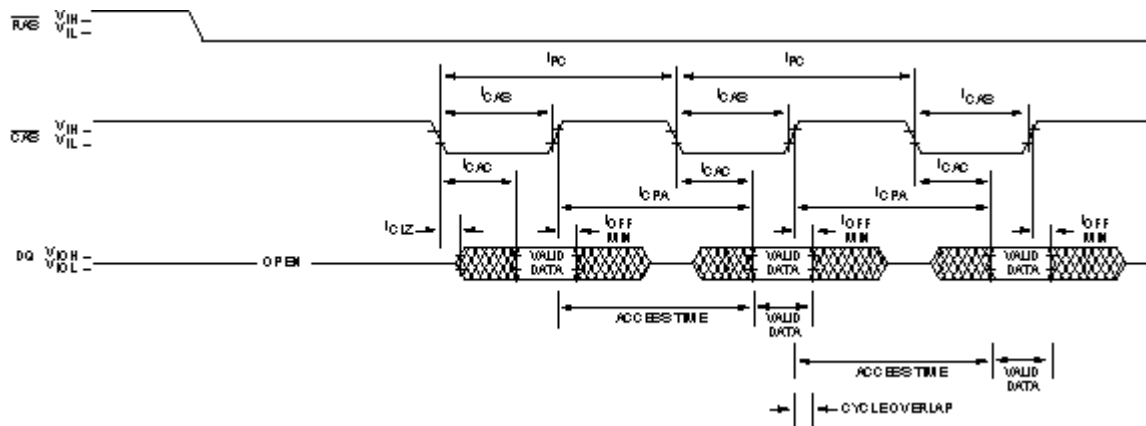


- The latch allows the data on the outputs to remain valid longer and hence more overlap between column access and data transfer than in FPM.

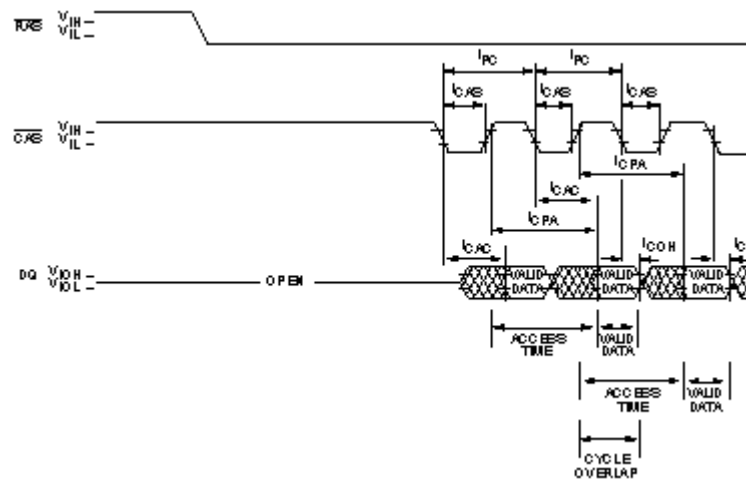


- This long overlapped period permits $\overline{\text{CAS}}$ to be rapidly de-asserted, allowing the memory array to begin precharging sooner.
- Considering that if a system using FPM requires data to be valid for 10ns but the time between accesses is 40ns, then a single access takes 50 ns.

- With EDO, there is less overhead, the time between accesses thus can be reduced to 20ns for a total access time of 30ns.
- To get a better understanding, the figure below compares the timing of a system designed to take full advantage of EDO and a system designed for FPM only. (Note the CAS cycle is shorter for EDO DRAM.)



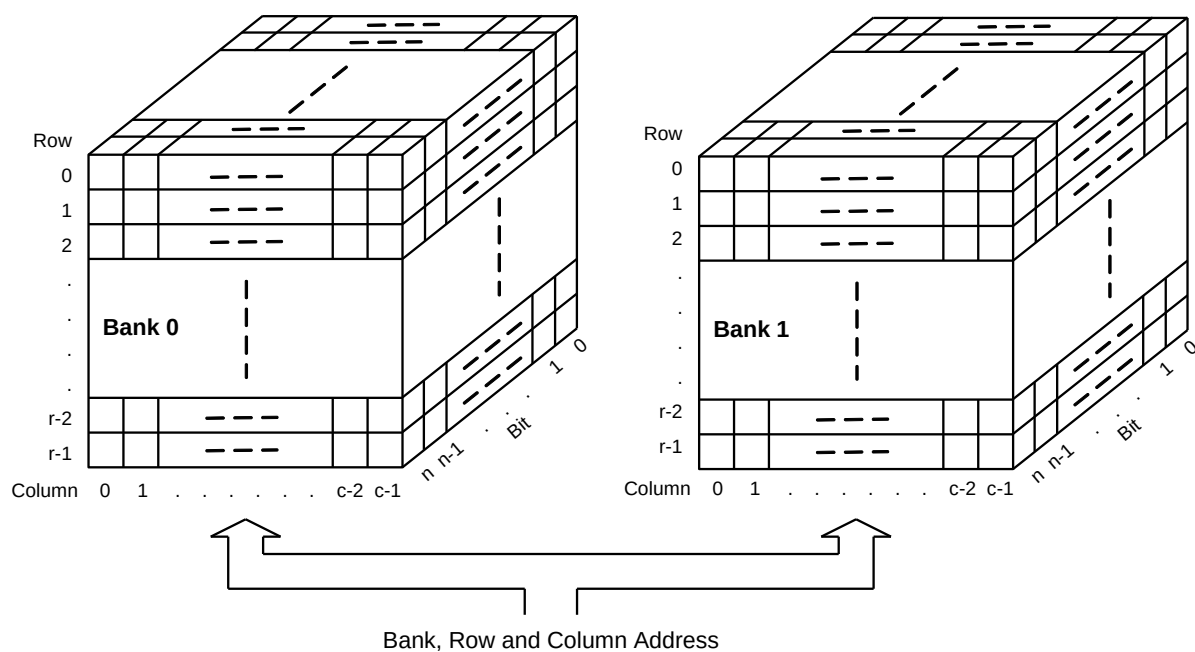
(a) Conventional FPM



(b) EDO

10.10 Synchronous DRAM (SDRAM)

- The DRAMs discussed in previous section above do NOT operate in synchronous with the CPU, i.e. no clock signal required from CPU.
- Synchronous DRAM requires a clock signal to synchronous it Read/Write operation with the system clock (or its derivative).
- CPU only sends the clock (SCLK for S3C44B0X) when accessing the SDRAM to reduce power.
- Its operation is more complicated when comparing with the DRAM.
- It is usually structured as banks, e.g. a 2 banks block diagram is shown below:



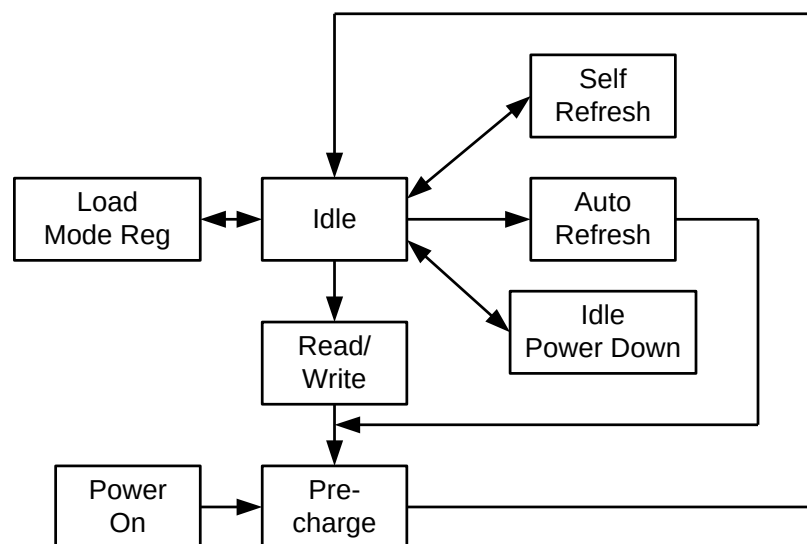
- While SRAM and DRAM uses hardware signals to control the read (nOE) and write (nWE) operations, SDRAM uses command to control read, write and other operations.
- The states of four hardware signals (**CS***, **RAS***, **CAS*** and **WE***) form the command.

- The following table shows the typical commands for operating the SDRAM (refer to data sheet for different devices).

Command Name	CS*	RAS*	CAS*	WE*
DESELECT DEVICE	H	X	X	X
NO OPERATION (NOP)	L	H	H	H
ACTIVE (select Bank/Row)	L	L	H	H
READ	L	H	L	H
WRITE	L	H	L	L
BURST STOP	L	H	H	L
PRECHARGE	L	L	H	L
AUTO REFRESH	L	L	L	H
LOAD MODE REGISTER	L	L	L	L

10.10.1 Operational state diagram

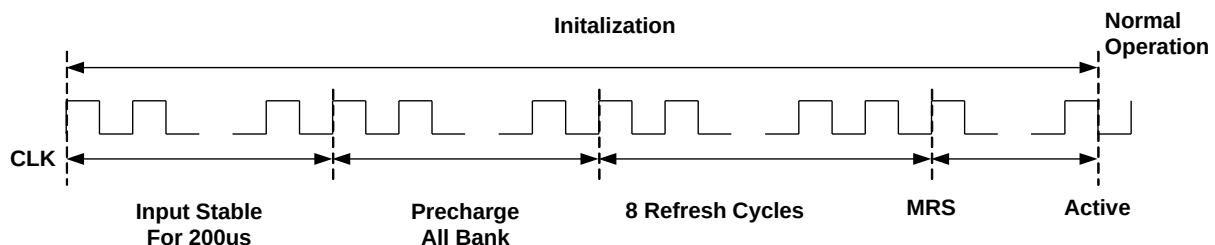
- During the IDLE, normal Read and Write operations of the SDRAM, the precharge and refresh actions are interleaved in between.
- A SDRAM controller (may be embedded in CPU) is generally used to control the data transfer to/from memory.
- The figure below shows the state diagram of the normal operation of the SDRAM.



10.10.2 Initialization

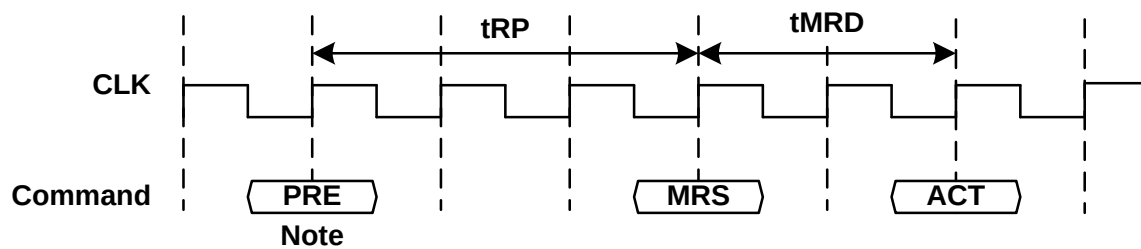
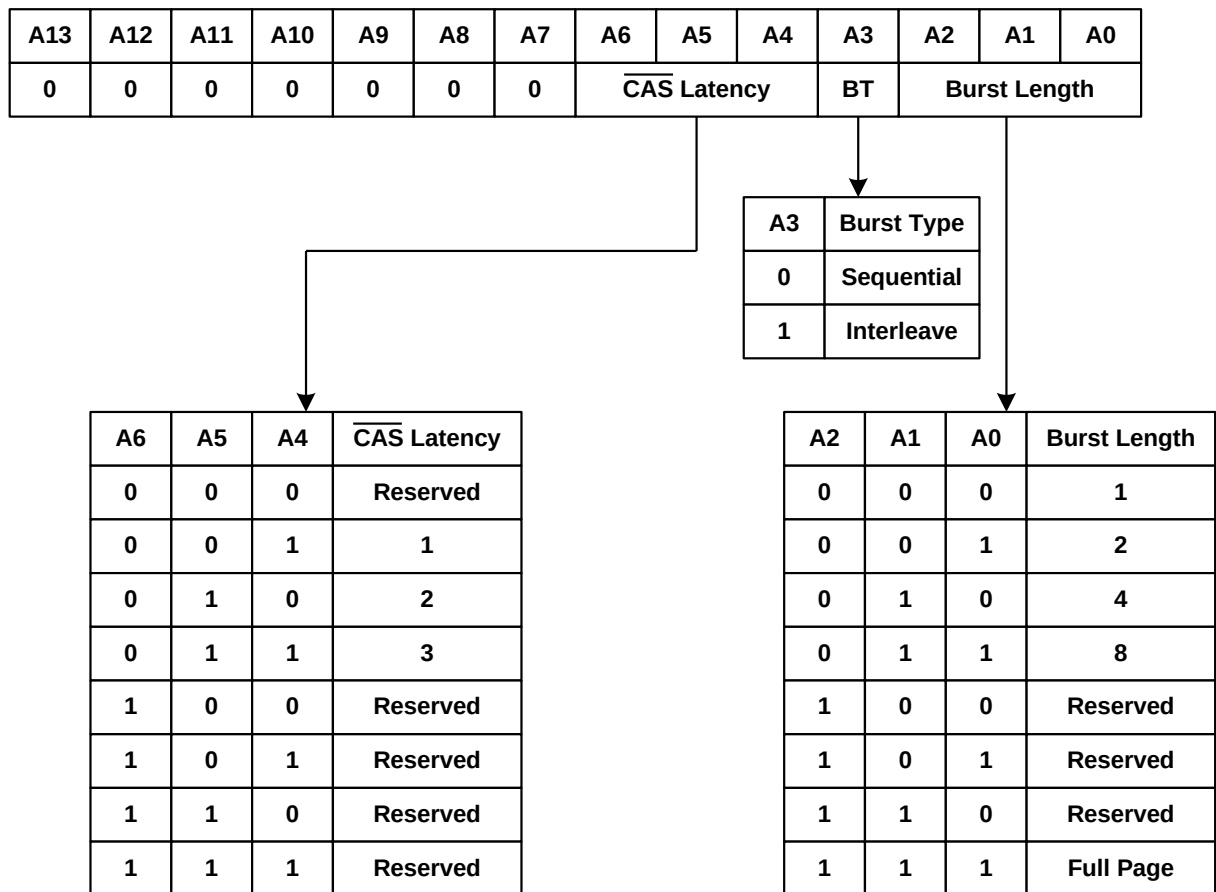
Before issuing the READ and WRITE commands, the SDRAM must be initialized—this is the power-on sequencing of the SDRAM (JEDEC Standard 21C 3.11.5.4):

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs.
2. Maintain stable power, stable clock, and a NOP condition for a minimum of 200 μ s.
3. Issue precharge commands for all banks of the device.
4. Issue 8 or more auto-refresh commands.
5. Issue a MRS (Mode Register Set) command to initialize the mode register



10.10.3 Mode register setting

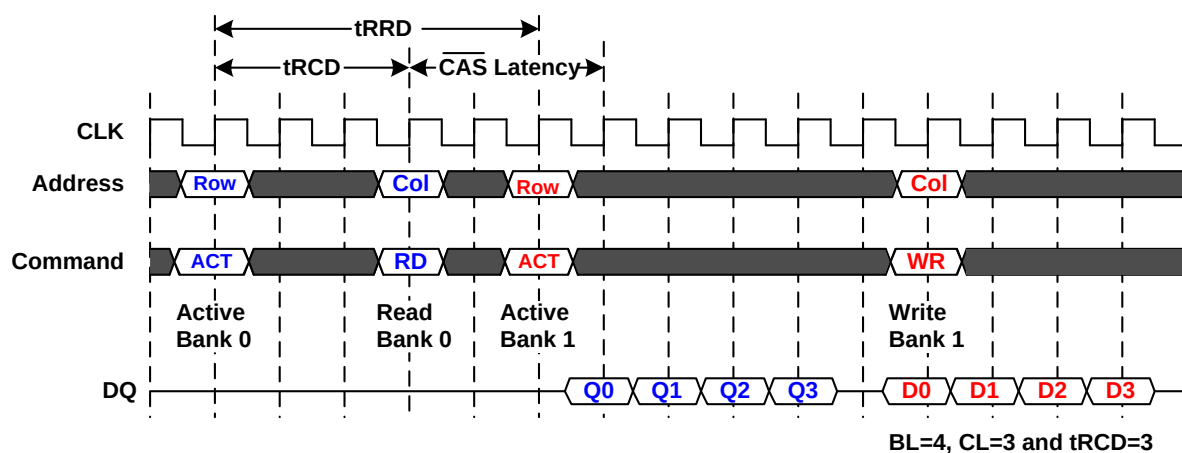
- After power-up sequence, the MRS command must be issued to initialize the device.
- The on-chip mode register (inside the SDRAM) is programmed by user to select the read latency (or $\overline{\text{CAS}}$ latency), burst length, and burst type to be used during READ/WRITE operations.
- This command can be issued only when all banks are in idle state.
- During the MRS cycle, no other commands can be issued.
- The $\overline{\text{CAS}}$ latency, burst type and burst length are programmed to the Mode Register.



Note : 1. All banks should be in precharge state to execute MRS command

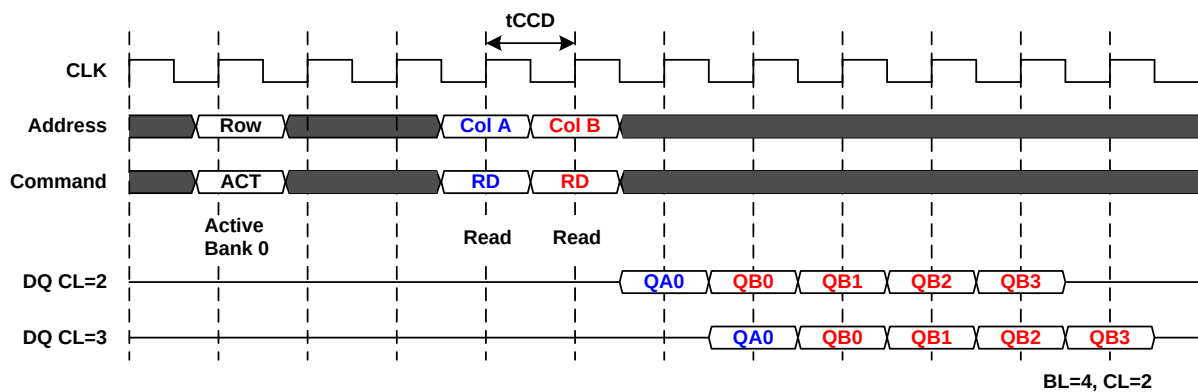
10.10.4 Read/Write operation

- The bank ACTIVE command is issued together with bank and row addresses.
- The row address is latched and the appropriate row in the bank is then selected.
- Data from that row of memory is sensed and latched by the sense amplifiers for later read or write operations.
- After t_{RCD} (row to column address delay), the column address and Read/Write are issued.
- After $\overline{CAS}$ latency delay, the first data can either be read by CPU or written into the memory. The timing diagram below shows the row active, read and write operations.

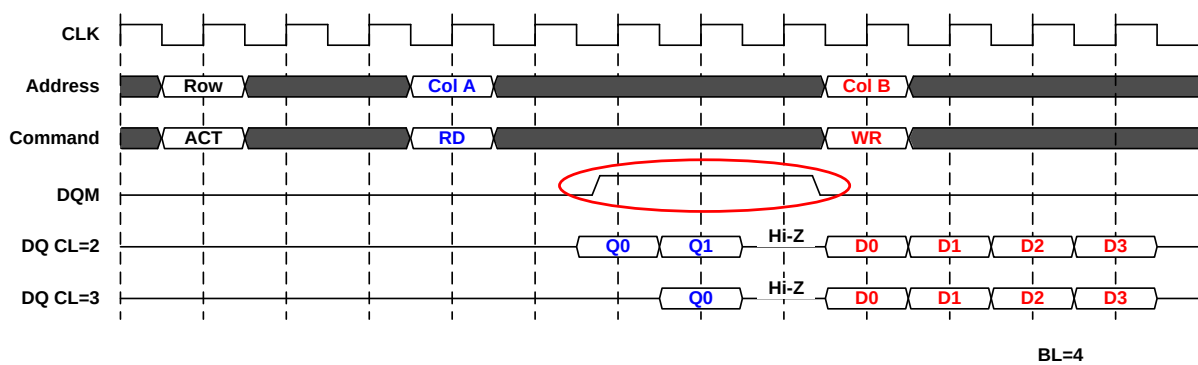


- More timing diagrams for different operations:

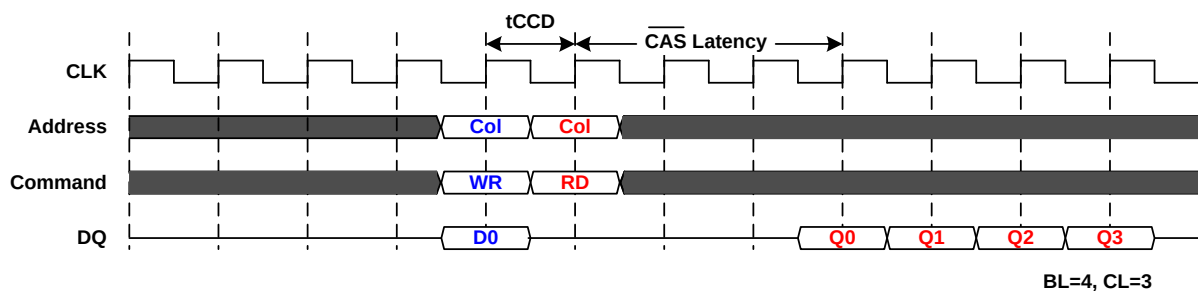
READ TERMINATED BY READ



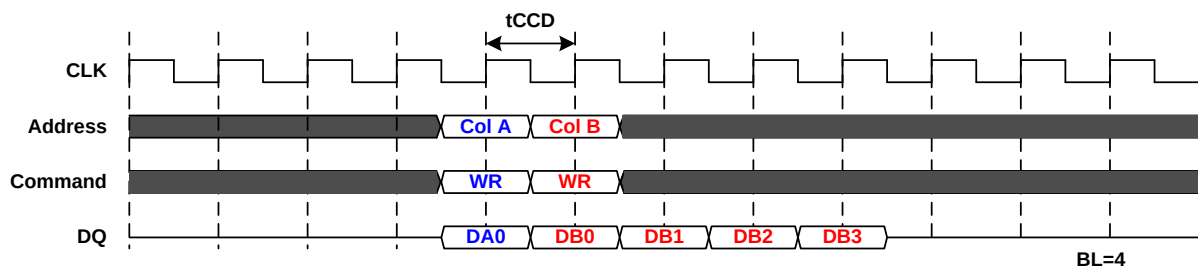
READ TERMINATED BY WRITE AND DQM



WRITE TERMINATED BY READ



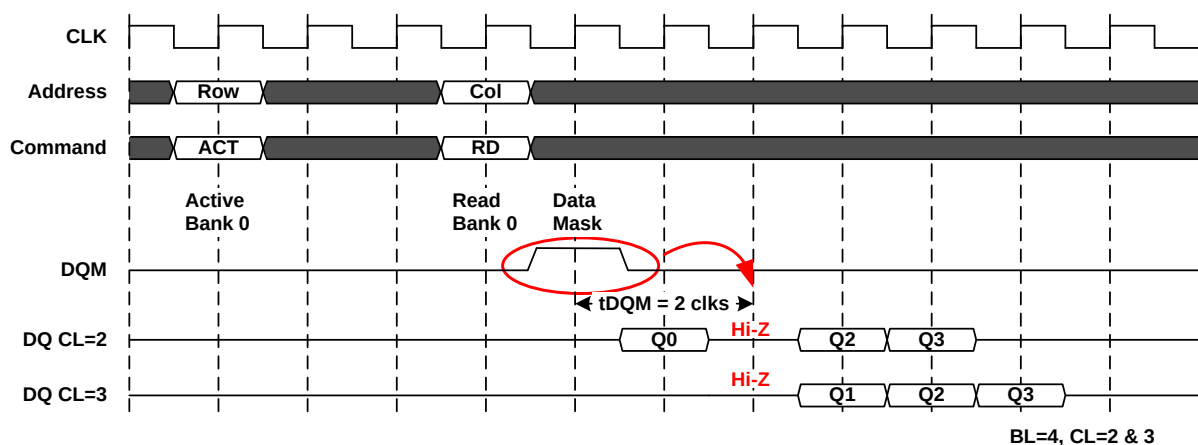
WRITE TERMINATED BY WRITE



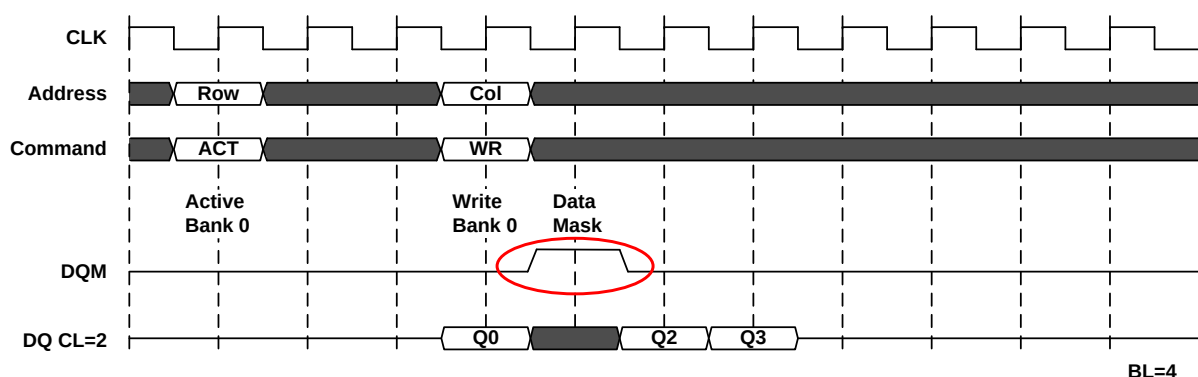
10.10.5 DQM function

- DQM controls output buffers in read mode and masks input data in write mode.
- If data mask is initiated by asserting low on DQM during the read cycle, the data outputs are masked (disabled) and become Hi-Z state after 2 cycles later.
- During the write cycle, DQM mask data input with zero latency.

READ DATA MASK



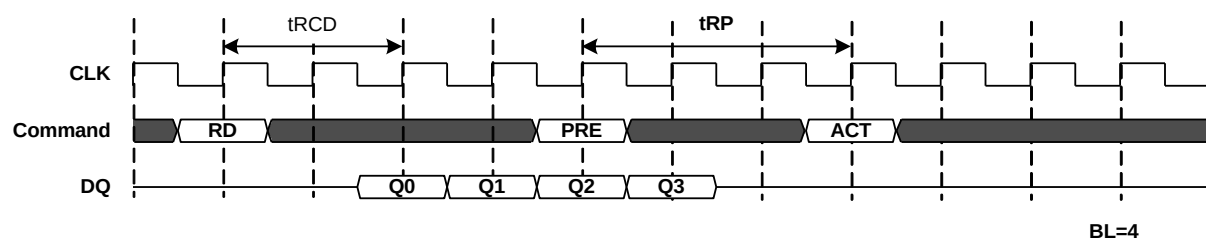
WRITE DATA MASK



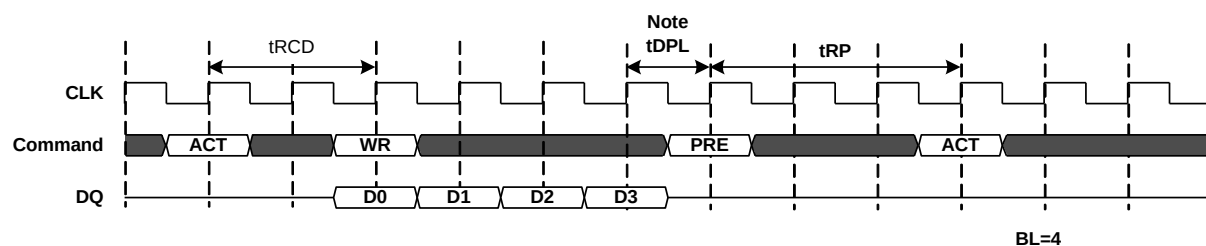
10.10.6 Precharge

- Precharging is a process of deactivating a particular bank or all banks and to charge the bit lines to $V_{cc}/2$ prior reading from bit cells.
- Once a row (page) has been opened to a particular bank within an SDRAM for READ/WRITE operations, at some point, this page must be closed either for performing refresh or activating another page.
- The SDRAM requires the open page to be closed and precharged prior to an ACTIVE command being applied to (i) open another page within the same bank; or (ii) select another bank.
- The precharge function is achieved manually by applying the PRECHARGE command or automatically via the auto precharge command in conjunction with the READ or WRITE command.

PRECHARGE AFTER BURST READ



PRECHARGE AFTER BURST WRITE



Note: t_{DPL} should be required to execute precharge after burst write. $t_{DPL} = 1 \text{ CLK}$ for CAS latency 2 and 3

10.10.7 HY57V641620HG (T-H) – an example

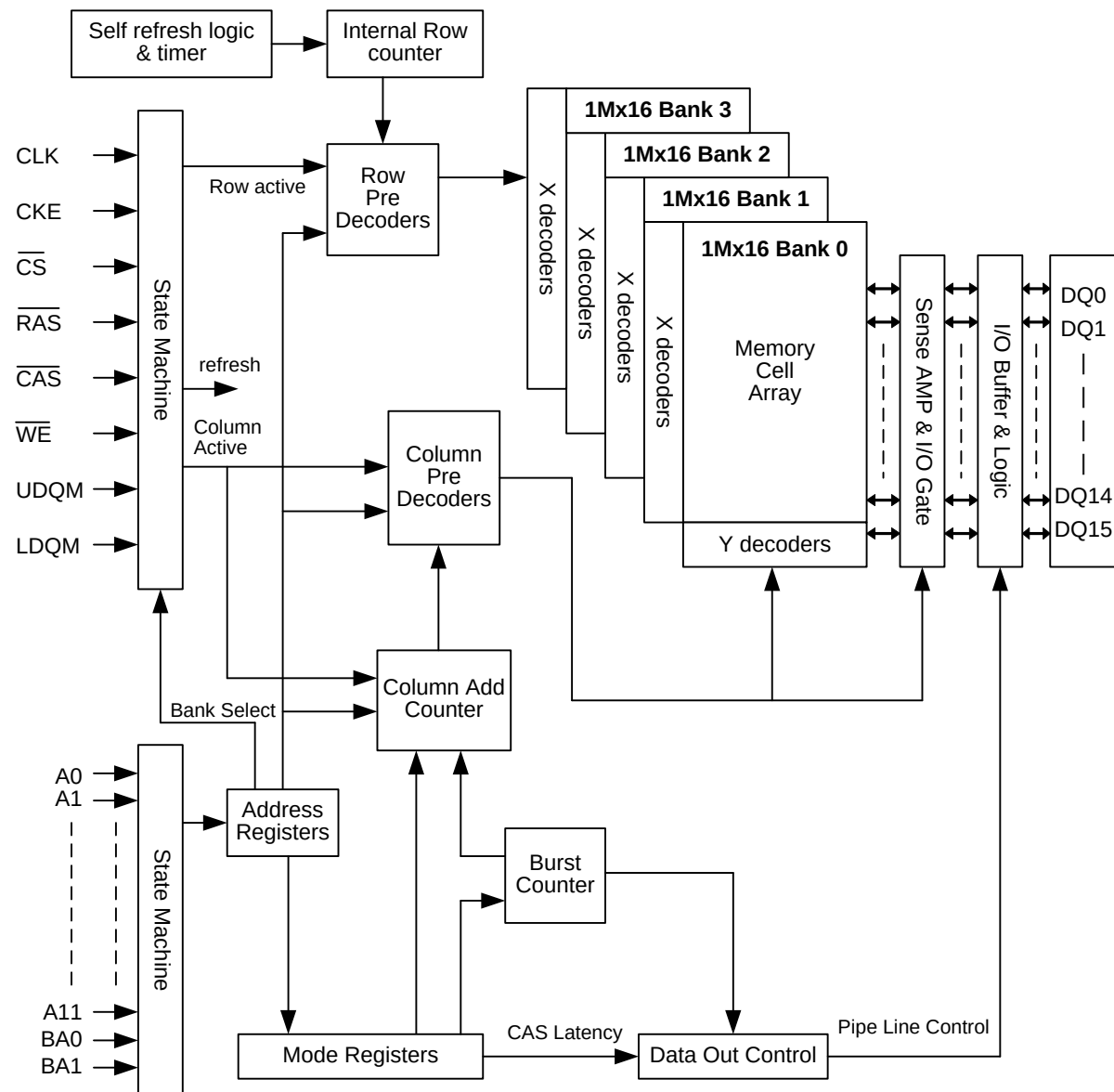
- 4 Banks x 1M x 16Bit Synchronous DRAM
- Inputs/outputs are referenced to +ve edge of system clock
- Data mask function by UDQM or LDQM
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
 - 1, 2, 4, 8 or Full page for Sequential Burst
 - 1, 2, 4 or 8 for Interleave Burst
- Programmable CAS Latency - 2, 3 Clocks

PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
BA0,BA1	Bank Address	Selects bank to be activated during /RAS activity Selects bank to be read/written during /CAS activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
/RAS, /CAS, /WE	Row Address Strobe, Column Address Strobe, Write Enable	/RAS, /CAS and /WE define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM

1Mbit x 4banks x 16 I/O Synchronous DRAM



AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-7		-H		-8		Unit
			Min	Max	Min	Max	Min	Max	
System clock cycle time	CAS Latency = 3	tCK3	7	1000	7.5	1000	8	1000	ns
	CAS Latency = 2	tCK2	10		10		10		ns
Clock high pulse width (note 1)		tCHW	2.5	-	2.5	-	3	-	ns
Clock low pulse width (note 1)		tCLW	2.5	-	2.5	-	3	-	ns
Access time from clock (note 2)	CAS Latency = 3	tAC3	-	5.4		5.4	-	6	ns
	CAS Latency = 2	tAC2	-	6		6	-	6	ns
Data-out hold time		tOH	2.7	-	2.7	-	3	-	ns
Data-Input setup time (note 1)		tDS	1.5	-	1.5	-	2	-	ns
Data-Input hold time (note 1)		tDH	0.8	-	0.8	-	1	-	ns
Address setup time (note 1)		tAS	1.5	-	1.5	-	2	-	ns
Address hold time (note 1)		tAH	0.8	-	0.8	-	1	-	ns
CKE setup time (note 1)		tCKS	1.5	-	1.5	-	2	-	ns
CKE hold time (note 1)		tCKH	0.8	-	0.8	-	1	-	ns
Command setup time (note 1)		tCS	1.5	-	1.5	-	2	-	ns
Command hold time (note 1)		tCH	0.8	-	0.8	-	1	-	ns
CLK to data output in low Z-time		tOLZ	1	-	1.5	-	1	-	ns
CLK to data output in high Z-time	CAS Latency = 3	tOHZ3	2.7	5.4	2.7	5.4	3	6	ns
	CAS Latency = 2	tOHZ2	2.7	5.4	3	5.4	3	6	ns

Note :

- 1.Assume tR / tF (input rise and fall time) is 1ns
- 2.Access times to be measured with input signals of 1v/ns edge rate

AC CHARACTERISTICS II

Parameter		Symbol	-7		-H		-8		Unit
			Min	Max	Min	Max	Min	Max	
RAS Cycle Time	Operation	tRC	63	-	65	-	68	-	ns
	Auto Refresh	tRRC	63	-	65	-	68	-	ns
RAS to CAS Delay		tRCD	20	-	20	-	20	-	ns
RAS Active Time		tRAS	42	120K	45	120K	48	100 K	ns
RAS Precharge Time		tRP	20	-	20	-	20	-	ns
RAS to RAS Bank Active Delay		tRRD	14	-	15	-	16	-	ns
CAS to CAS Delay		tCCD	1	-	1	-	1	-	CLK
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	CLK
Data-In to Precharge Command		tDPL	1	-	1	-	2	-	CLK
Data-In to Active Command		tDAL	4	-	4	-	5	-	CLK
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	CLK
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	CLK
MRS to New Command		tMRD	1	-	1	-	2	-	CLK
Precharge to Data Output Hi-Z	CAS Latency = 3	tPROZ 3	3	-	3	-	3	-	CLK
	CAS Latency = 2	tPROZ 2	2	-	2	-	2	-	CLK
Power Down Exit Time		tPDE	1	-	1	-	1	-	CLK
Self Refresh Exit Time (note 1)		tSRE	1	-	1	-	1	-	CLK
Refresh Time		tREF	-	64	-	64	-	64	ms

Note :

1. A new command can be given tRRC after self refresh exit

DEVICE OPERATING OPTION TABLE : HY57V641620HG(L)T-H

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
133MHz(7.5ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz(15ns)	2CLKs	2CLKs	3CLKs	5CLKs	2CLKs	6ns	3ns

SDRAM timing is usually expressed in **X-X-X-X** for a specific bus frequency, e.g. 3-3-3-8 = CL - tRCD – tRP - tRAS

133 MHz ==> 3-3-3-6, 125 MHz ==> 3-3-3-6

100 MHz ==> 2-2-2-5, 66 MHz ==> 2-2-2-3

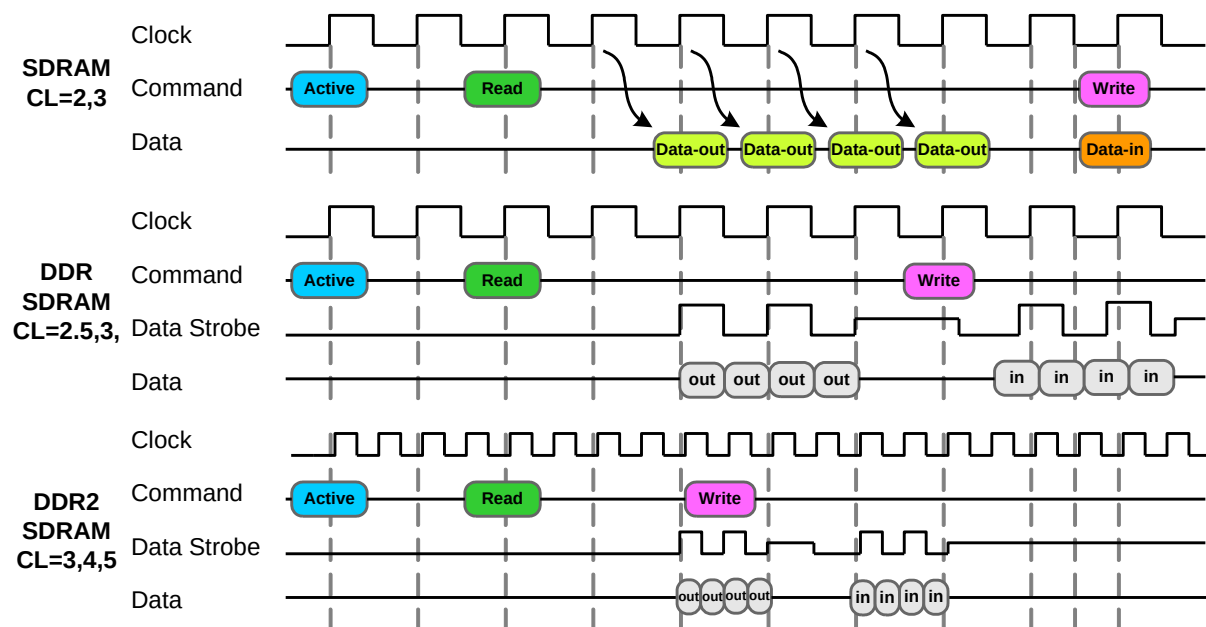
Double data rate (DDR) SDRAM doubles the bandwidth available from SDRAM by transferring data at both edges of the clock.

DDR SDRAM is very similar to single data rate SDRAM in all other characteristics. They use the same signaling technology and the same interface specification.

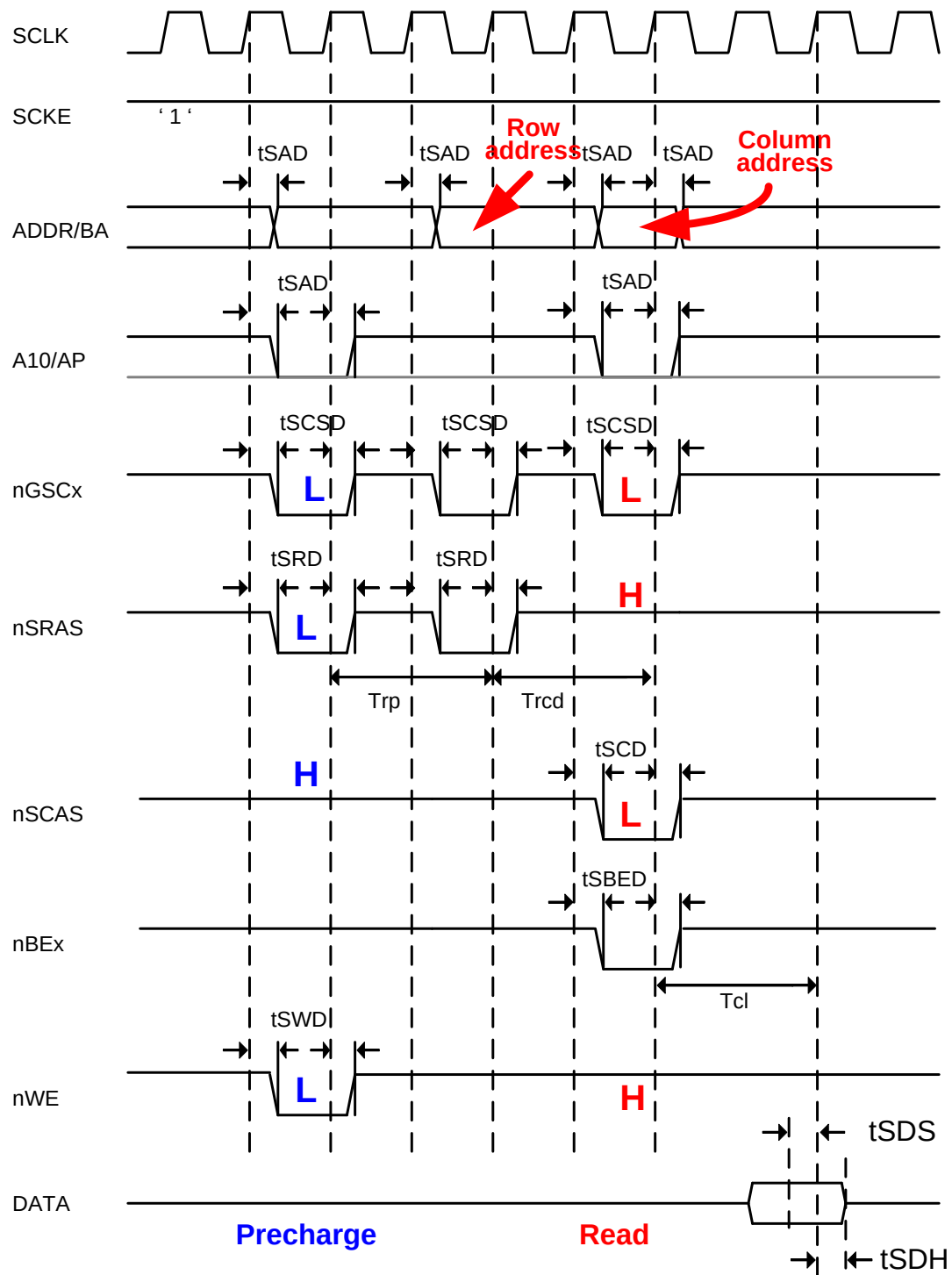
However, DDR-SDRAM's internal transfers from and to the SDRAM array, respectively, read and write twice the number of bits as SDRAM.

10.10.9 DDR2 SDRAM

By means of multiplexing technique, the memory module has a higher bandwidth although the memory cells work at the same low frequency. The data output is double of that of the DDR SDRAM

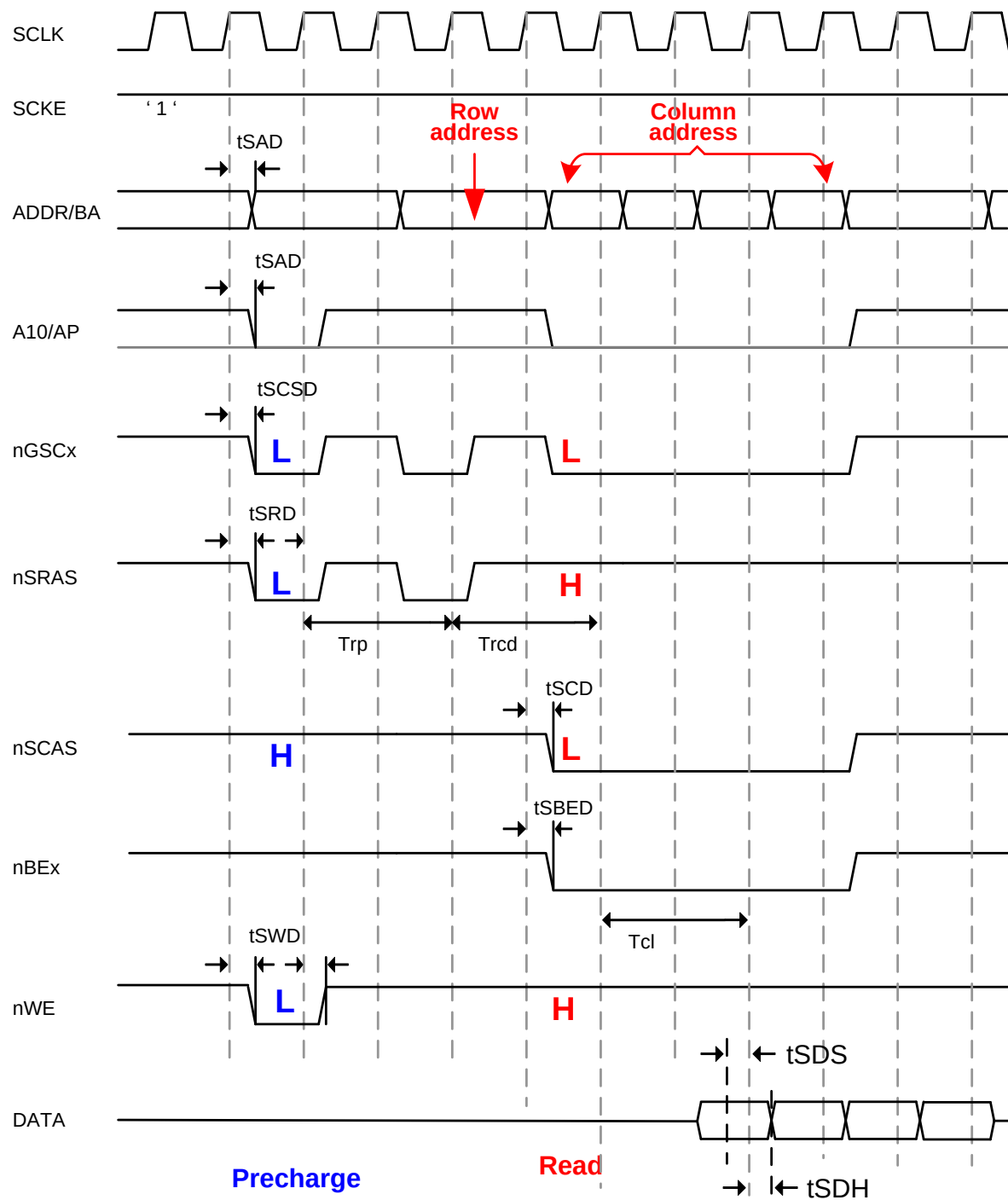


10.11 S3C44B0X's SDRAM timing

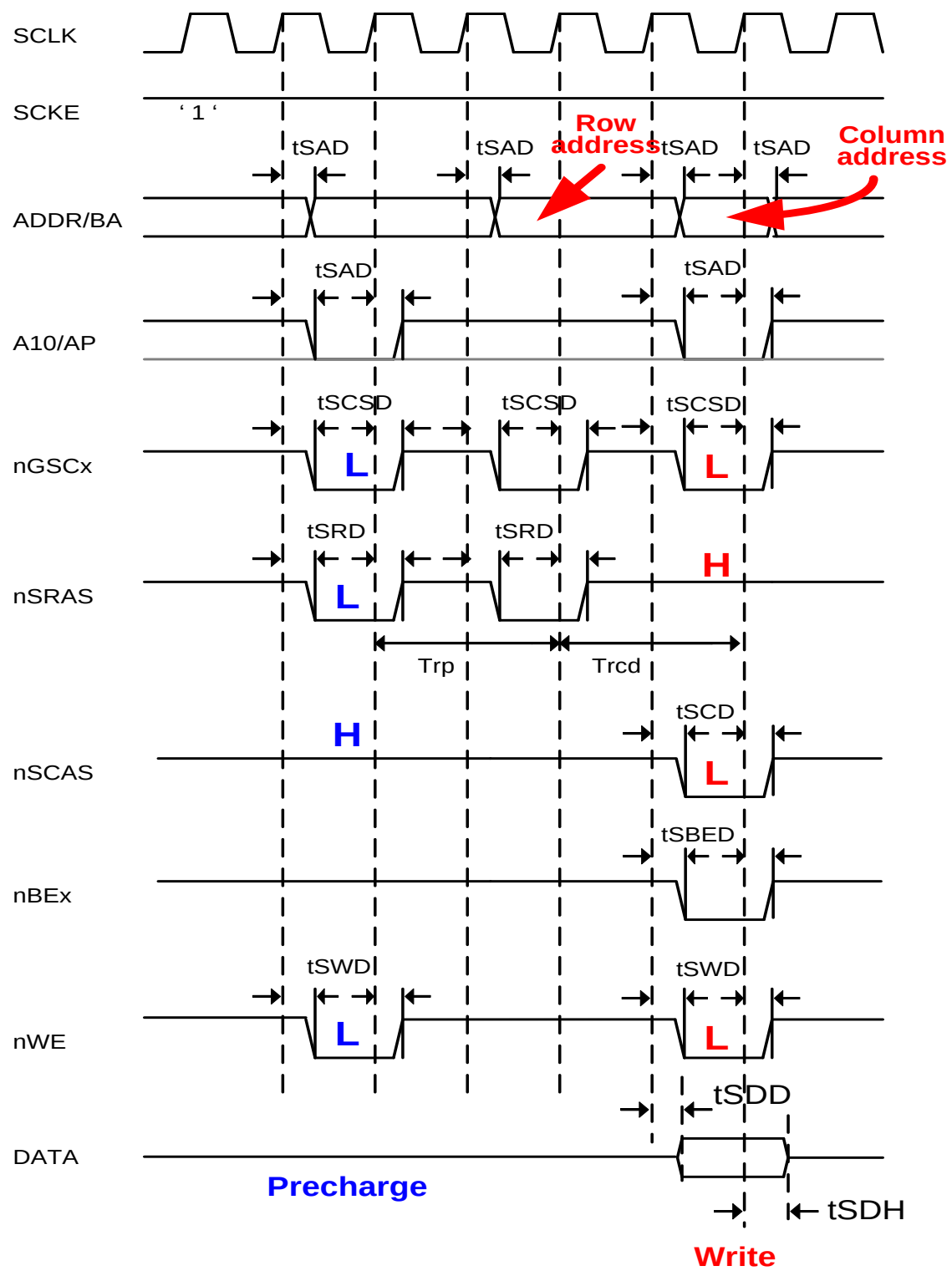


SDRAM Single READ Timing(I) (Trp=2, Trcd=2, Tcl=2)

Command Name	nGCS	nSRAS	nSCAS	nWE
PRECHARGE	L	L	H	L
READ	L	H	L	H
WRITE	L	H	L	L



SDRAM Single Burst READ Timing ($Trp=2$, $Trcd=2$, $Tcl=2$, $DW=16\text{bit}$, $BL=4$)

SDRAM Single Write Timing ($Trp=2$, $Trcd=2$)

Memory Interface Timing Constants

(VDDP :3.3V, VDDI:2.5V, Ta = 25°C, PLCAP = 70pf, max/min = typ ± 30%)

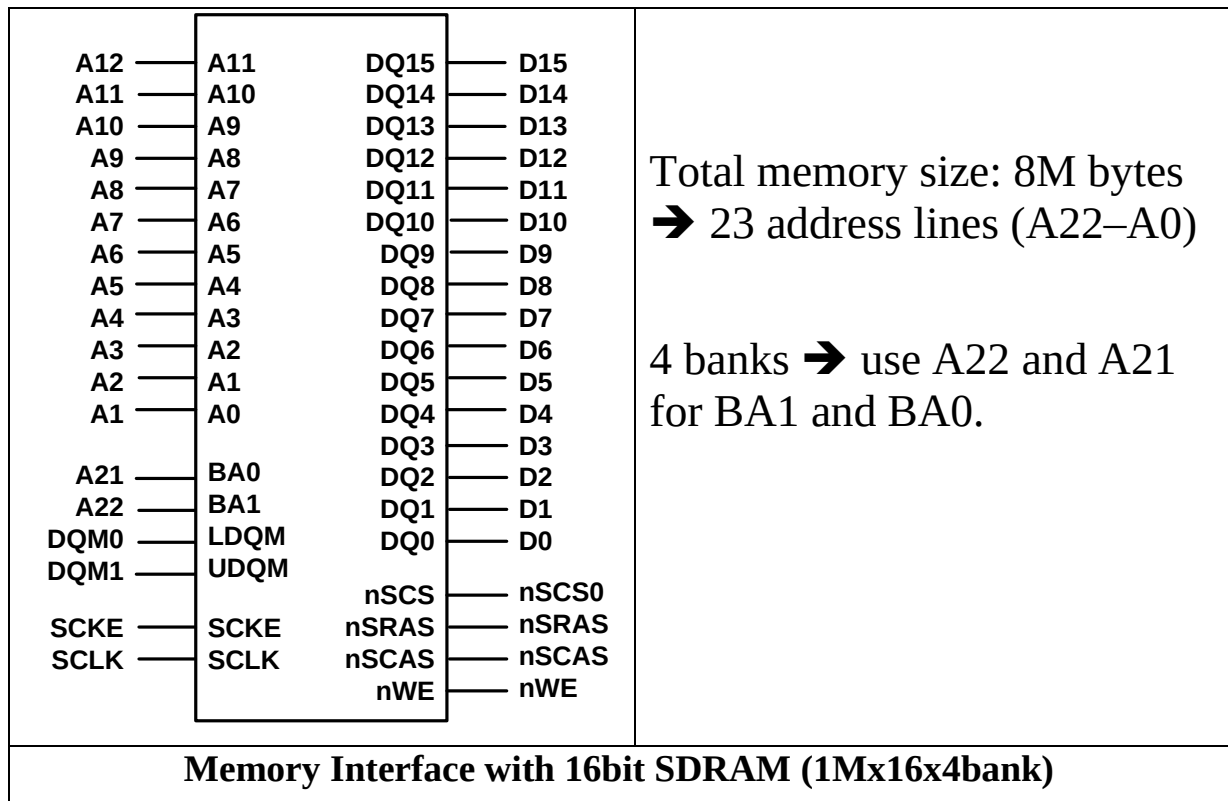
Parameter	Symbol	Min	Typ	Max	Unit
SDRAM Address Delay	tSAD	–	4	–	ns
SDRAM Chip Select Delay	tSCSD	–	4	–	ns
SDRAM Row active Delay	tSRD	–	4	–	ns
SDRAM Column active Delay	tSCD	–	4	–	ns
SDRAM Byte Enable Delay	tSBED	–	5	–	ns
SDRAM Write enable Delay	tSWD	–	5	–	ns
SDRAM read Data Setup time	tSDS	–	4	–	ns
SDRAM read Data Hold time	tSDH	–	0	–	ns
SDRAM output Data Delay	tSDD	–	8	–	ns
SDRAM Clock Enable Delay	Tcked	–	5	–	ns

10.12 Hardware interface for S3C44B0X and SDRAM

The following hardware signals are used to interface SDRAM.

DRAM/SDRAM		
Signal	I/O	Description
nSRAS	O	SDRAM Row Address Strobe
nSCAS	O	SDRAM Column Address Strobe
nSCS[1:0]	O	SDRAM Chip Select
nWE	O	Write Enable
BA[1,0]	O	Bank Address Selection
DQM[3:0]	O	SDRAM Data Mask
SCLK	O	SDRAM Clock
SCKE	O	SDRAM Clock Enable

Note that DRAM/EDO DRAM/SDRAM can only be connected to Banks 6 & 7, and must be defined in registers BANKCON6 and BANKCON7.



The detail connections of BA1 and BA0 of S3C44B0X for different types SDRAM are given in the following table.

Bank Size	Bus Width	Base Component	Memory Configuration	Bank Address
2MByte	x8	16Mbit	(1M x 8 x 2Bank) x 1	A20
	x16		(512K x 16 x 2B) x 1	
4MB	x8	16Mb	(2M x 4 x 2B) x 2	A21
	x16		(1M x 8 x 2B) x 2	
	x32		(512K x 16 x 2B) x 2	
8MB	x16	16Mb	(2M x 4 x 2B) x 4	A22
	x32		(1M x 8x 2B) x 4	
	x8	64Mb	(4M x 8 x 2B) x 1	A[22:21]
	x8		(2M x 8 x 4B) x 1	
	x16		(2M x 16 x 2B) x 1	A22
	x16		(1M x 16 x 4B) x 1	A[22:21]
	x32		(512K x 32 x 4B) x 1	

Bank Size	Bus Width	Base Component	Memory Configuration	Bank Address
16MB	x32	16Mb	(2M x 4 x 2B) x 8	A23
	x8	64Mb	(8M x 4 x 2B) x 2	
	x8		(4M x 4 x 4B) x 2	A[23:22]
	x16		(4M x 8 x 2B) x 2	A23
	x16		(2M x 8 x 4B) x 2	A[23:22]
	x32		(2M x 16 x 2B) x 2	A23
	x32		(1M x 16 x 4B) x 2	A[23:22]
	x8	128Mb	(4M x 8 x 4B) x 1	
	x16		(2M x 16 x 4B) x 1	
32MB	x16	64Mb	(8M x 4 x 2B) x 4	A24
	x16		(4M x 4 x 4B) x 4	A[24:23]
	x32		(4M x 8 x 2B) x 4	A24
	x32		(2M x 8 x 4B) x 4	A[24:23]
	x16	128Mb	(4M x 8 x 4B) x 2	
	x32		(2M x 16 x 4B) x 2	
	x8	256Mb	(8M x 8 x 4B) x 1	
	x16		(4M x 16 x 4B) x 1	

Important note:

The number of address lines of the DRAM and SDRAM devices is much less than the size requirement.

Why?

CPU accesses memory location by sending Row address first and followed by the column address.

The row and column address are placed onto the same set of address lines in multiplexed manner (CPU's memory controller takes care the action).

Thus, only a subset of physical address lines from CPU is connected to the memory device.

10.13 Interfacing S3C44B0X with HY57V641620HG (T-H)

- The design of SDRAM must be conformed to JEDEC standard for compatibility purpose.
- Therefore, memory devices of different size configurations can be directly replaced without redesigning the PCB due to the same footprint design.
- For example the pin assignment for 64M/128M SDRAM devices (16Mx4, 8Mx8, 4Mx16, 16Mx8, and 8Mx16)

			4M x 16 / 8M x 16 8M x 8 / 16M x 8 16M x 4				
VCC	VCC	VCC	1	54	VSS	VSS	VSS
DQ0	DQ0	NC	2	53	NC	DQ7	DQ15
VCCQ	VCCQ	VCCQ	3	52	VSSQ	VSSQ	VSSQ
DQ1	NC	NC	4	51	NC	NC	DQ14
DQ2	DQ1	DQ0	5	50	DQ3	DQ6	DQ13
VSSQ	VSSQ	VSSQ	6	49	VCCQ	VCCQ	VCCQ
DQ3	NC	NC	7	48	NC	NC	DQ12
DQ4	DQ2	NC	8	47	NC	DQ5	DQ11
VCCQ	VCCQ	VCCQ	9	46	VSSQ	VSSQ	VSSQ
DQ5	NC	NC	10	45	NC	NC	DQ10
DQ6	DQ3	DQ1	11	44	DQ2	DQ4	DQ9
VSSQ	VSSQ	VSSQ	12	43	VCCQ	VCCQ	VCCQ
DQ7	NC	NC	13	42	NC	NC	DQ8
VCC	VCC	VCC	14	41	VSS	VSS	VSS
DQML	NC	NC	15	40	RESERVED	RESERVED	RESERVED
WE#	WE#	WE#	16	39	DQM	DQM	DQMH
CAS#	CAS#	CAS#	17	38	CLK	CLK	CLK
RAS#	RAS#	RAS#	18	37	CLKE	CLKE	CLKE
CS#	CS#	CS#	19	36	RESERVED	RESERVED	RESERVED
A13(BA0)	A13(BA0)	A13(BA0)	20	35	A11	A11	A11
A12(BA1)	A12(BA1)	A12(BA1)	21	34	A9	A9	A9
A10(AP)	A10(AP)	A10(AP)	22	33	A8	A8	A8
A0	A0	A0	23	32	A7	A7	A7
A1	A1	A1	24	31	A6	A6	A6
A2	A2	A2	25	30	A5	A5	A5
A3	A3	A3	26	29	A4	A4	A4
VCC	VCC	VCC	27	28	VSS	VSS	VSS

HY57V641620 is organized as 4 banks of 1M × 16 (**4M x 16 DEVICE**).

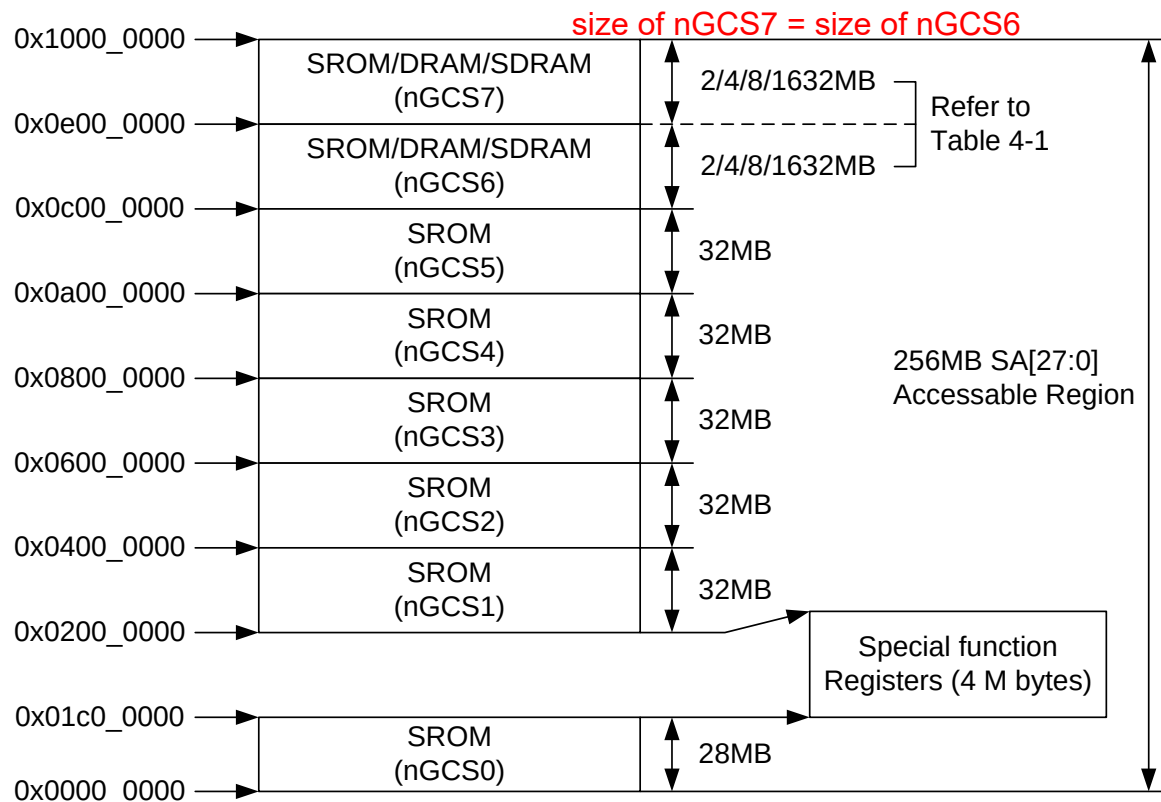


With jumper control for BA1 and BA0:

16M-bytes memory device uses R78 and R82 (A22 & A23)

10.14 Memory Controller of S3C44B0X

Memory Map of S3C44B0X:



- Bank 0 is divided into two regions: 28 Mbytes for program/data and 4 M Bytes for Special Function Registers.
- Banks 1 – 5 are free space for connecting ROM, SRAM and memory mapped I/O peripheral I/O devices.
- Banks 6 – 7 are for connecting external memory devices: ROM, SRAM, FP DRAM, EDO DRAM and SDRAM and it support the following configuration:

Bank	Support				Not support	
Bank7	SROM	DRAM	SDRAM	SROM	SDRAM	DRAM
Bank6	DRAM	SROM	SROM	SDRAM	DRAM	SDRAM

NOTE: SROM means ROM or SRAM type memory

- The memory bank configuration and timing parameters of all banks must be programmed to the appropriate registers for proper operation.

Bus Width & Wait Status Control Register

Register	Address	R/W	Description	Reset Value
BWCON	0x01C80000	R/W	Bus Width & Wait Status Control Register	0x000000

BWCON	Bit	Description	Initial state
ST7	[31]	This bit determines SRAM for using UB/LB for bank 7 0 = Not using UB/LB (Pin[14:11] is dedicated nWBE[3:0]) 1 = Using UB/LB (Pin[14:11] is dedicated nBE[3:0])	0
WS7	[30]	This bit determines WAIT status for bank 7 (If bank7 has DRAM or SDRAM, WAIT function is not supported) 0 = WAIT disable 1 = WAIT enable	0
DW7	[29:28]	These two bits determine data bus width for bank 7 00 = 8-bit 01 = 16-bit, 10 = 32-bit	0
ST6	[27]	This bit determines SRAM for using UB/LB for bank 6 0 = Not using UB/LB (Pin[14:11] is dedicated nWBE[3:0]) 1 = Using UB/LB (Pin[14:11] is dedicated nBE[3:0])	0
WS6	[26]	This bit determines WAIT status for bank 6 (If bank6 has DRAM or SDRAM, WAIT function is not supported) 0 = WAIT disable, 1 = WAIT enable	0
DW6	[25:24]	These two bits determine data bus width for bank 6 00 = 8-bit 01 = 16-bit, 10 = 32-bit	0

ST5	[23]	This bit determines SRAM for using UB/LB for bank 5 0 = Not using UB/LB (Pin[14:11] is dedicated WBE[3:0]) 1 = Using UB/LB (Pin[14:11] is dedicated nBE[3:0])	0
ST4	[19]		
ST3	[15]		
ST2	[11]		
ST1	[7]		
WS5	[22]	This bit determines WAIT status for bank 5 0 = WAIT disable 1 = WAIT enable	0
WS4	[18]		
WS3	[14]		
WS2	[10]		
WS1	[6]		
DW5	[21:20]	These two bits determine data bus width for bank 5 00 = 8-bit 01 = 16-bit 10 = 32-bit	0
DW4	[17:16]		
DW3	[13:12]		
DW2	[9:8]		
DW1	[5:4]		

DW0	[2:1]	Indicates data bus width for bank 0 (read only) 00 = 8-bit 01 = 16-bit, 10 = 32-bit The states are selected by OM[1:0] pins	-
ENDIAN	[[0]	Indicates endian mode (read only) 0 = Little endian 1 = Big endian The states are selected by ENDIAN pins	-

Note: Bank 0 is important for system boot-up.

BANK CONTROL REGISTER (BANKCONn: nGCS0-nGCS5)

Register	Address	R/W	Description	Reset Value
BANKCON0	0x01C80004	R/W	Bank 0 control register	0x0700
BANKCON1	0x01C80008	R/W	Bank 1 control register	0x0700
BANKCON2	0x01C8000C	R/W	Bank 2 control register	0x0700
BANKCON3	0x01C80010	R/W	Bank 3 control register	0x0700
BANKCON4	0x01C80014	R/W	Bank 4 control register	0x0700
BANKCON5	0x01C80018	R/W	Bank 5 control register	0x0700

BANKCONn	Bit	Description	Initial State
Tacs	[14:13]	Address set-up before nGCSn 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tcos	[12:11]	Chip selection set-up nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tacc	[10:8]	Access cycle 000 = 1 clock 010 = 2 clocks 100 = 3 clocks 110 = 4 clocks 001 = 6 clocks 011 = 8 clocks 101 = 10 clocks 111 = 14 clocks	111
Toch	[7:6]	Chip selection hold on nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tcah	[5:4]	Address hold time on nGCSn 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tpac	[3:2]	Page mode access cycle @ Page mode 00 = 2 clock 01 = 3 clock 10 = 4 clocks 11 = 6 clocks	00
PMC	[1:0]	Page mode configuration 00 = normal (1 data) 01 = 4 data 10 = 8 data 11 = 16 data	00

BANK CONTROL REGISTER (BANKCONn: nGCS6-nGCS7)

Register	Address	R/W	Description	Reset Value
BANKCON6	0x01C8001C	R/W	Bank 6 control register	0x18008
BANKCON7	0x01C80020	R/W	Bank 7 control register	0x18008

BANKCONn	Bit	Description	Initial State
MT	[16:15]	These two bits determine the memory type for banks 6 & 7 00 = ROM or SRAM 01 = FP DRAM 10 = EDO DRAM 11 = Sync. DRAM	11

Memory Type = ROM or SRAM [MT=00] (15-bit)

Tacs	[14:13]	Address set-up before nGCS 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tcos	[12:11]	Chip selection set-up nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clock	00
Tacc	[10:8]	Access cycle 000 = 1 clock 010 = 3 clocks 100 = 6 clocks 110 = 10 clocks 001 = 2 clocks 011 = 4 clocks 101 = 8 clocks 111 = 14 clocks	111
Toch	[7:6]	Chip selection hold on nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tcah	[5:4]	Address hold time on nGCSn 00 = 0 clock 01 = 1clock 10 = 2 clocks 11 = 4 clocks	00
Tpac	[3:2]	Page mode access cycle @ Page mode 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 6 clocks	00
PMC	[1:0]	Page mode configuration 00 = normal (1 data) 10 = 8 consecutive accesses 01 = 4 consecutive accesses 11 = 16 consecutive accesses	00

Memory Type = FP DRAM [MT=01] or EDO DRAM [MT=10] (6-bit)**Memory Type = SDRAM [MT=11] (4-bit)**

Trcd	[3:2]	RAS to CAS delay 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks	10
SCAN	[1:0]	Column address number 00 = 8-bit 01 = 9-bit 10 = 10-bit	00

selection from datasheet

tRCD = 20ns, 66MHz → tCYC = 15.15ns → tRCD = 2 clocks

Column address: CA0 ~ CA7

Thus, **rBANKCON6 = 0x00018000**replace
by

REFRESH CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
REFRESH	0x01C80024	R/W	DRAM/SDRAM refresh control register	0xac0000

REFRESH	Bit	Description	Initial State
REFEN	[23]	DRAM/SDRAM Refresh Enable 0 = Disable 1 = Enable (self or CBR/auto refresh)	1
TREFMD	[22]	DRAM/SDRAM Refresh Mode 0 = CBR/Auto Refresh 1 = Self Refresh In self-refresh time, the DRAM/SDRAM control signals are driven to the appropriate level.	0
Trp	[21:20]	DRAM/SDRAM RAS pre-charge Time DRAM : 00 = 1.5 clocks 01 = 2.5 clocks 10 = 3.5 clocks 11 = 4.5 clocks SDRAM : 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = Not support	10
Trc	[19:18]	SDRAM RC minimum Time 00 = 4 clocks 1 = 5 clocks 10 = 6 clocks 11 = 7 clocks	11
Tchr	[17:16]	CAS Hold Time (DRAM) 00 = 1 clock 01 = 2 clocks 10 = 3 clocks 11 = 4 clocks	00
Reserved	[15:11]	Not use	00000
Refresh Counter	[10:0]	DRAM/SDRAM refresh count value. Refresh period = $(2^{11} - \text{refresh_count} + 1) / \text{MCLK}$ e.g. If refresh period is 15.6 us and MCLK is 60 MHz, the refresh count is as follows; refresh count = $2^{11} + 1 - 60 \times 15.6 = 1113 = \text{0x459}$	0

Enable refresh : REFEN = 1

CBR/Auto Refresh: TREFMD = 0

Precharge time = 20ns (2 clocks) → tRP = 00

Minimum RC = 65ns (5 clocks) → tRC = 01 4096 refresh cycles / 64ms

Tchr = 3 clocks = 10 (it is only for DRAM)

Refresh period = 64ms/4096 = 15.625μs

For 60MHz CPU clock

Refresh counter = $2^{11} + 1 - 60 \times 15.625 = 1113 = \text{0x459}$

Thus, **rREFRESH = 0x00860459**

Refresh counter = $2^{11} + 1 - 66 \times 15.625 = 1017 = \text{0x3F9}$

For 66MHz CPU clock

Thus, **rREFRESH = 0x008603F9**

SDRAM MODE REGISTER SET REGISTER (MRSR)

Register	Address	R/W	Description	Reset Value
MRSRB6	0x01C8002C	R/W	Mode register set register bank6	xxx
MRSRB7	0x01C80030	R/W	Mode register set register bank7	xxx

MRSR	Bit	Description	Initial State
Reserved	[11:10]	Not use	—
WBL	[9]	Write burst length 0 is the recommended value	x
TM	[8:7]	Test mode 00: mode register set, 01, 10, 11: reserved	xx
CL	[6:4]	CAS latency 000 = 1 clock, 010 = 2 clocks, 011=3 clocks the others = reserved	xxx
BT	[3]	Burst type 0: Sequential (recommended) 1: N/A	x
BL	[2:0]	Burst length 000: 1 the others: N/A	xxx

Write burst length: WBL = 0

Mode register: TM = 00

CAS latency (2 clocks): CL = 010

Burst type (sequential): BT = 0

Burst length (1): BL = 000

Thus, **rMRSRB6 = 0x00000020**

BANKSIZE REGISTER

Register	Address	R/W	Description	Reset Value
BANKSIZE	0x01C80028	R/W	Flexible bank size register	0x0

BANKSIZE	Bit	Description	Initial State
SCLKEN	[4]	SCLK will be generated only during SDRAM access cycle. This feature will reduce the power consumption. 1 is recommended. 0 = normal SCLK 1 = SCLK for reducing power consumption	0
Reserved	[3]	Not use	0
BK76MAP	[2:0]	BANK6/7 memory map 000 = 32M/32M 100 = 2M/2M 101 = 4M/4M 110 = 8M/8M 111 = 16M/16M	000

For 32M Bytes in Bank 6, then **rBANKSIZE = 0x10**

For 8M Bytes in Bank 6, then **rBANKSIZE = 0x16 (actual size)**

General notes:

The memory devices within the same memory bank:

- i. **MUST** be of the same type;
- ii. Registers settings must satisfy all devices – generally fit for the slowest device.

Initial setup of the memory registers:

For the EmbestIDE software, the command script file ev40boot.cs will be downloaded to the CPU when connecting to the development board.

The basic setting of the registers is defined in this file:

```

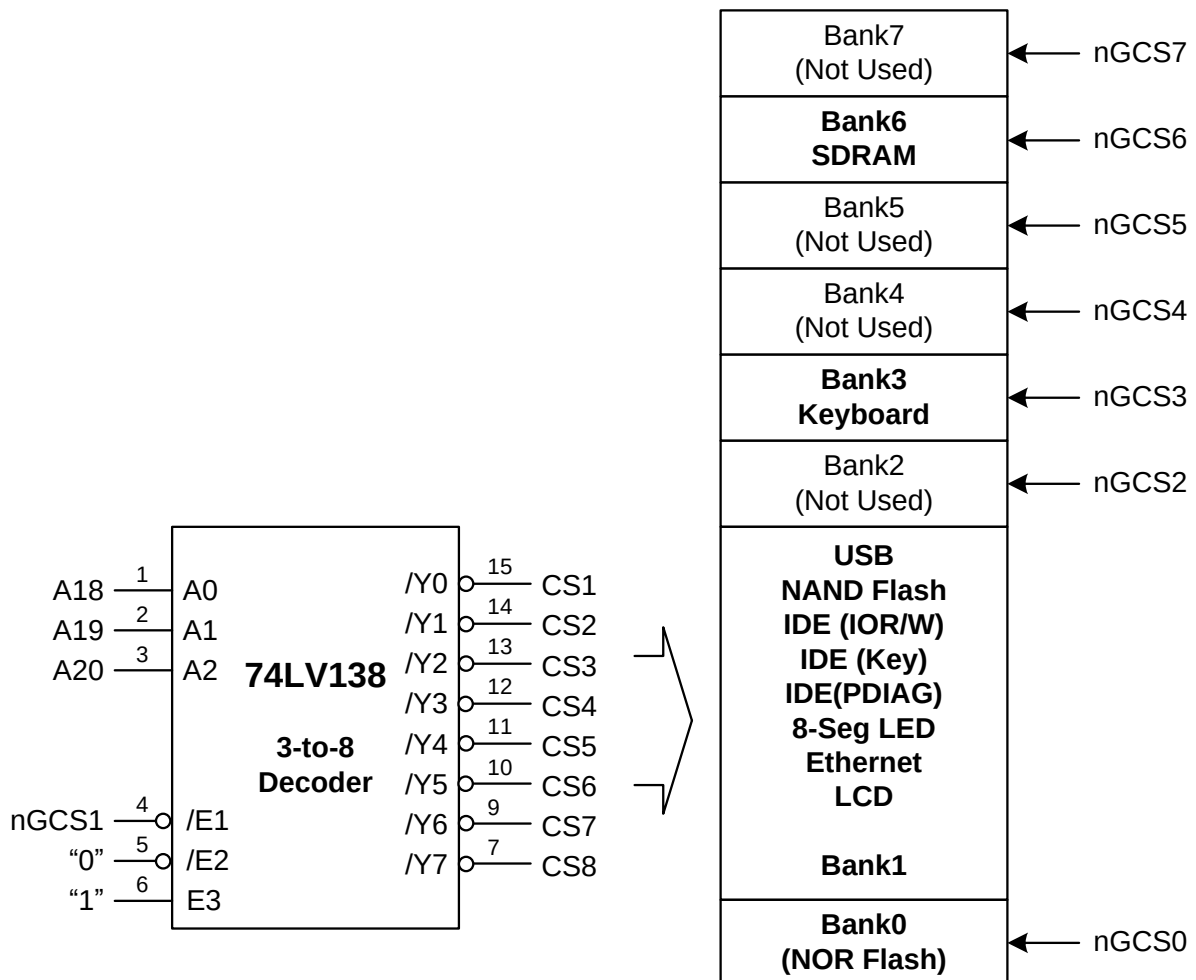
reset
memwrite 0x01D30000 0x00000000 ; WTCN (disable watch dog)
memwrite 0x01E0000C 0x07FFFFFF ; INTMSK (disable all interrupt)
memwrite 0x01E00024 0xFFFFFFFF ; clear all interrupt
memwrite 0x01C80000 0x11110102 ; BWSCON
memwrite 0x01C80004 0x00000600 ; BANKCON0
memwrite 0x01C80008 0x00007FFC ; BANKCON1
memwrite 0x01C8000C 0x00007FFC ; BANKCON2
memwrite 0x01C80010 0x00007FFC ; BANKCON3
memwrite 0x01C80014 0x00007FFC ; BANKCON4
memwrite 0x01C80018 0x00007FFC ; BANKCON5
memwrite 0x01C8001C 0x00018000 ; BANKCON6
memwrite 0x01C80020 0x00018000 ; BANKCON7
memwrite 0x01C80024 0x00860459 ; REFRESH
memwrite 0x01C80028 0x00000010 ; BANKSIZE
memwrite 0x01C8002C 0x00000020 ; MRSRB6
memwrite 0x01C80030 0x00000020 ; MRSRB7

```

BANKCON0: Access time of NOR flash is 55ns and CPU clock frequency of 60 MHz, Tacc is set to 4 clock cycles (an estimation directly from $55/15 = 3.5$, margin is not sufficient from theoretical point of view. BUT it works ==> the access

time may be less than 55 ns and/or CPU timing is better than the specified ones !!).

The register settings above are for specific memory map design and devices used on the development board as shown in the following diagram and table:



The setting for BANKCON1 must satisfy the timing requirement of the slowest devices

Peripheral	CS	CS register	Address space
NOR Flash	nGCS0	BANKCON0	0x0000_0000~0x01BF_FFFF
SDRAM	nGCS6	BANKCON6	0x0C00_0000~0x0DFF_FFFF
USB	CS1	BANKCON1	0x0200_0000~0x0203_FFFF
NAND Flash	CS2	BANKCON1	0x0204_0000~0x0207_FFFF
IDE (IOR/W)	CS3	BANKCON1	0x0208_0000~0x020B_FFFF
IDE (button)	CS4	BANKCON1	0x020C_0000~0x020F_FFFF
IDE (PDIAG)	CS5	BANKCON1	0x0210_0000~0x0213_FFFF
8-seg LED	CS6	BANKCON1	0x0214_0000~0x0217_FFFF
Ethernet	CS7	BANKCON1	0x0218_0000~0x021B_FFFF
LCD	CS8	BANKCON1	0x021C_0000~0x021F_FFFF
Not Used	nGCS2	BANKCON2	0x0400_0000~0x05FF_FFFF
Keyboard	nGCS3	BANKCON3	0x0600_0000~0x07FF_FFFF
Not Used	nGCS4	BANKCON4	0x0800_0000~0x09FF_FFFF
Not Used	nGCS5	BANKCON5	0x0A00_0000~0x0BFF_FFFF
Not Used	nGCS7	BANKCON7	0x0E00_0000~0x1FFF_FFFF