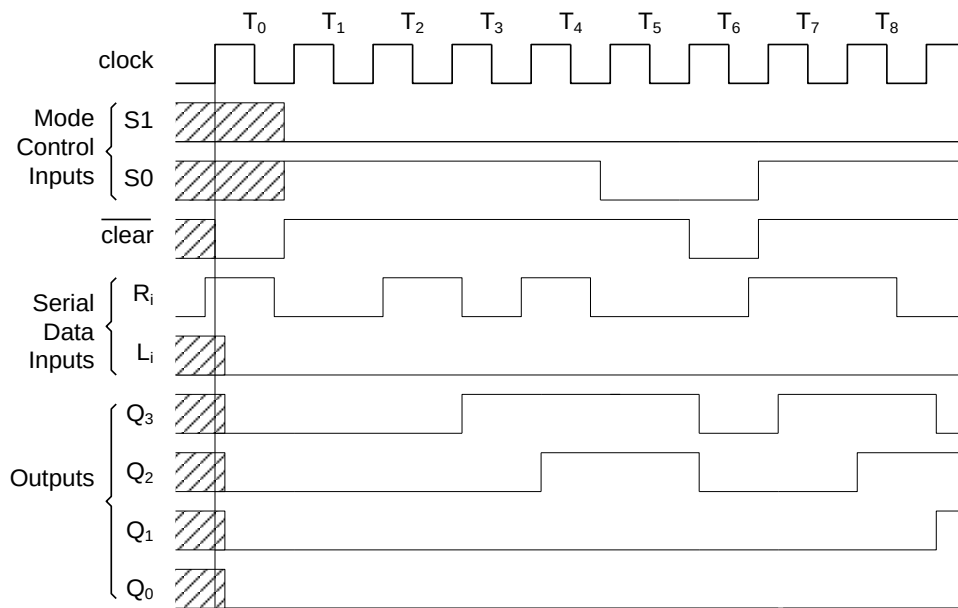


Logic Circuit Design: Tutorial 7 - Answer

Q1.



Q2.

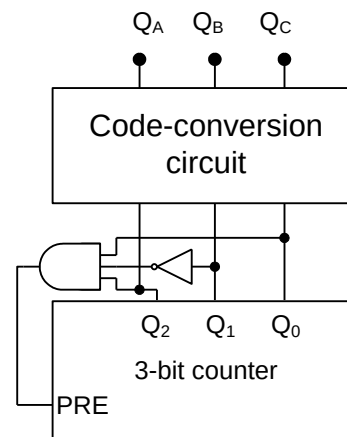
Consider the repeating sequence: 111, 000, 001, 011, 010, 110

Use the 6 counter outputs to represent 6 states.

Use the 7th state (101) to preset the counter output to 111 because of the asynchronous preset.

Code-conversion table

3-bit counter o/p (state) ($Q_2 Q_1 Q_0$)	$Q_A Q_B Q_C$
111	111
000	000
001	001
010	011
011	010
100	110
101	xxx
110	xxx

Use K-map to design circuits to generate Q_A , Q_B and Q_C from ($Q_2 Q_1 Q_0$).

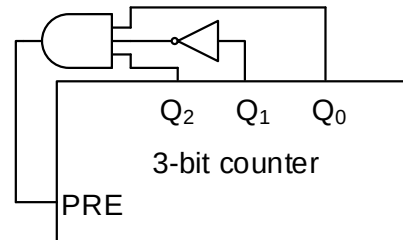
Q3.

Modulo-6 counter output: 000, 001, 010, 011, 100, 101, repeat

Use the count state “101” to preset the counter output to 000 (synchronous preset).

Code-conversion table

Present CNT	Q ₂ Q ₁ Q ₀	Next CNT	Q _A Q _B Q _C
000		001	
001		010	
010		011	
011		100	
100		101	
101		000	

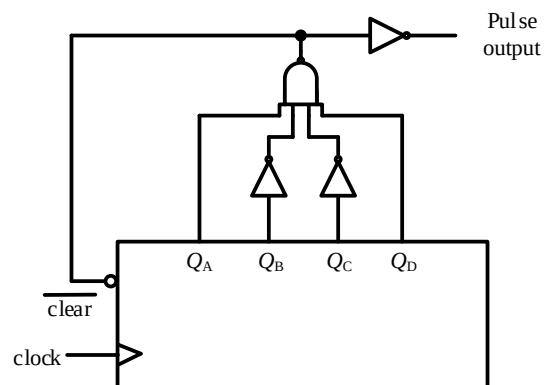
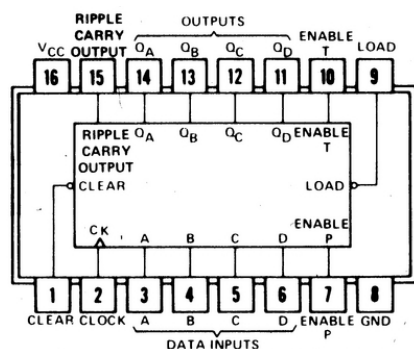


Q4. 74LS163 is a synchronous 4-bit binary counter with synchronous clear pin.

The counter starts to count from “0000” to “1001” and then reset.

The reset is to apply a “0” to the clear when count reach “1001”.

The pulse can be generated when count is “1001”.



Yes, but the circuit needs to use 1010 to generate asynchronous clear signal, and counter “0” or count “9” to generate the pulse output. Using count output other than “0” and “9” will generate a pulse and a glitch (due asynchronous clear).