

Tutorial Memory

1. Consider a machine with a byte addressable main memory of 216 bytes and block size of 8 bytes.

Assume that a direct mapped cache consisting of 32 lines is used with this machine.

- a. How is a 16-bit memory address divided into tag, line number, and byte number?
b. Into what line would bytes with each of the following addresses be stored?

0001 0001 0001 1011

1100 0011 0011 0100

1101 0000 0001 1101

1010 1010 1010 1010

- c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?
d. How many total bytes of memory can be stored in the cache?

Solution

- a. 8 leftmost bits = tag; 5 middle bits = line number; 3 rightmost bits = byte number
b. slot 3; slot 6; slot 3; slot 21
c. Bytes with addresses 0001 1010 0001 1000 through 0001 1010 0001 1111 are stored in the cache
d. 256 bytes

2. A set-associative cache has a block size of four 16-bit words and a set size of 2. The cache can accommodate a total of 4096 words. The main memory size that is cacheable is 64K 32 bits. Design the cache structure and show how the processor's addresses are interpreted.

Solution

- Block size = 4 words = 2 double words;
- associativity K = 2;
- cache size = 4048 words;
- C = 1024 block frames;
- number of sets $S = C/K = 512$;
- main memory = $64K \times 32 \text{ bits} = 256 \text{ Kbytes} = 218 \text{ bytes}$;
- address = 18 bits.

