

EE 2000 Logic Circuit Design
Semester A 2013

Tutorial 10

1. Using JK FFs and with the minimum number of states to design a counter with counting sequence: 0,4,2,1,6 and repeat. State whether the circuit is a self started circuit.
2. Design a sequential circuit with two JK FFs, A & B , and two inputs, x & E . if $E=0$, the circuit remains in the same state regardless of the value of x . When $E = 1$ and $x = 1$, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeats. When $E = 1$ and $x = 0$, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeats.
3. In many communication and networking systems, the signal transmitted on the communication line uses a non-return-to-zero (NRZ) format. Universal Serial Bus (USB) uses a specific version referred to as non-return-to-zero inverted (NRZI). A circuit that converts any message sequence of 0s and 1s to a sequence in the NRZI format is to be designed. The mapping for such a circuit is as follows:
 - (i) If the message bit is a 0, then the NRZI format message immediately flips its NRZI value
 - (ii) If the message bit is a 1, then the NRZI format message remains fixed at current NRZI value

This transformation is illustrated by the following example, which assumes that the initial value of the NRZI value is 1.

Message: 10001110011010

NRZI Message: 10100001000110

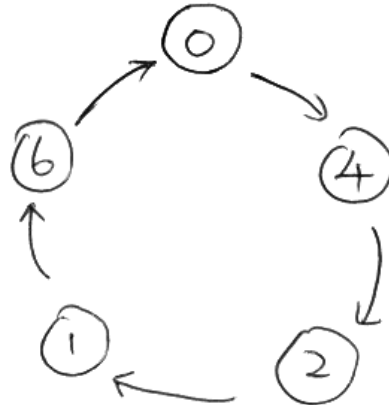
- (a) Derive the state table for the circuit and make a state assignment.
- (b) Draw the Mealy model state diagram for the circuit.
- (c) Implement the circuit using D flip-flops and logic gates.

Solution:

1. All the unused states are treated as don't care condition.

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

JK Excitation Table.



P.S.			N.S.			FFA		FFB		FFC	
A	B	C	A	B	C	JA	KA	JB	KB	JC	KC
0	0	0	1	0	0	1	X	0	X	0	X
0	0	1	1	1	0	1	X	1	X	X	1
0	1	0	0	0	1	0	X	X	1	1	X
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	0	1	0	X	1	1	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	X	X	X	X	X	X	X	X	X

A B C	JA	KA	JB	KB	JC	KC
000	1	X	0	X	0	X
100	X	1	1	X	0	X
010	0	X	X	1	1	X
001	1	X	1	X	X	1
110	X	1	X	1	0	X

$$d(A,B,C) = \Sigma(3,5,7)$$

$JA = B'$ $JB = A + C$ $JC = A'B$
 $KA = KB = KC = 1$ by inspection
 $011 \rightarrow 000$ $101 \rightarrow 010$ $111 \rightarrow 000$
 (self-starting)

P.S.			B'	1	A+C	1	A'C	1	NS		
A	B	C	JA	KA	JB	KB	JC	KC	A	B	C
0	1	1	0	1	1	1	1	10	0	0	0
1	0	1	1	1	1	1	0	1	0	1	0
1	1	1	0	1	1	1	0	1	0	0	0

Q2.

Binary up-down counter with enable E.

P.S		N.S		FF/Imps			
AB	E	A	B	JA	KA	JB	KB
00	00	00	00	0	X	0	X
00	01	00	00	0	X	0	X
00	10	11	11	1	X	1	X
00	11	01	01	0	X	1	X
01	00	01	01	0	X	X	0
01	01	01	01	0	X	X	0
01	10	00	00	0	X	X	1
01	11	10	10	1	X	X	1
10	00	10	10	X	0	0	X
10	01	10	10	X	0	0	X
10	10	01	01	X	1	1	X
10	11	11	11	X	0	1	X
11	00	11	11	X	0	X	0
11	01	11	11	X	0	X	0
11	10	10	10	X	0	X	1
11	11	00	00	X	1	X	1

JA = $(Bx + B'x')E$

JB = E

KA = $(Bx + B'x')E$

KB = E

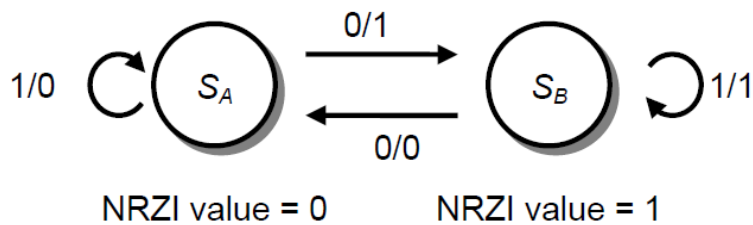
Q3.

(a)

The state table:

PS	Input Message Bit	NS	Output
Q_A	X	$Q_{A(next)}$	NRZI
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1

(b)



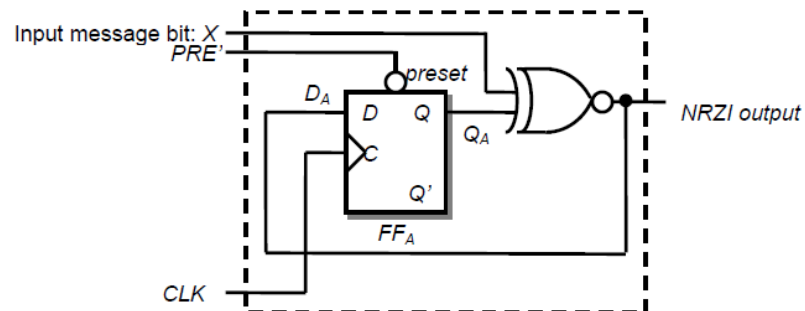
(c)

flip-flop Excitation Table:

$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

PS	Input Message Bit	NS	FF input	Output
Q_A	X	$Q_{A(next)}$	D_A	$NRZI$
0	0	1	1	1
0	1	0	0	0
1	0	0	0	0
1	1	1	1	1

From the truth table, $D_A = NRZI = Q_A \otimes X$. (i.e. Q_A exclusive-NOR X)



Note: Give a low signal to PRE' to preset the output to 1 initially