

EE4218 Computer Architecture
Sem A 2019-20
Assignment I

- (a) Write a program to compute

$$X = (A + B \times C) / (D - E \times F)$$

There is a working register, $W \leftarrow$. All the arithmetic instruction has to be conducted through the working register, The instructions available for use are as follows:

MOV	M	% ($W \leftarrow M$), The data is at memory location M
MOVW	M	% ($M \leftarrow W$)
ADD	M	% ($W \leftarrow W + M$)
SUB	M	% ($W \leftarrow W - M$)
MUL	M	% ($W \leftarrow W \times M$)
DIV	M	% ($W \leftarrow W / M$)

- (b) For each of the 6 instructions, show the addressing modes of source operand and destination operand, and the number of memory references.
- (c) A microprocessor has a pipeline with 5 stages:
- fetch instruction (FI),
 - decode instruction (DI),
 - fetch **ONE** source operand from memory (FO),
 - execute instruction (EI), and
 - write **ONE** destination operand to memory (WO).

Instructions are issued at a rate of one per clock cycle. Assume that each pipeline stage takes one clock cycle. FI, FO and WO cannot occur simultaneously.

Draw the timing diagram showing the pipeline operation in running the program in part (a).

2. Design a set-associative cache for a set size of 4 to accommodate a total of 2048 words and line size of 4. The main memory size is 64K 32 bits. Show the cache structure and how the processor's addresses are interpreted.

3. The following table shows the execution times, in seconds, for three different benchmark programs on three machines.

Benchmark	Processor		
	X	Y	Z
1	38	51	122
2	5805	4218	3309
3	407	386	233

Compute the overall SPEC rating for each system using Y as the reference machine.

4. A nonpipelined processor has a clock rate of 2.5 GHz and an average CPI (cycles per instruction) of 4. An upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays, such as latch delay, the clock rate of the new processor must be reduced to 2 GHz.
- a. What is the speedup achieved for a typical program?
- b. What is the MIPS rate for each processor?