

EE2000 Logic Circuit Design

Logic Gate Characteristics

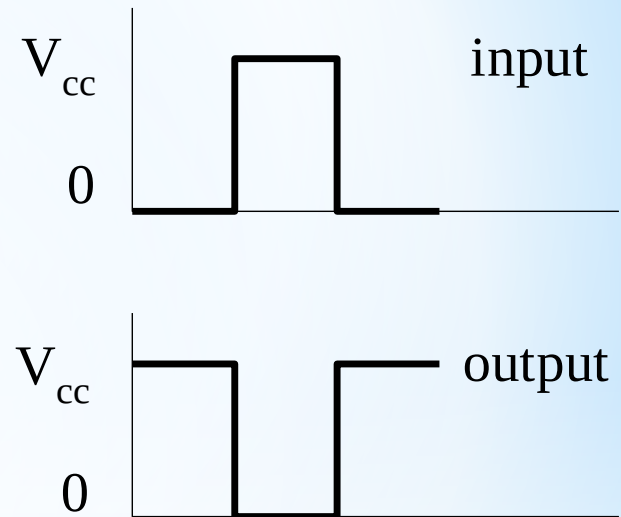
Outline

Electrical Characteristics of Logic Gates

- Ideal and practical electrical characteristics
- Logic levels, noise margins, speed of operation, power dissipation, operation temperature, fan-in, fan-out
- comparison of logic families
- logic gate interface

Ideal electrical characteristics

- I/O waveforms are ideal.
- Voltage cannot changes from 0V to V_{cc} or from V_{cc} to 0V with 0 second.
- Do NOT consider input/output current → No limit of devices connected to logic gate output.
- Input circuit sinks current or source current to the logic gate output.
- Limited source current.



Example: Inverter

Logic Gate Characteristics

For practical gates, the following features have to be considered during selection of appropriate gate type to ensure a specified performance:

- (1) Range of voltages correspond to the logic 0 and 1 levels.
- (2) Uncertainty region for these logic levels, i.e. noise margin.
- (3) Switching speed.
- (4) Static and dynamic power dissipation.
- (5) Input and output loading effects.
- (6) Operating temperature.
- (7) Supply voltage limits.

Logic Levels

Ideal logic levels Logic 0: 0 V Logic 1: V_{CC}

For practical logic gates, the input and output voltages for logic 0 and 1 are denoted as:

V_{OH} is the minimum high output voltage

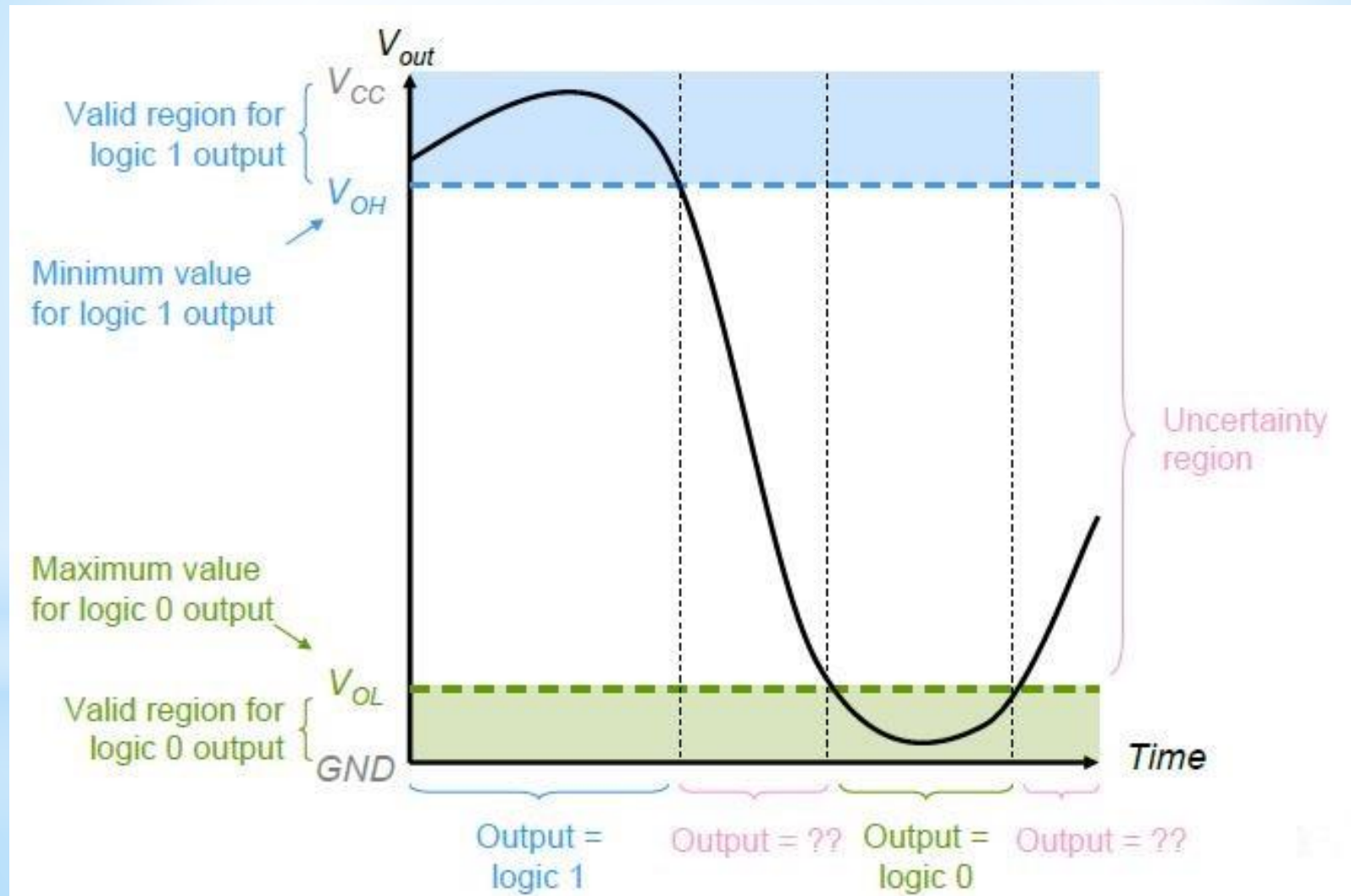
V_{IH} is the minimum high input voltage

V_{OL} is the maximum low output voltage

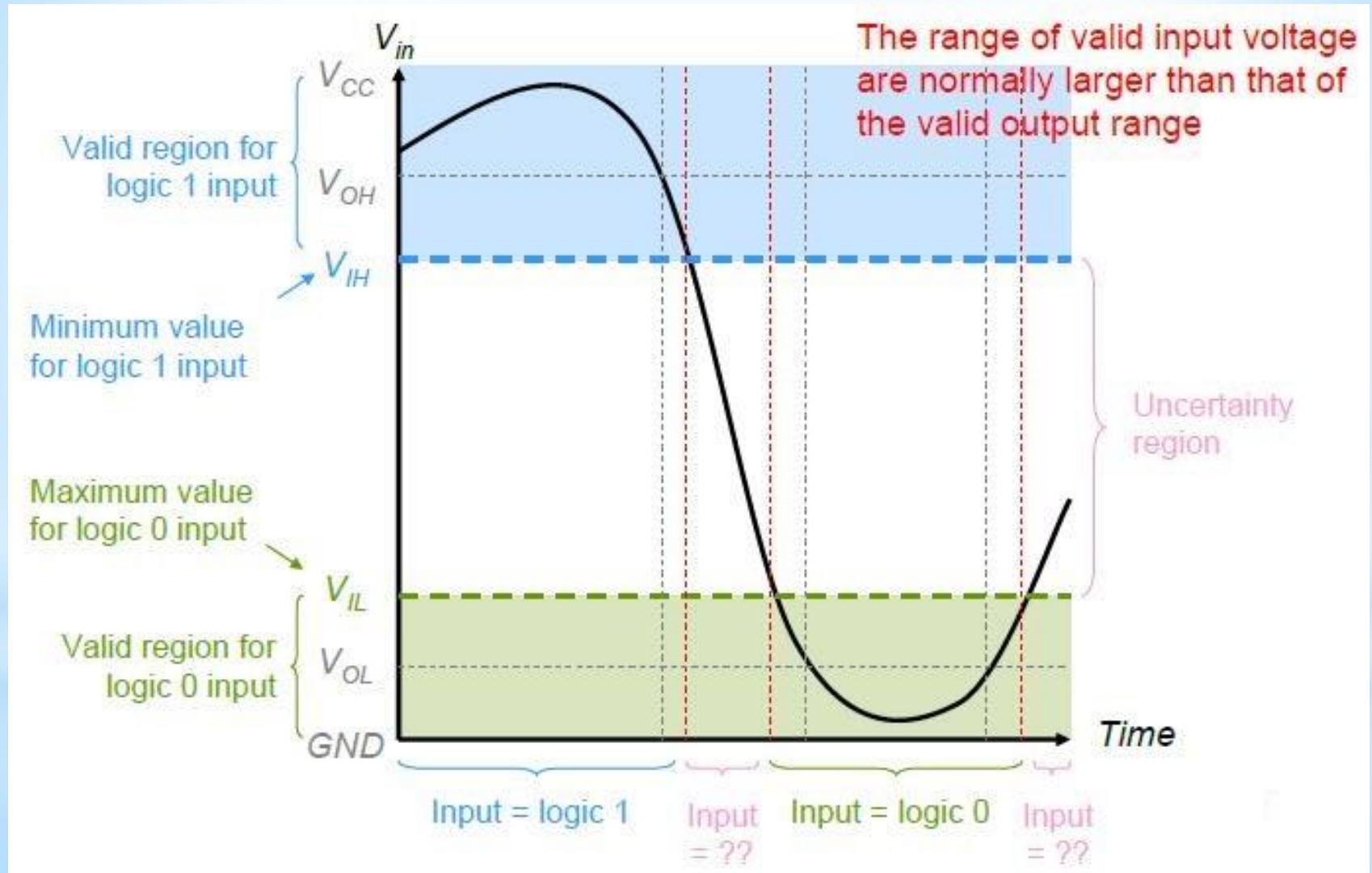
V_{IL} is the maximum low input voltage

Region between V_{IL} and V_{IH} is called uncertainty region because input level within this region will not provide a clear output level, i.e. can either be HIGH (logic 1) or LOW (logic 0).

Output Logic Levels: V_{OH} , V_{OL}



Parallel Registers



Noise Margin

Noise is **unwanted signal** present in the electric circuit

Noise margin is a measure of the immunity towards unwanted signal.

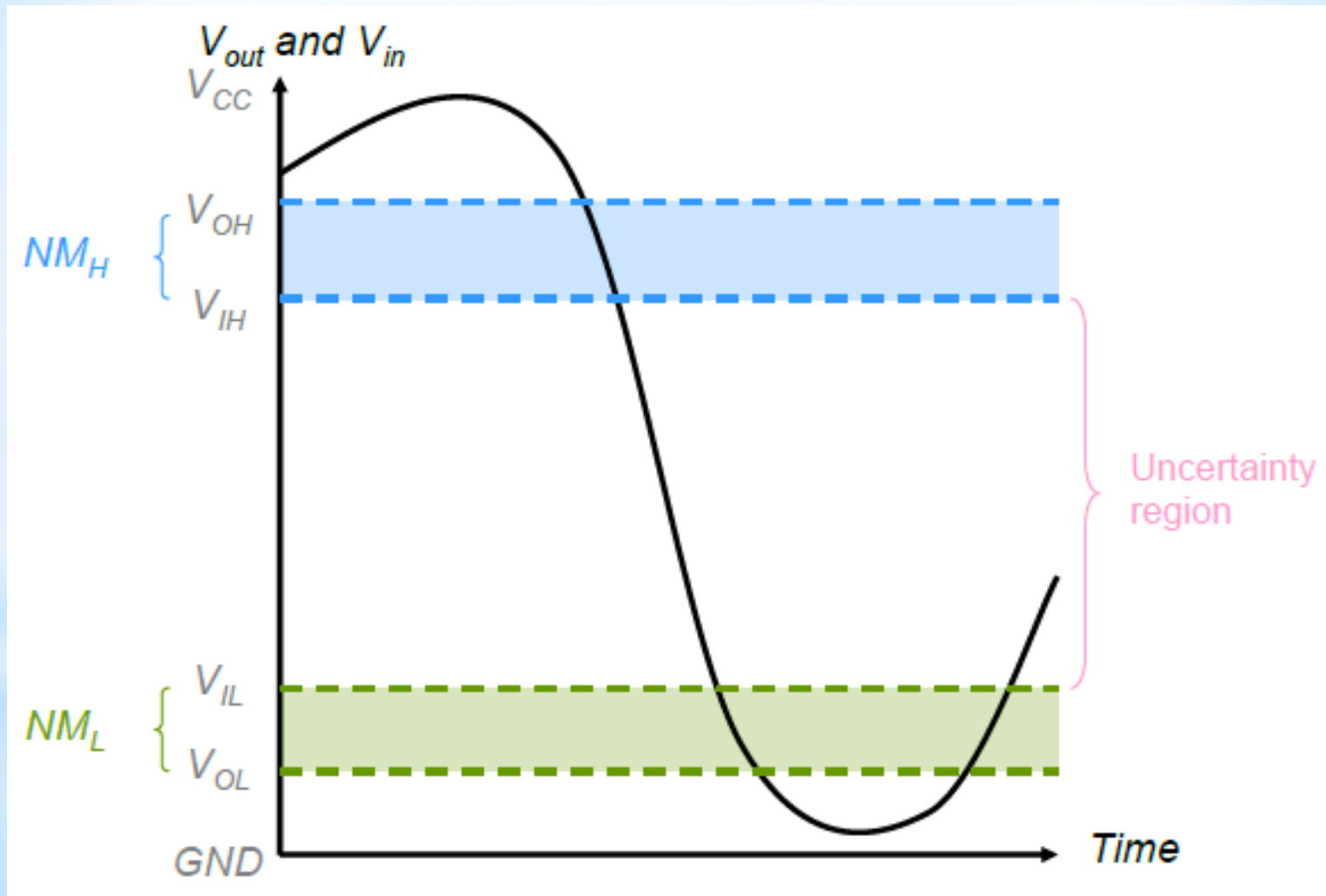
Ideally, unwanted signal of noise should not alter the logic states.

If the noise level exceeds the noise margin in the **uncertainty region**, it can trigger the transition - wrong state.

$$NM_H = V_{OH} - V_{IH} \quad (\text{Noise margin for logic 1})$$

$$NM_L = V_{IL} - V_{OL} \quad (\text{Noise margin for logic 0})$$

Noise Margin : NM_H , NM_L



Speed of Operation

- Speed of operation is determined by:
 1. time for a signal to propagate from input to output
 2. the transition time between states.
- Transition time (defined earlier on).
- Propagation delay time (defined earlier on).
- "Cycle time" t_{cyc} is the time required to make two successive cycles of transition and often it is the reciprocal of the clock frequency.
- "Delay power product" is used to measure the gate performance and is the product of the propagation delay and the power dissipation.

Speed of Operation

Speed of operation is determined by

1. Time for a signal to propagate from input to output -denoted by t_{PHL} and t_{PLH} (see Chapter 6)
2. The transition time between states - denoted by t_{tHL} and t_{tLH} (see Chapter 6)

Cycle time

- Denoted by t_{cyc}
- The time required to make two successive cycles of transition
- Often the reciprocal of the clock frequency

Delay power product

- The product of the **propagation delay** and the **power dissipation**
- Used to measure the gate performance

Power Dissipation

- Due to the true logic states in a practical gate is not 0 and V_{CC} , the difference in these levels contribute to the static or D.C. power dissipation.
- Similarly, during the change of state, the transition time is not instantaneously, hence, it contributes the dynamic power dissipation.
- The total static and dynamic consumption and is a measurement of the efficiency and a key factor during the design to avoid overheating.

Operating Temperature

- Most commercial logic gates operate between 0° and 70° C.
- For some special gates, temperature range can be extended to operate between -40° and 100° C, (e.g. **military products**).
- Most data supply by manufacturer are produced at room temperature, i.e. 25° C.

Fan-in and Fan-out

Fan in:

- The number of inputs that a gate can accept without affecting its normal performance.
- The fan in is constrained by the number of inputs provided by the gate.

Fan out:

- The number of gates that a gate can drive without degrading its performance.
- The fan out is directly related to the input and output resistance of the gates.
- Different logic gate types will provide different fan out values.

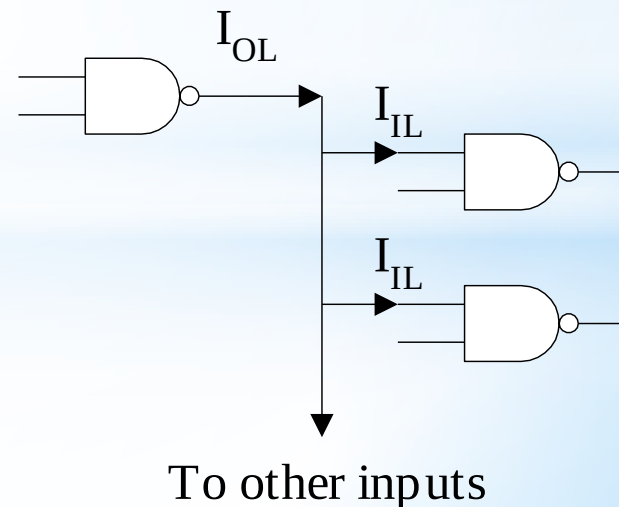
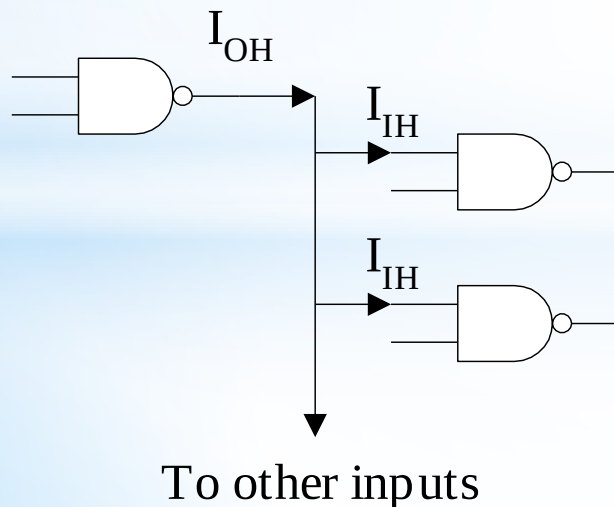
Fan-in and Fan-out

For TTL ALS gates, $I_{OH}=400\mu A$, $I_{IH}=20\mu A$, $I_{OL}=8mA$, $I_{IL}=100\mu A$.

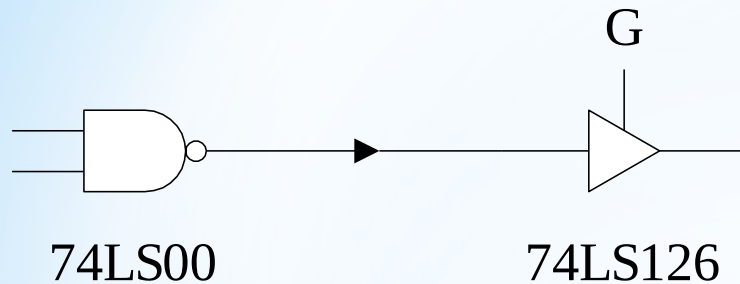
Fan-out for high output: fan out_{high} = $I_{OH}/I_{IH} = 400/20 = 20$

Fan-out for low output: fan out_{low} = $I_{OL}/I_{IL} = 8m/100\mu = 80$

fan-out of the gate = minimum(fan out_{high} , fan out_{low}) = 20



How to improve Fan-out



	74LS00	74LS126
$I_{OH(max)}$	-0.4 mA	-2.6 mA
$I_{IH(max)}$	20 μ A	20 μ A
$I_{OL(max)}$	8 mA	24 mA
$I_{IL(max)}$	-0.4 mA	-0.4 mA

Use buffer (74LS126)

fan-out of 74LS00 to 74LS00:

$$= \min(I_{OH}/I_{IH} = 0.4\text{m}/20\mu, I_{OL}/I_{IL} = 8/0.4) = 20$$

fan-out of 74LS126 to 74LS00:

$$= \min(I_{OH}/I_{IH} = 2.6\text{m}/20\mu, I_{OL}/I_{IL} = 24/0.4) = 60$$

Buffer/driver are having greater output current and/or voltage capability than ordinary logic gates.

Comparison of logic families

Most commonly used logic families are: TTL and CMOS.

Generally speaking,

1. TTL has the smallest delay power product.
2. CMOS has the lowest power dissipation and is used for LOW power consumption circuits, such as calculator and digital watches.

Comparison of logic families

Supply voltage

Logic	Subfamily	Voltages (Volts)	
		Range	Absolute maximum
TTL	all 74	4.75 - 5.25	7
TTL	all 54	4.5 - 5.5	7
CMOS	4000/4000B	3.0 - 15.0	-.5 - 7.0
CMOS	74C/HC/HCT	2.0 - 6.0	-.5 -7.0

Comparison of logic families

Propagation delay

Logic	Subfamily	Typical (ns)		Worst case (ns)	
		LH	HL	LH	HL
TTL	74	12	7	22	15
TTL	74L	35	31	60	60
TTL	74H	5.9	6.2	10	10
TTL	74S	4	5	7	8
TTL	74LS	8	8	15	15
TTL	74AS	1	1	4	4
TTL	74ALS	3	2	11	8
CMOS	4000B	75	75	150	150
CMOS	74HC	10	10	18	18
ECL	10K/100K	0.2	0.2	0.6	0.6

Testing conditions: $V_{cc} = 5V$, $C_L = 50 \text{ pF}$, $R_L = 500\Omega$

Comparison of logic families

Power dissipation

Logic	Subfamily		Power dissipation (1 NAND)	
			Typical	Worst case
TTL	74		10 mW	29 mW
TTL	74L		1 mW	3 mW
TTL	74H		21 mW	50 mW
TTL	74S		19 mW	47 mW
TTL	74LS		4 mW	6 mW
TTL	74AS		16 mW	23 mW
TTL	74ALS		2 mW	4 mW
CMOS	4000B		2 μ W	Freq. Dependent
CMOS	74HC	static	1 mW	12 μ W
		active	550 μ W	Freq. Dependent
CMOS	74HCT	static	2 μ W	20 μ W
		active	1 mW	Freq. Dependent

TTL and CMOS-HCT family are operating at the same logic levels. Extra interfacing devices is NOT required.

TTL and CMOS interface:

Logic family	TTL			CMOS	
Subfamily	74	74LS	74ALS	74HC	74HCT
$I_{IH(max)}$	40 μA	20 μA	20 μA	1 μA	1 μA
$I_{IL(max)}$	1.6 mA	400 μA	100 μA	1 μA	1 μA
$I_{OH(max)}$	400 μA	400 μA	400 μA	4 mA	4 mA
$I_{OL(max)}$	16 mA	8 mA	8 mA	4 mA	4 mA
$V_{IH(min)}$	2.0	2.0	2.0	3.5	2.0
$V_{IL(max)}$	0.8	0.8	0.8	1.0	0.8
$V_{OH(min)}$	2.4	2.7	2.7	4.9	4.9
$V_{OL(max)}$	0.4	0.4	0.4	0.1	0.1

Interfacing CMOS to TTL:

Voltage levels are compatible.

From the parameters shown in the table, when CMOS output is HIGH, the fan out:

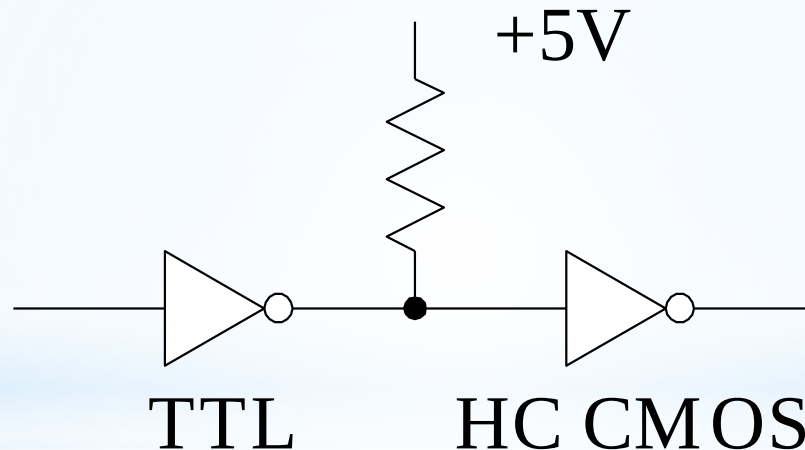
- to 74 is $4\text{m}/40\mu = 100$,
- to 74LS is $4\text{m}/20\mu = 200$,
- to 74ALS is $4\text{m}/20\mu = 200$.

When CMOS output is LOW, the fan out:

- to 74 is $4/1.6 = 2$ (very small),
- to 74LS is $4\text{m}/400\mu = 10$,
- to 74ALS is $4/400\mu = 40$.

Interfacing CMOS to TTL:

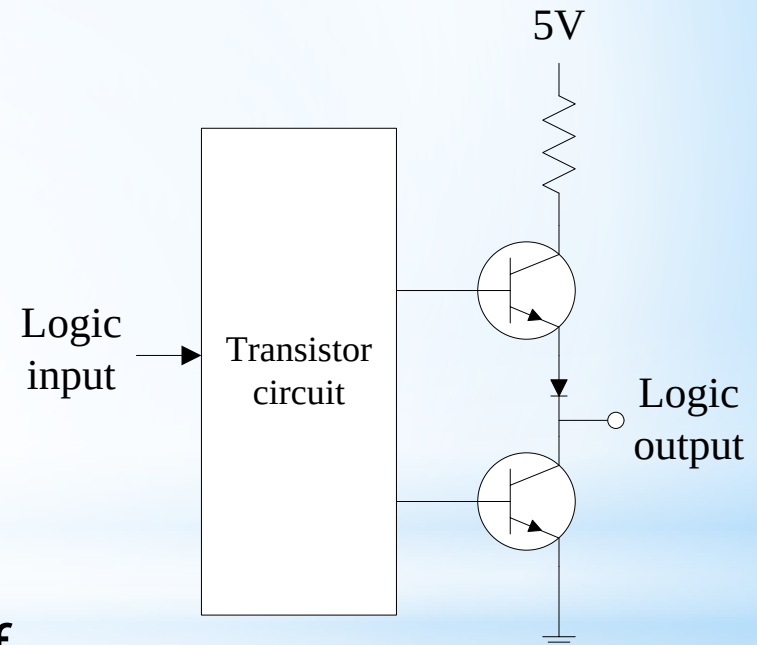
For HC CMOS logic, requires pull-up resistor from TTL to CMOS.



TTL Totem-pole output

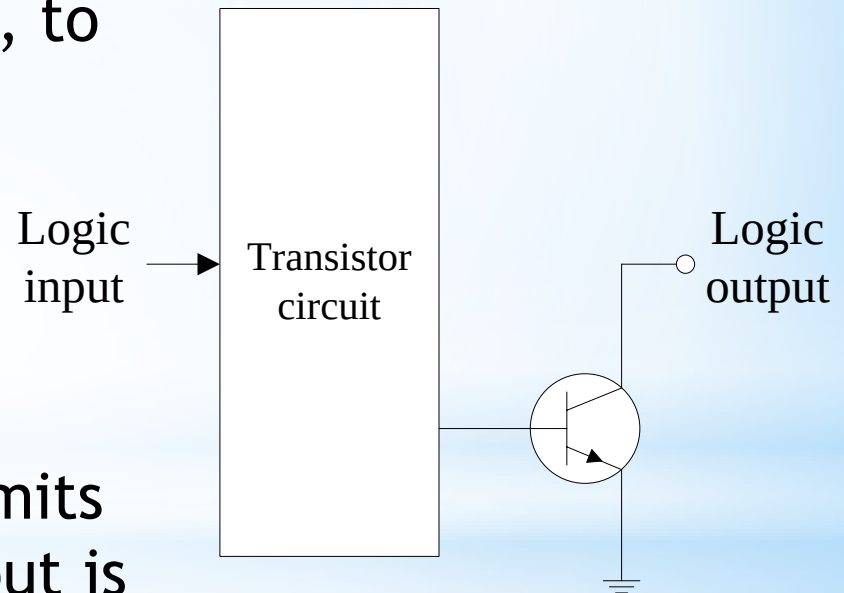
- *totem-pole* and *tristate (Hi-Z)* output:
both output circuits are identical.

- Tristate output -
disconnecting a tristate device from whatever it is connected to, even though a physical wiring connection is intact.
- This is achieved by switching off the two transistors in the output circuit.



TTL open-collector output

- *Open-collector output*: does not have a transistor connected to a V_{CC} .
- The output **must be connected** to V_{CC} through a ***pull-up resistor***, to produce logic “1” output.
- It may produce a higher V_{OH} level if a higher voltage is used.
- The ***pull-up resistor's*** value limits the sink current when the output is LOW.



TTL open-collector output

For minimum R_p :

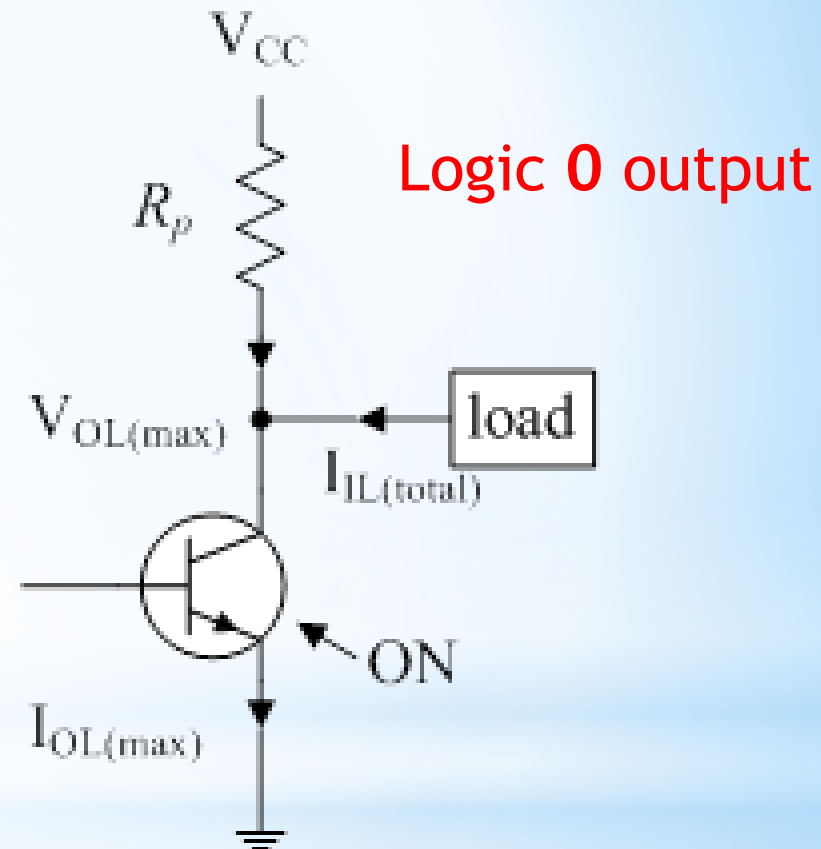
$$R_{p(\min)} = \frac{V_{CC} - V_{OL(\max)}}{I_{OL(\max)} - I_{IL(\text{total})}}$$

V_{CC} = supply voltage

$V_{OL(\max)}$ = source device max V_{OL}

$I_{OL(\max)}$ = source device max I_{OL}

$I_{IL(\text{total})}$ = total I_{IL} for all the devices connected to pull-up resistor



TTL open-collector output

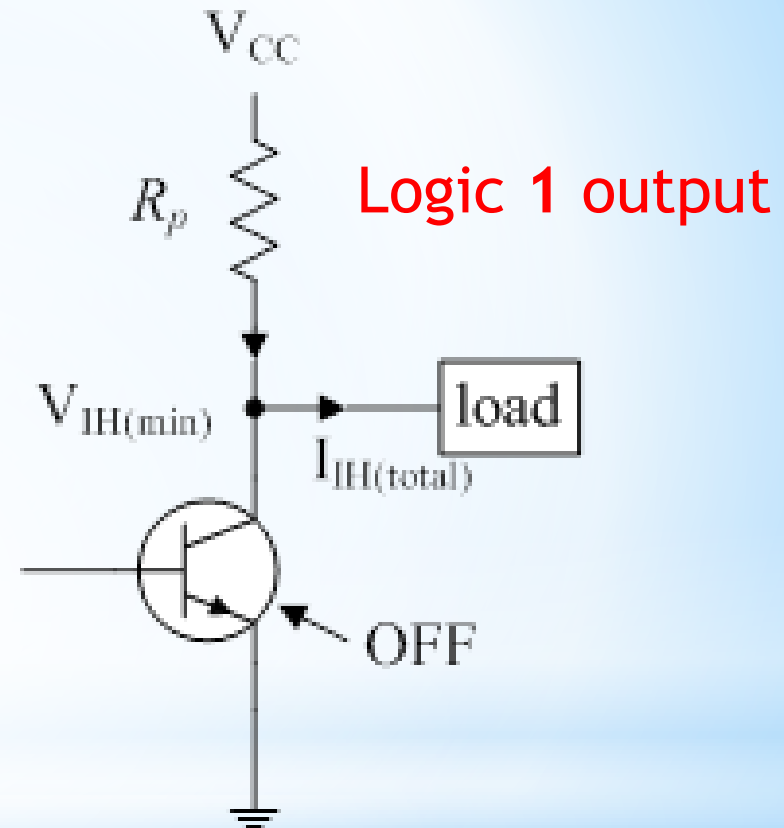
For maximum R_p :

$$R_{p(\max)} = \frac{V_{CC} - V_{IH(\min)}}{I_{IH(\text{total})}}$$

V_{CC} = supply voltage

$V_{IH(\min)}$ = load device min V_{IH}

$I_{IH(\text{total})}$ = total I_{IH} for all the devices connected to pull-up resistor



TTL open-collector output

A 74LS01 open-collector NAND gate is used to drive eight 74LS04 inverters. Determine an appropriate value for a pull-up resistor. Use $V_{CC} = 5V$.

$$V_{CC} = 5V$$

$$V_{OL(max)} = 0.4 V$$

$$I_{OL(max)} = 8 \text{ mA}$$

$$V_{IH(min)} = 2 V$$

$$I_{IL(total)} = 400 \mu A \times 8 \\ = 3.2 \text{ mA}$$

$$I_{IH(total)} = 20 \mu A \times 8 \\ = 0.16 \text{ mA}$$

$$R_{p(min)} = \frac{5 - 0.4 V}{8 - 3.2 \text{ mA}} = 958 \Omega$$

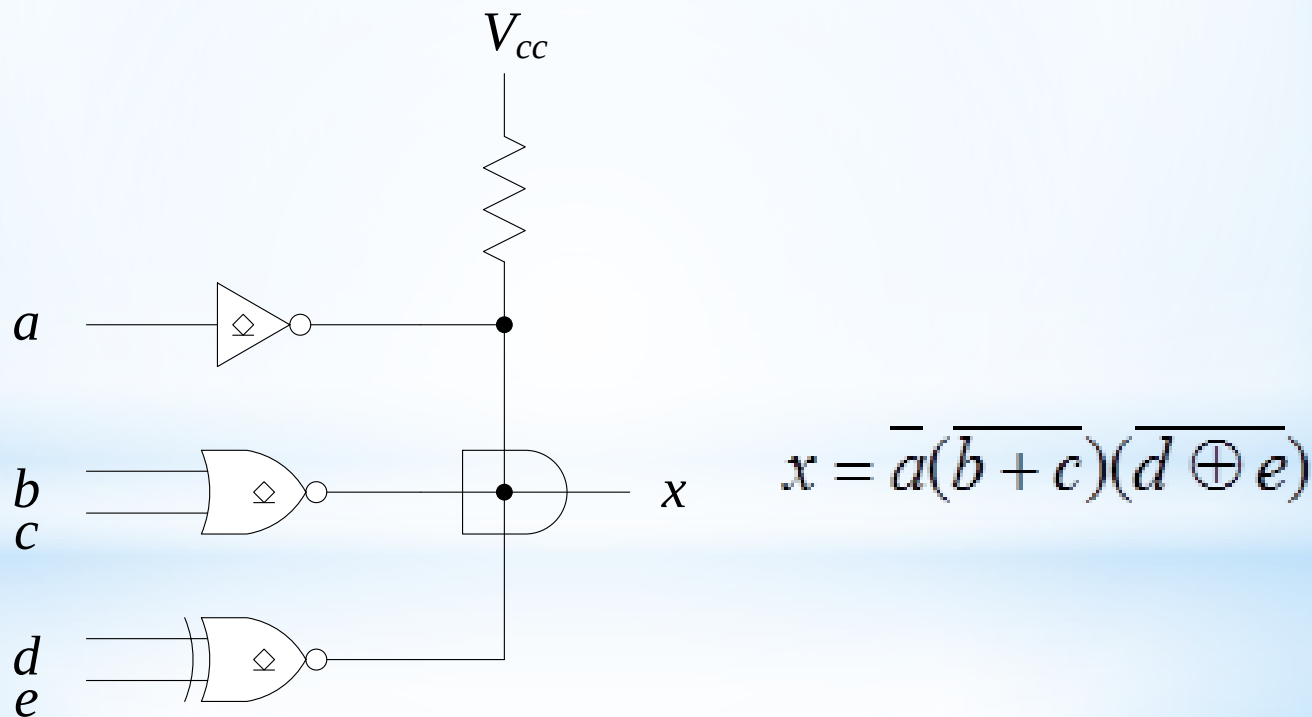
$$R_{p(max)} = \frac{5 - 2 V}{0.16 \text{ mA}} = 18.75 \text{ K}\Omega$$

In order not to reduce the switching speed of the device, a $1k\Omega$ resistor is chosen.

Note that open-collector device can be used as a buffer or driver.

Wired-AND connection

Open-collector devices with outputs connected together generate a Boolean AND operation and is known as **wired-AND** connection.



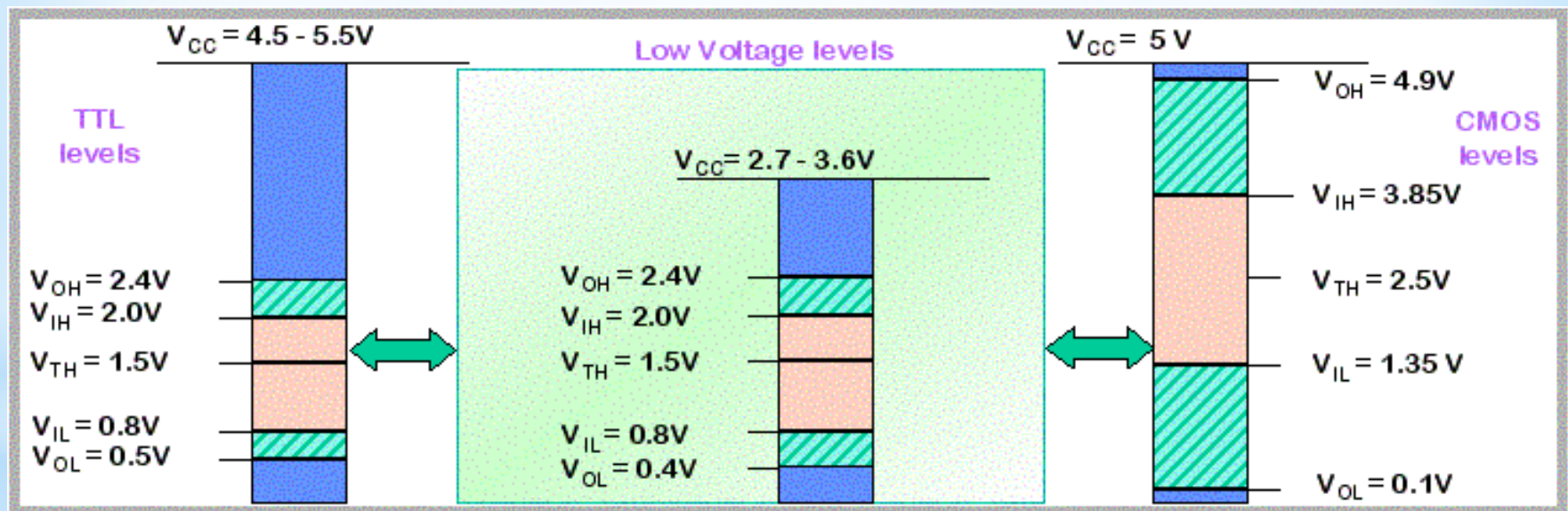
Comparison of logic families

Family	Description	Propagation delay (ns)	Toggle speed (MHz)	Power per gate @1 MHz (mW)	Typical supply voltage V (range)	Introduction year	Remarks
RTL	Resistor–transistor logic	500	4	10	3.3	1963	the first CPU built from integrated circuits (the Apollo Guidance Computer) used RTL.
DTL	Diode–transistor logic	25		10	5	1962	Introduced by Signetics, Fairchild 930 line became industry standard in 1964
CMOS	AC/ACT	3	125	0.5	3.3 or 5 (2-6 or 4.5-5.5)	1985	ACT has TTL Compatible levels
CMOS	HC/HCT	9	50	0.5	5 (2-6 or 4.5-5.5)	1982	HCT has TTL compatible levels
CMOS	4000B/74C	30	5	1.2	10V (3-18)	1970	Approximately half speed and power at 5 volts
TTL	Original series	10	25	10	5 (4.75-5.25)	1964	Several manufacturers
TTL	L	33	3	1	5 (4.75-5.25)	1964	Low power
TTL	H	6	43	22	5 (4.75-5.25)	1964	High speed
TTL	S	3	100	19	5 (4.75-5.25)	1969	Schottky high speed
TTL	LS	10	40	2	5 (4.75-5.25)	1976	Low power Schottky high speed
TTL	ALS	4	50	1.3	5 (4.5-5.5)	1976	Advanced Low power Schottky
TTL	F	3.5	100	5.4	5 (4.75-5.25)	1979	Fast
TTL	AS	2	105	8	5 (4.5-5.5)	1980	Advanced Schottky
TTL	G	1.5	1125 (1.125 GHz)		1.65 - 3.6	2004	First GHz 7400 series logic
ECL	ECL III	1	500	60	-5.2(-5.19 - -5.21)	1968	Improved ECL
ECL	MECL I	8		31	-5.2	1962	first integrated logic circuit commercially produced
ECL	ECL 10K	2	125	25	-5.2(-5.19 - -5.21)	1971	Motorola
ECL	ECL 100K	0.75	350	40	-4.5(-4.2 - -5.2)	1981	
ECL	ECL 100KH	1	250	25	-5.2(-4.9 - -5.5)	1981	

74ALB	Advanced - Low Voltage - BiCMOS
74LV (U)	Low - Voltage (Unbuffered output) (CMOS)
74LVC (R) (U)	LV - CMOS (damping Resistor)(Unbuffered output)
74LVCH	Low - Voltage - CMOS - bus Hold
74ALVC	Advanced - Low - Voltage - CMOS
74LVT (R) (U)	LV - TTL (damping Resistor)(Unbuffered output) (BiCMOS)
74LVTZ	Low - Voltage - TTL - High Impedance power-up
74ALVC (R)	ALV - CMOS (bus Hold) (damping Resistor)
74ALVCH	Advanced - Low - Voltage - CMOS - bus Hold
74LCX	LV - CMOS (operates with 3v and 5v supplies)
74VCX	LV - CMOS (operates with 1.8v and 3.6v supplies)
74CBTLV	CBT - Low Voltage

Logic voltage level for LV TTL

Low Voltage [LV] families switch at the same voltage levels as the normal TTL glue logic families



LV TTL and 5V TTL interface

A (74LVC16245) Bidirectional 3.3V to 5V transceiver is used to switch between the two logic families.

Bus "B" is the TTL +5V side, Bus "A" is the +3.3V side.

