

EE4218 Computer Architecture
Sem A 2019-20
Tutorial 1

1. (Chapter 2) The following measurements are recorded on the two machines running a number of benchmark programs consisting of four types of instruction. Machine A has the processor clock cycle time of 0.8 nsec. The processor clock rate of Machine B is 3.0 GHz.

	Instruction Count (millions)	Cycles per Instruction
Machine A		
Arithmetic and Logic	20	1
Load and store	9	3
Branch	13	3
Others	4	4
Machine B		
Arithmetic and Logic	7	1
Load and store	6	4
Branch	8	3
Others	19	6

- Determine the effective CPI, MIPS rate, and execution time for each machine.
- Comment on the results.

2. (Chapter 3) Given the Hypothetical Machine as shown:



(a) Instruction format



(b) Integer format

Program counter (PC) = Address of instruction
Instruction register (IR) = Instruction being executed
Accumulator (AC) = Temporary storage

(c) Internal CPU registers

0001 = Load AC from memory
0010 = Store AC to memory
0101 = Add to AC from memory

(d) Partial list of opcodes

Figure 3.4 Characteristics of a Hypothetical Machine

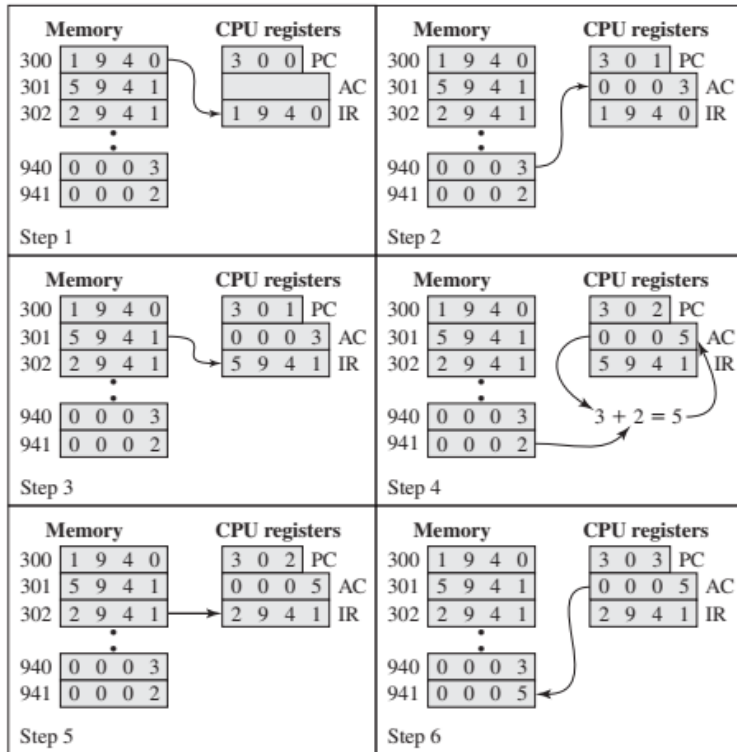


Figure 3.5 Example of Program Execution (contents of memory and registers in hexadecimal)

The hypothetical machine of Figure 3.4 also has two I/O instructions:

0011 Load AC from I/O
0111 Store AC to I/O

In these cases, the 12-bit address identifies a particular I/O device. for the following program:

1. Load AC from device 5.
2. Add contents of memory location 940.
3. Store AC to device 6

The program stored at memory location from 300 to 302, (using the format of Figure 3.5), show the content of all the CPU registers and memory contents for the execution of the program.

3. (Chapter 10) Compare zero-, one-, two-, and three-address machines by writing programs to compute

$$X = (A + B \times C) / (D - E \times F)$$

for each of the four machines. The instructions available for use are as follow:

0 Address	1 Address	2 Address	3 Address
PUSH M	LOAD M	MOVE ($X \leftarrow Y$)	MOVE ($X \leftarrow Y$)
POP M	STORE M	ADD ($X \leftarrow X + Y$)	ADD ($X \leftarrow Y + Z$)
ADD	ADD M	SUB ($X \leftarrow X - Y$)	SUB ($X \leftarrow Y - Z$)
SUB	SUB M	MUL ($X \leftarrow X \times Y$)	MUL ($X \leftarrow Y \times Z$)
MUL	MUL M	DIV ($X \leftarrow X/Y$)	DIV ($X \leftarrow Y/Z$)
DIV	DIV M		

4. (Chapter 11) Assume an instruction set that uses a fixed 16-bit instruction length. Operand specifiers are 6 bits in length. There are K two-operand instructions and L zero-operand instructions. What is the maximum number of one-operand instructions that can be supported?

5. The 16-bit Zilog Z8001 has the following general instruction format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
mode		opcode					w/b	operand 1				Operand 2			

The mode field specifies how to locate the operands from the operand fields. The w/b field is used in certain instructions to specify whether the operands are bytes or 16-bit words. The operand 1 field may (depending on the mode field contents) specify one of 16 general-purpose registers. The operand 2 field may specify any general-purpose registers except register 0. When the operand 2 field is all zeros, each of the original opcodes takes on a new meaning. How many opcodes are provided on the Z8001?