

## EE4803 Analog IC Design Quiz 2

### Instructions

1. This is a closed-book examination. But you can bring 2 A4 sheets with formula written on both sides
2. Unless specifically stated, all symbols have their usual meanings.
3. Time allowed: 1 hour.
4. Use the following parameters for MOS transistors taken from a nominal 0.8  $\mu\text{m}$  process

| Parameter<br>Symbol | Parameter Description                      | Typical Parameter Value                                  |                                                          | Units                    |
|---------------------|--------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|--------------------------|
|                     |                                            | n-Channel                                                | p-Channel                                                |                          |
| $V_{T0}$            | Threshold voltage ( $V_{BS} = 0$ )         | $0.7 \pm 0.15$                                           | $-0.7 \pm 0.15$                                          | V                        |
| $K'$                | Transconductance parameter (in saturation) | $110.0 \pm 10\%$                                         | $50.0 \pm 10\%$                                          | $\mu\text{A}/\text{V}^2$ |
| $\gamma$            | Bulk threshold parameter                   | 0.4                                                      | 0.57                                                     | $\text{V}^{1/2}$         |
| $\lambda$           | Channel length modulation parameter        | $0.04 (L = 1 \mu\text{m})$<br>$0.01 (L = 2 \mu\text{m})$ | $0.05 (L = 1 \mu\text{m})$<br>$0.01 (L = 2 \mu\text{m})$ | $\text{V}^{-1}$          |
| $2 \phi_F $         | Surface potential at strong inversion      | 0.7                                                      | 0.8                                                      | V                        |

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1. Figure 1(a) shows a Common-source amplifier with current source load and Fig. 1(b) shows an improved cascoded common-source amplifier.

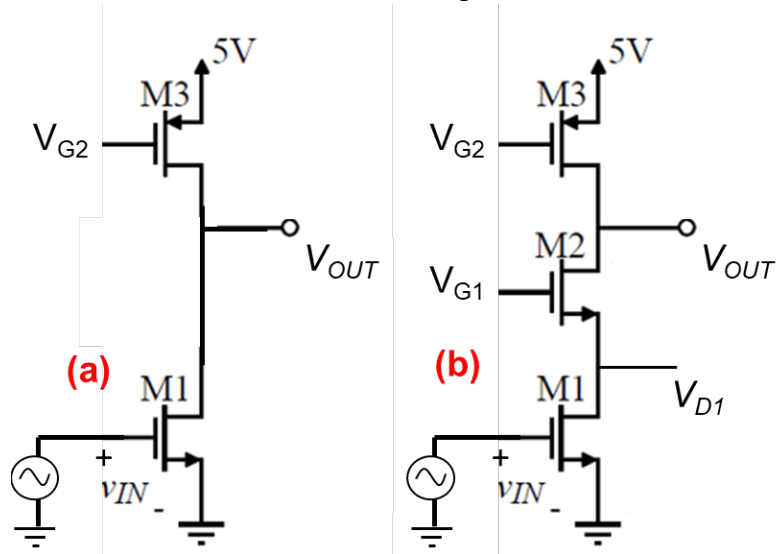


Figure 1

The size of the transistors in  $\mu\text{m}$  are given as  $(W/L)_1 = (W/L)_2 = (W/L)_3 = 4/1$ . The DC bias voltage  $V_{G2}$  is designed to create a DC bias current of  $10\ \mu\text{A}$ .

- Derive the expression of output resistance  $R_{out}$  and the AC gain ( $V_{out} / V_{in}$ ) for both the circuits in terms of  $g_m$ ,  $r_o$  of the transistors. Assume all transistors are in saturation.
  - Find the numerical value of the AC gains derived above using device parameters from the table given.
  - If the output in Fig. 1(b) is measured at  $V_{D1}$ , derive the expression of the AC gain ( $V_{D1} / V_{in}$ ).
- In Fig. 1(b), improve the design of the current source to increase the AC gain ( $V_{out} / V_{in}$ ) found in Q1 by **50 times** while keeping DC bias current of  $10\ \mu\text{A}$ . Draw the circuit, specify  $(W/L)$  values and bias voltages used.
  - Consider the circuit in Fig. 3 where CLKB is inverted waveform of CLK (CLKB = NOT(CLK)). Suppose I want to design a switch using **one transistor only** to charge a capacitor  $C = 10\ \text{pF}$  from  $0.1\ \text{V}$  to  $0.3\ \text{V}$  using a  $0.8\ \mu\text{m}$  CMOS process with power supply  $V_{dd} = 5\ \text{V}$ .
    - What type of transistor should be used – NMOS or PMOS and why?
    - For  $(W/L)=20$  for this transistor, what is the maximum clock frequency that can be applied so that the circuit can still charge to 1% of its final value within this clock period?

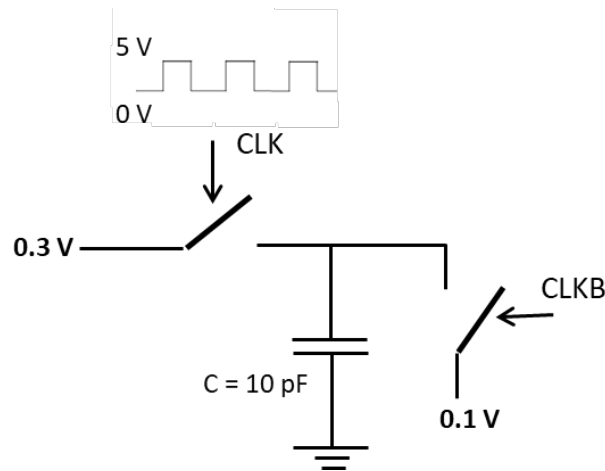


Figure 3