

EE 2000 Logic Circuit Design
Semester A 2013

Tutorial 11

- Using a synchronous binary counters as shown in Figure 1, design and draw a counter to generate the following repeating sequences 2 to 9 repeatedly for a free running clock.

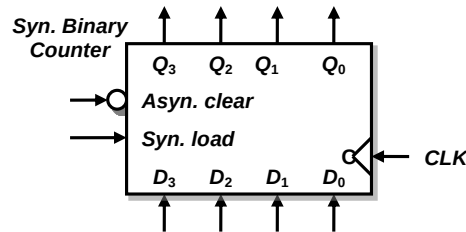


Figure 1.

- Using two 4-bit synchronous binary counters as shown in Figure 2, design a BCD counter to count from 00 to 99. Draw the circuit. *Note that the clear and load are synchronous inputs.*

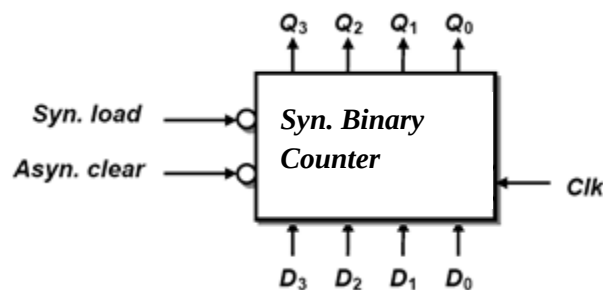


Figure 2.

- State the major advantage and disadvantage of using ECL logic family as compared with TTL and CMOS logic families.

(b) Table 1 shows the DC characteristic of a logic device when the supply voltage is equal to 5 V.

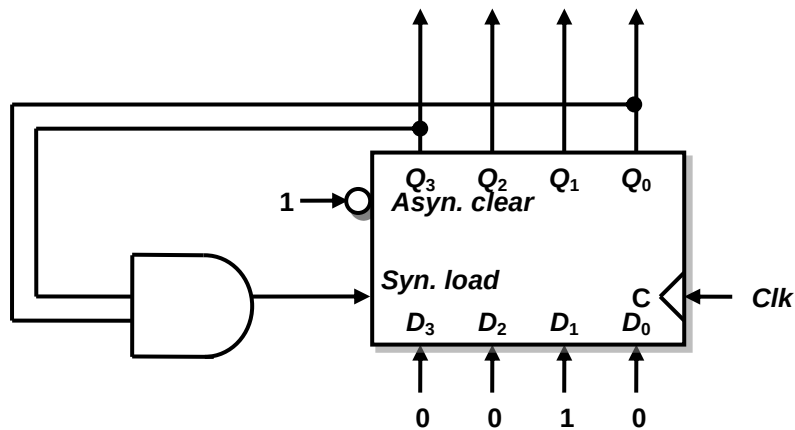
- What are the noise margins of this TTL family?
- What is the fan-out of this TTL family?

Symbol	Parameter	Value
V_{IH}	Guaranteed minimum Input High Voltage	2.0V
V_{IL}	Guaranteed maximum Input LOW Voltage	0.9V
V_{OH}	Guaranteed minimum Output High Voltage	2.4V
V_{OL}	Guaranteed maximum Output LOW Voltage	0.3V
I_{IH}	Input HIGH Current	40uA
I_{IL}	Input LOW Current	0.8mA
I_{OH}	Output HIGH Current	400uA
I_{OL}	Output LOW Current	16mA

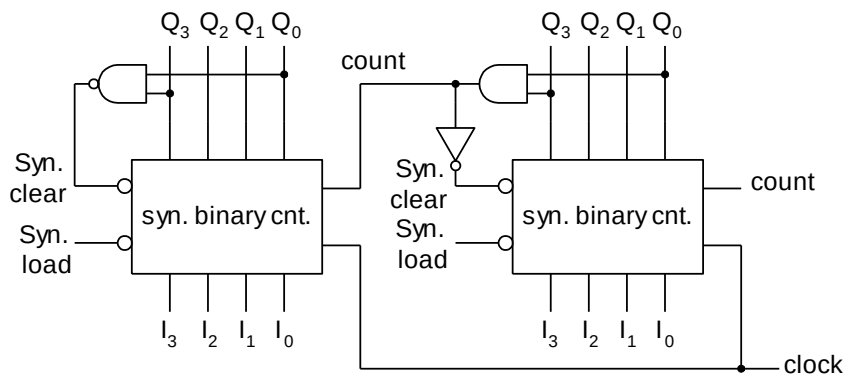
Table 1

Solution:

(1)



(2)



(3)

- (a) Advantage: highest speed
Disadvantage: high power consumption

(b)(i) $NM_H = V_{OH} - V_{IH} = 2.4V - 2.0V = 0.4V$
 $NM_L = V_{IL} - V_{OL} = 0.9V - 0.3V = 0.6V$

(b) (ii) Fan-out for high output: fan out high = $I_{OH}/I_{IH} = 400\mu A/40\mu A = 10$

Fan-out for low output: fan out low = $I_{OL}/I_{IL} = 16mA/0.8mA = 20$

fan-out of the gate = minimum (fan out high , fan out low) = 10