

Block D - Unit 2 Outline

- MOSFETs
 - > Schematic figure and Symbol
 - > Basic working principle and Operating modes
 - > Application to logic gates
- Bipolar transistors
 - > Construction
 - > Basic working principle and Operating modes
 - > Application to logic gates

Classification of FETs

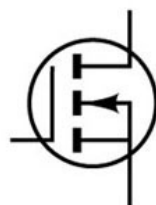
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FET: Field Effect Transistor

Enhancement MOS



p channel



n channel

Depletion MOS

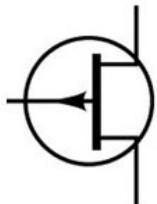


p channel

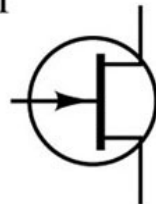


n channel

JFET



p channel



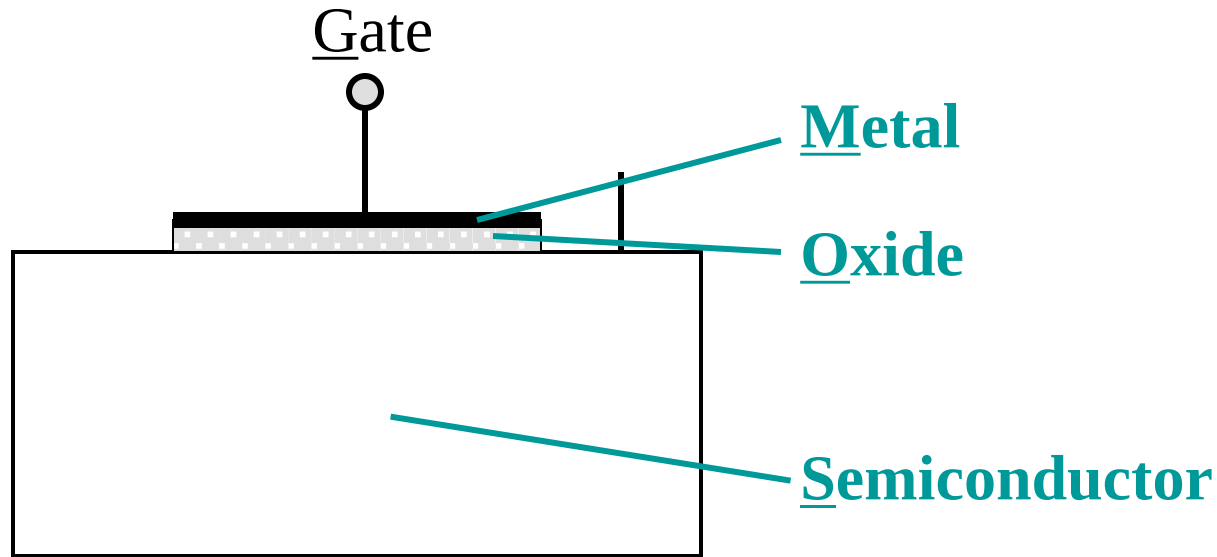
n channel

MOSFET: Metal Oxide
Semiconductor FET

**In contrast to diodes (2 terminals),
transistors are 3 terminal devices.**

JFET: Junction FET

MOS Structure



Schematic

Sandwich structure: Metal-Oxide-Semiconductor

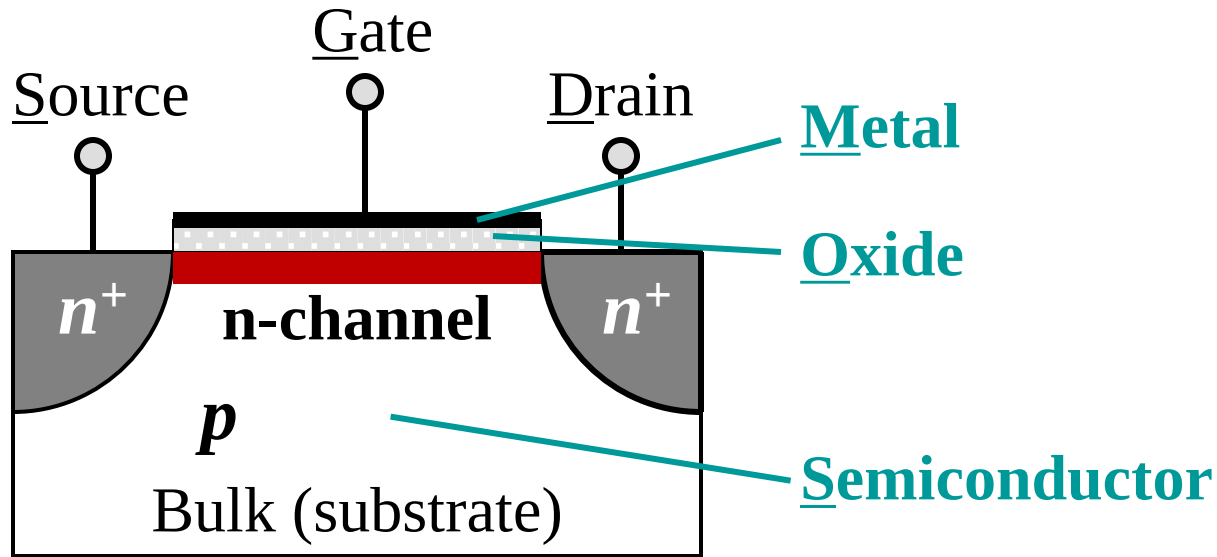
Metal (Conductor)

Oxide (Insulator)

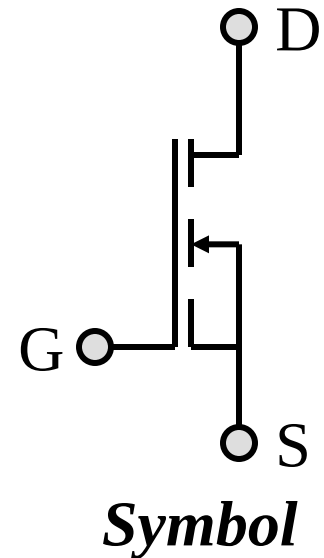
Semiconductor (Can be made to conductor or not)

Looks like a capacitor

NMOS Schematic and Symbol



Schematic



Symbol

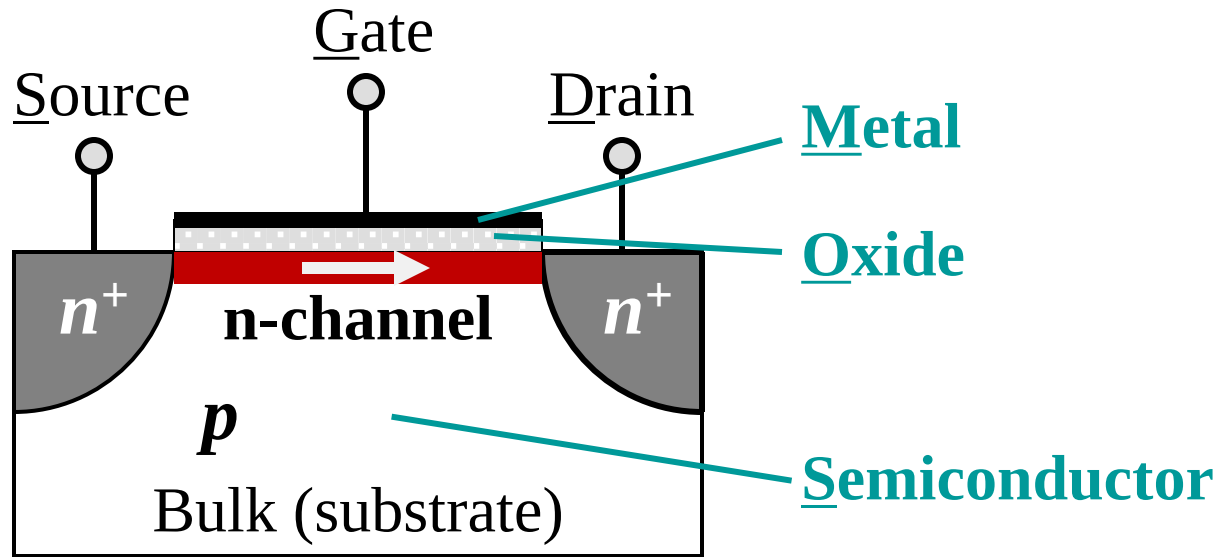
3 terminals: Gate (G), Source (S), Drain

NMOS: P-type semiconductor (bulk) that is n-doped at 2 regions to form S and D

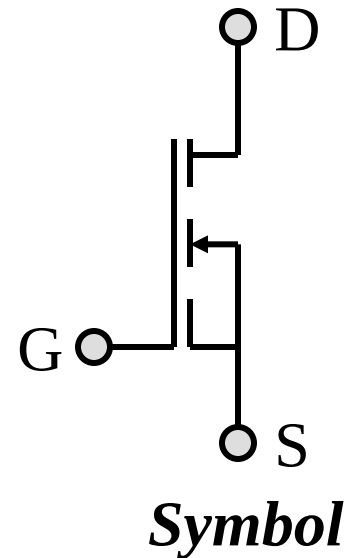
Voltage at G controls current between S and D

Key feature: CHANNEL (n-channel for NMOS) and Drain Current

NMOS Schematic and Symbol



Schematic



Carriers from S move to D through the channel

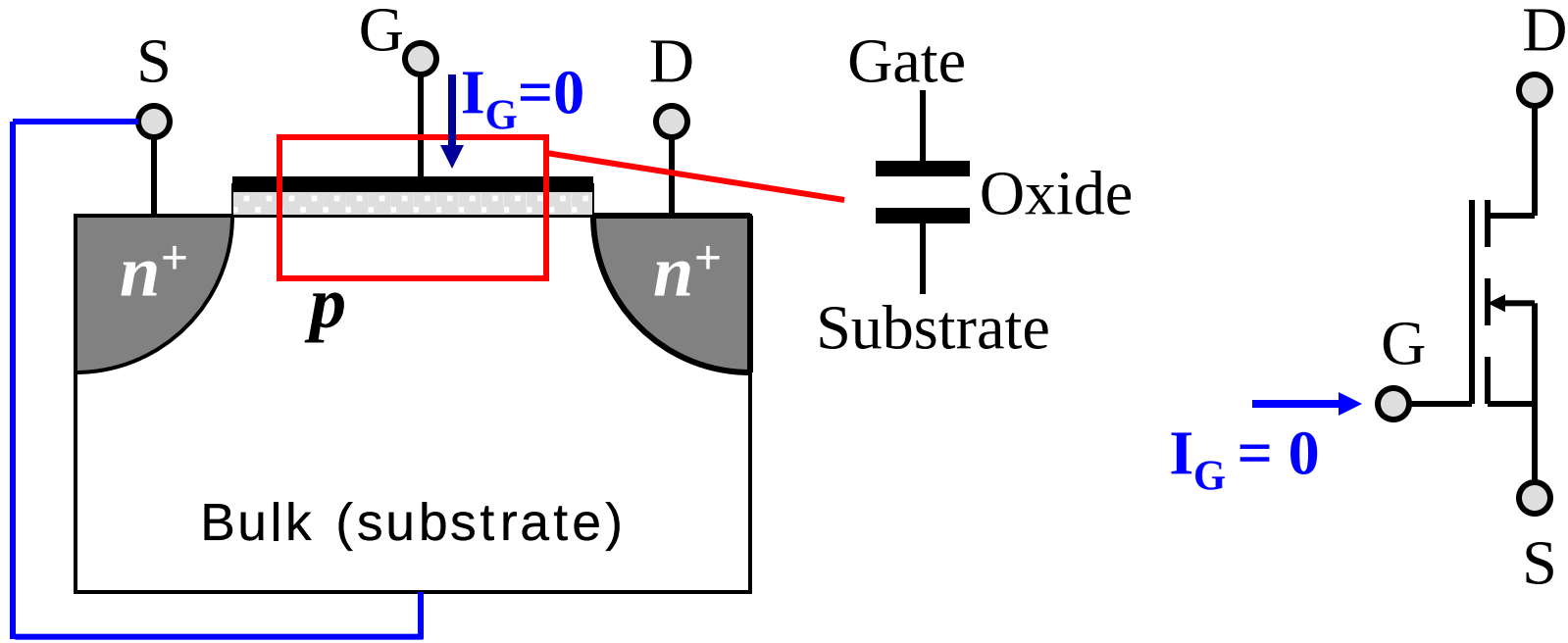
NMOS: carriers are electrons $\Rightarrow$ Current flows from _____

Voltage at G determines whether a channel forms under the gate

NO CHANNEL NO CURRENT (Device is OFF)

The only current we care is the DRAIN current (between _____)

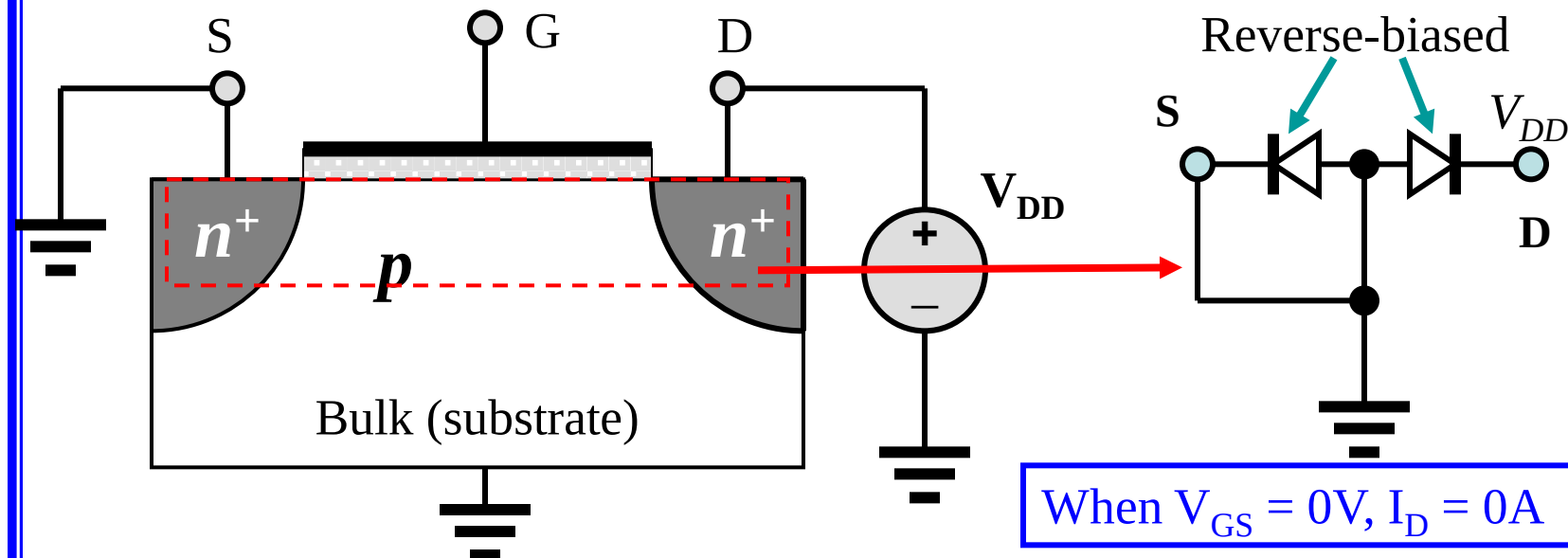
Gate Current



The gate current in a MOSFET is ideally zero:

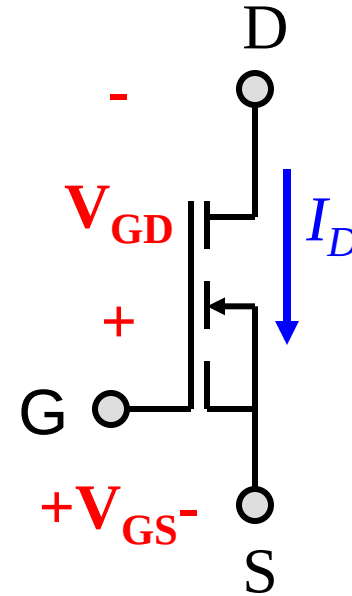
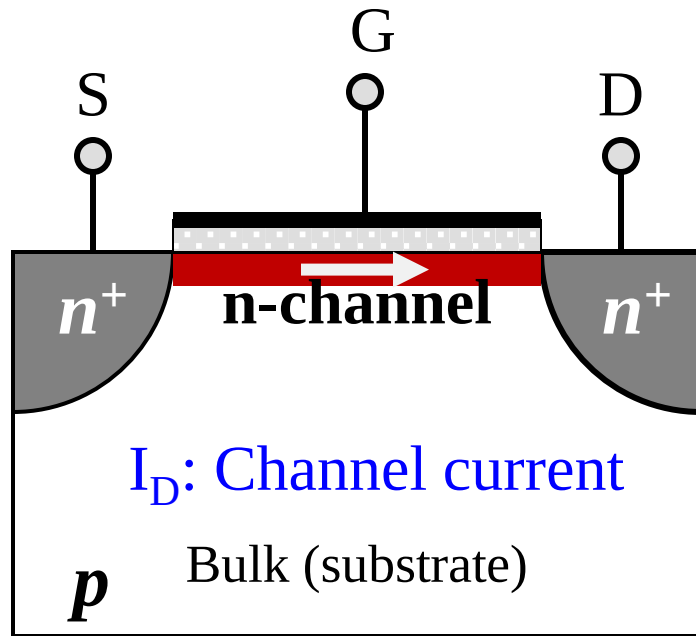
Gate current sees a capacitor formed by the gate, oxide (which is insulating), and substrate (conducting)

NMOS is normally off



- When no voltage is applied to the gate, no channel is formed under the gate
- Drain-Bulk n+p junction is strongly reverse-biased
- Source-Bulk n+p junction is also reverse-biased
- No conductive path between S and D: no current

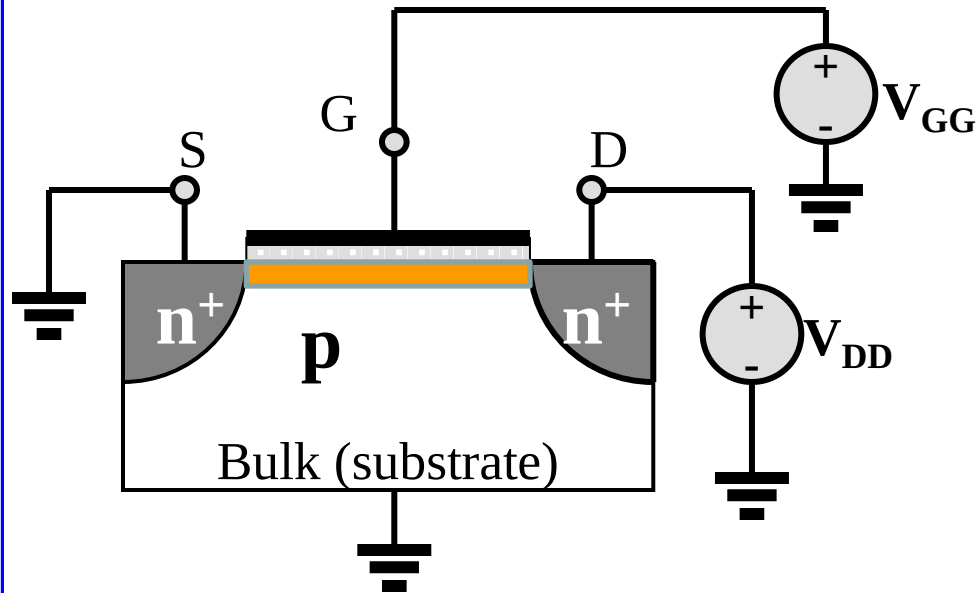
NMOS Operation



Amount of current in the channel is controlled by the voltage applied at the terminals (V_{GS} and V_{GD})

Device is “switched on” (formation of a conducting channel) by the voltage on the Gate

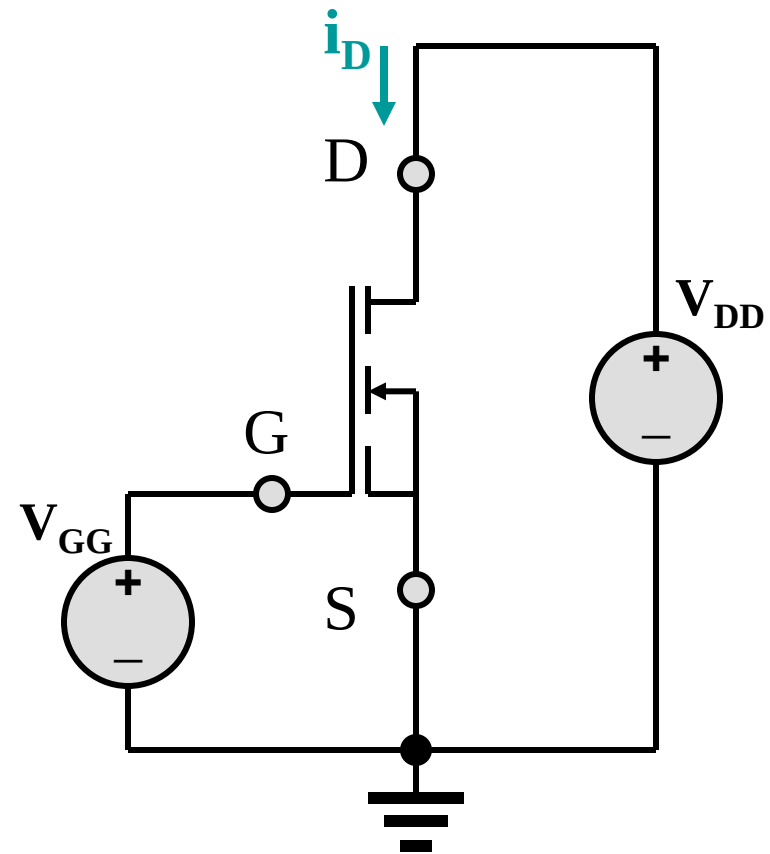
Conducting channel in NMOS



NO CHANNEL NO CURRENT

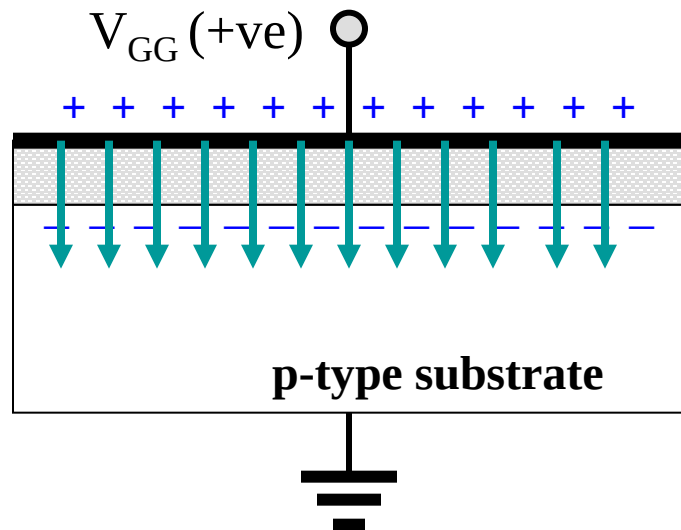
Channel forms **only** when $V_{GS} > V_T$

V_T is a parameter whose value depends on the design of the MOSFET and the material properties.



For conduction to occur, $V_{GS} > V_T$

Formation of channel in NMOS



Initially when $V_{GS} < V_T$:

- The majority carriers in p-type silicon are holes (positively charged)
- Holes are repelled away from the surface at the silicon-oxide interface
- The interface becomes depleted of majority carriers
- No conduction occurs between S and D

When $V_{GS} > V_T$:

- The minority carriers in p-type silicon are electrons (negatively charged)
- Electrons are attracted towards the surface at the silicon-oxide interface
- A narrow conducting n-type channel near this surface forms
- Electrons from the source can now flow towards the drain resulting in a drain current I_D
- Increasing V_{GS} (while keeping V_{DS} fixed) increases the concentration of carriers, thereby increasing conduction

Cutoff mode

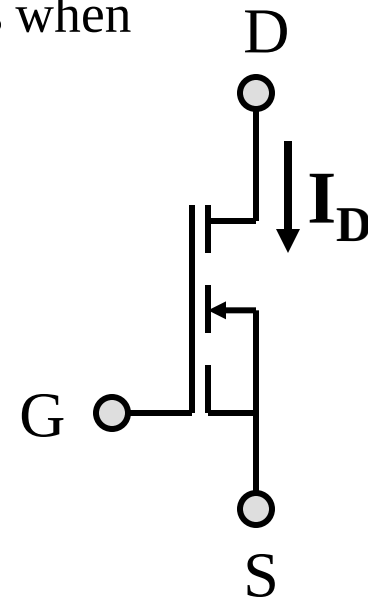
The first mode we shall consider is when the device is off. This is known as Cutoff. As previously pointed out, this occurs when the threshold voltage has not been reached.

Cutoff Region

$$V_{GS} < V_T, V_{GD} < V_T$$

As a result of this,

$$I_D = 0A$$



Cutoff Region

- V_{GS} and V_{GD} both less than V_T
- Channel is off at both source and drain
- No conduction and no current flow between S & D

Triode mode

As mentioned previously, when the gate voltage exceeds the threshold the MOS can conduct and therefore turns on. When it turns on, it can operate in one of two possible regions. One of these 2 modes is known as the triode or ohmic region.

Triode/Ohmic Region

$$V_{GS} > V_T, V_{GD} > V_T$$

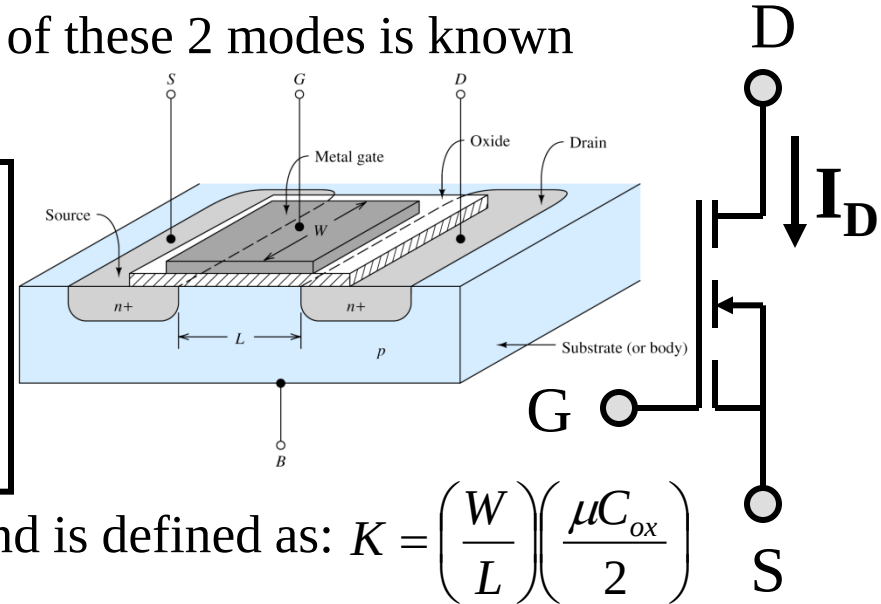
The drain current is given by:

$$I_D = K [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

K is known as the conductance parameter, and is defined as: $K = \left(\frac{W}{L}\right)\left(\frac{\mu C_{ox}}{2}\right)$

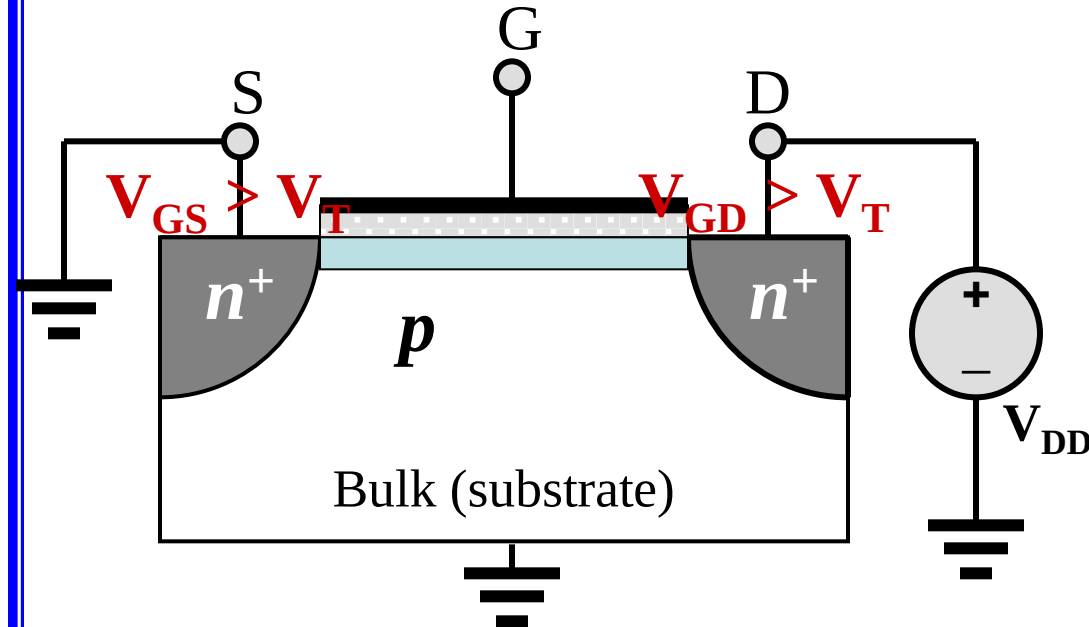
Triode/Ohmic Region

- Both V_{GS} and V_{GD} are greater than V_T
- Channel is on at source and also on at drain
- Current is dependent of both V_{DS} and V_{GS}



W: channel width
L: channel length
 μ : mobility of carriers
 C_{ox} : Oxide capacitance

MOS in Triode mode



Near both the drain and source:

⇒ Voltage difference $> V_T$

⇒ Conducting channel is formed on both sides

In fact everywhere under the gate oxide is larger than V_T so there is a continuous channel between the drain and source.

⇒ Increasing V_{GS} thus increases the number of carriers, resulting in a larger drain current

⇒ Increase V_{DS} increases the voltage drop across the channel, resulting in a larger drain current

I_D is dependent therefore on both V_{DS} and V_{GS} (Refer to equation on previous slide)

Saturation mode

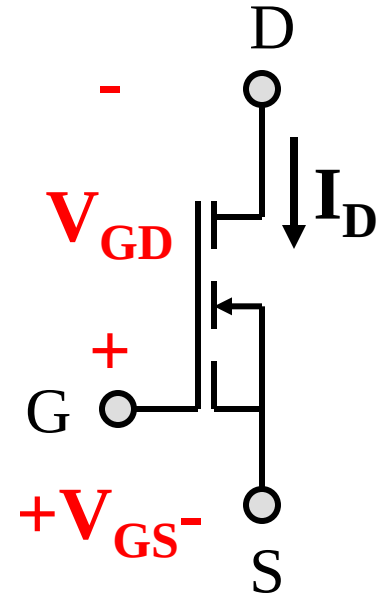
While the MOS is still on, if we continue to increase V_{DS} without increasing V_{GS} , there will come a point when the voltage near the drain becomes less than the threshold ($V_{GD} < V_T$). This is known as the saturation region.

Saturation Region

$$V_{GS} > V_T, V_{GD} < V_T$$

The drain current is given by:

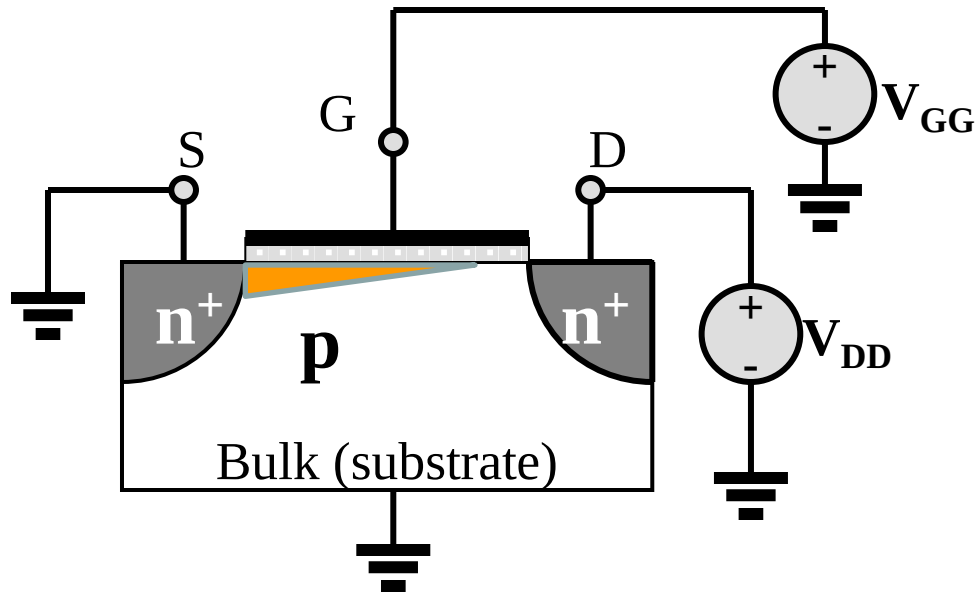
$$i_D = K (V_{GS} - V_T)^2$$



Saturation Region

- $V_{GS} > V_T$ and $V_{GD} < V_T$
- Channel is on at source but off at drain
- Current is nearly independent of V_{DS} , depending only on V_{GS}
- One might expect the MOS to operate like in cutoff under these bias conditions but it does not.

NMOS in Saturation



The channel in saturation mode is typically represented as tapered or wedged (as shown in the figure). Large currents still conduct via the channel due to the large voltage drop across drain and source, but changes little with increasing V_{DS} .

Pinch-off (going from triode to saturation)

The channel near the drain begins to fall below the threshold condition when

$$V_{GD} = V_T$$

In terms of the drain-source voltage, this corresponds to:

$$V_{DS}(\text{pinch-off}) = V_{GS} - V_T$$

Summary of operating modes

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- **Cut-Off:**

$$V_{GS} < V_T, V_{GD} < V_T$$

- **Linear/Triode/Ohmic:**

$$V_{GS} > V_T, V_{GD} > V_T$$

- **Saturation:**

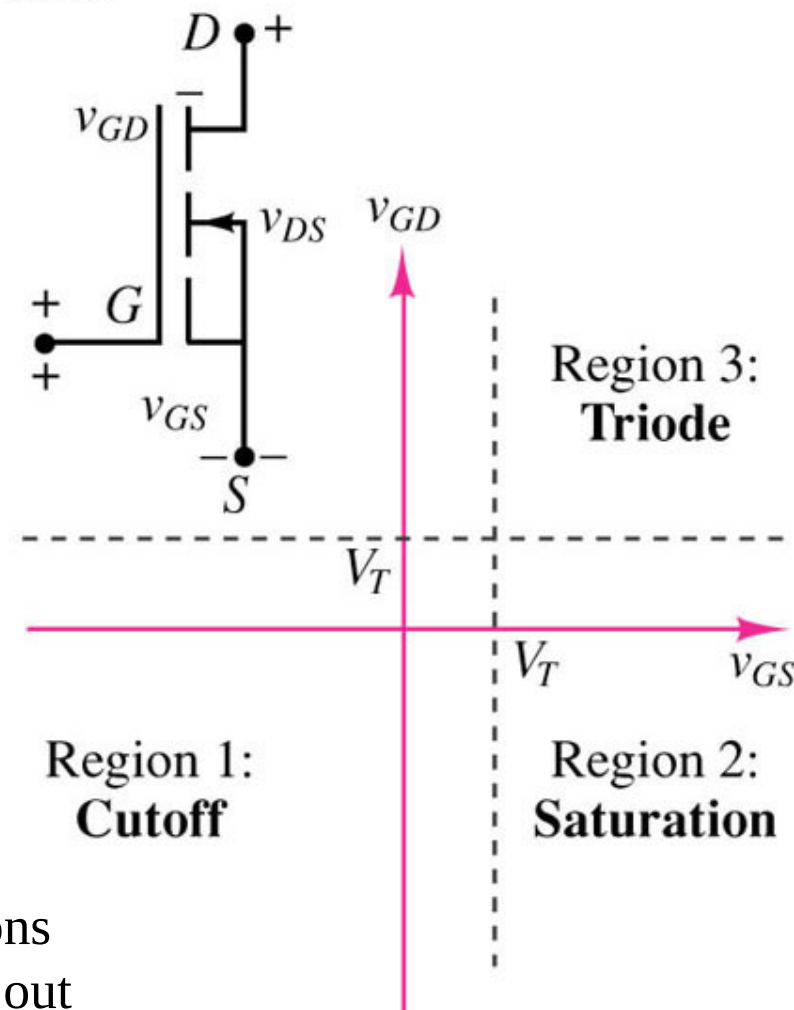
$$V_{GS} > V_T, V_{GD} < V_T$$

For n-channel
enhancement MOS

$$\text{Power} = I_D V_{DS}$$

This sets a limit on the operating conditions

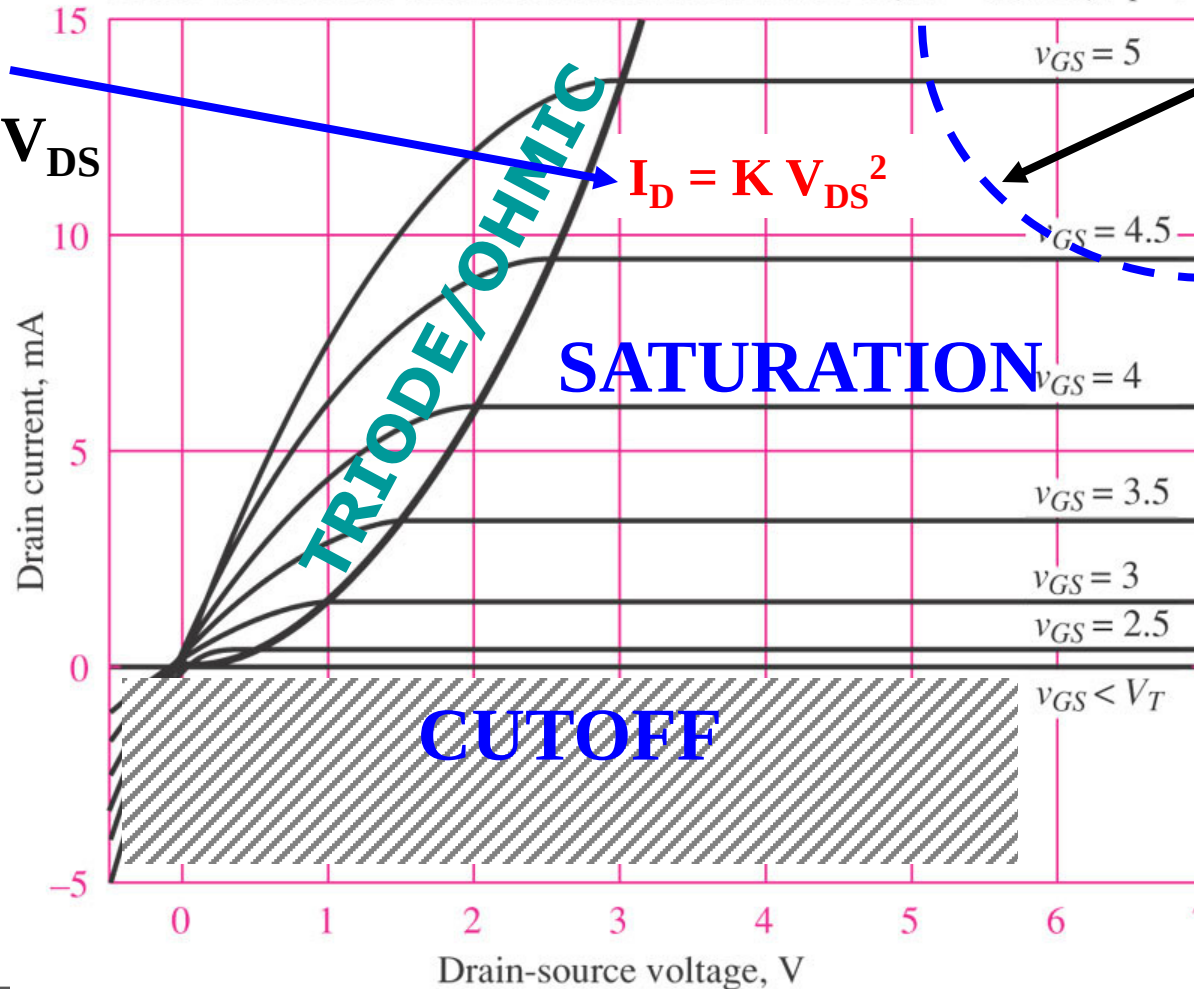
Too much power and the transistor burns out



Operating Regions

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Drain curves for n -channel enhancement MOSFET; $K = 0.0015$, $V_T = 2$

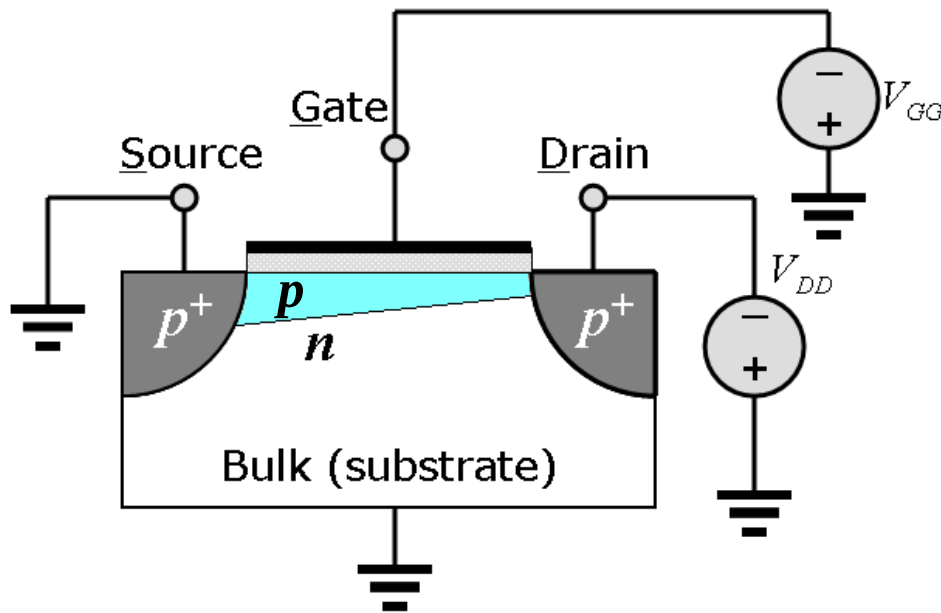


When

$$V_{GS} - V_T = V_{DS}$$

BREAKDOWN

p-Channel MOS (PMOS)



The PMOS operates on the same principle as the NMOS only that the charge carrier types are reversed. As a consequence of this swap:

- (1) It is p-type conducting channel that is formed in an n-type bulk
- (2) It requires a negative threshold voltage in order to form the channel

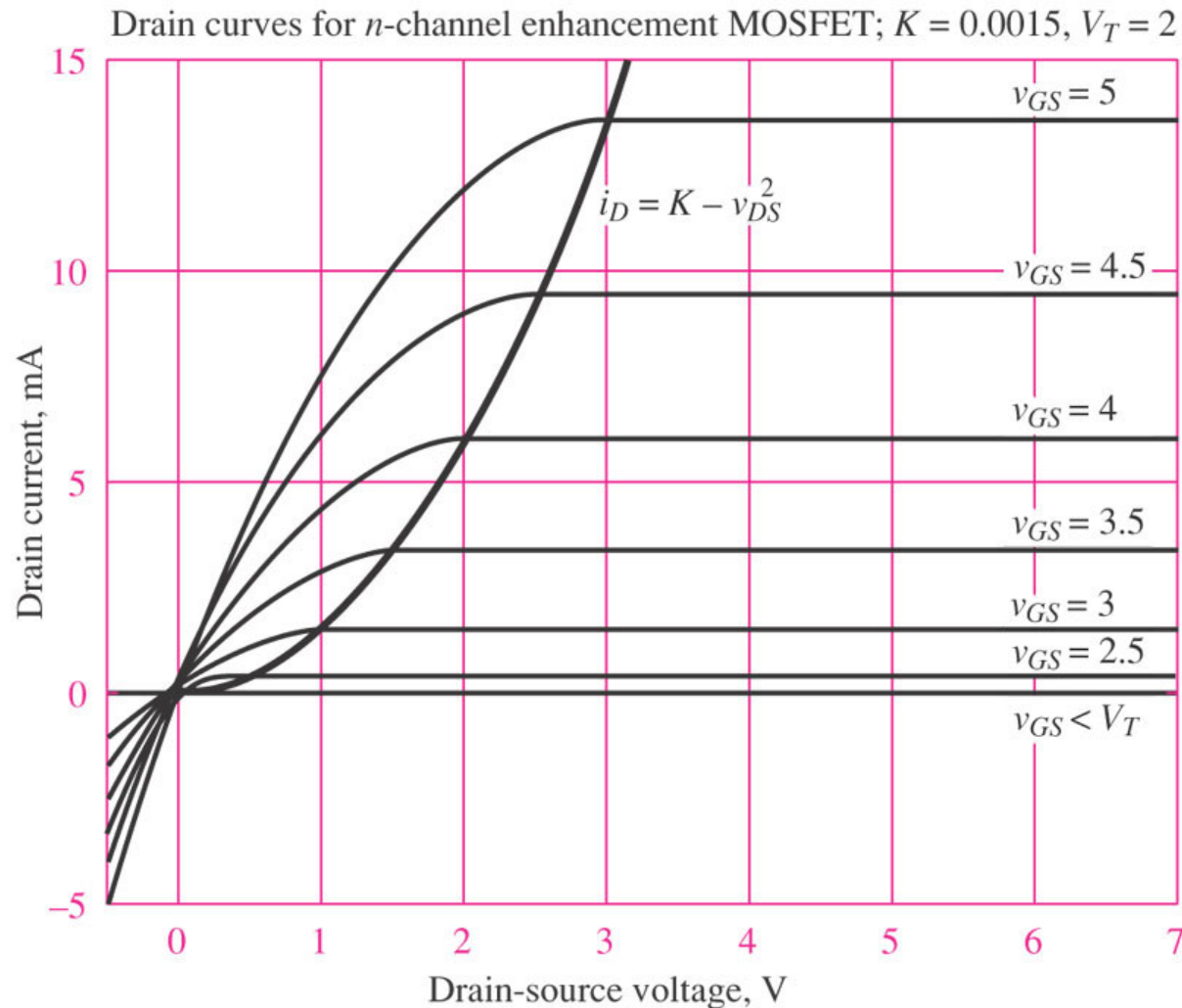
NMOS vs PMOS

NMOS

PMOS

Applications of each mode

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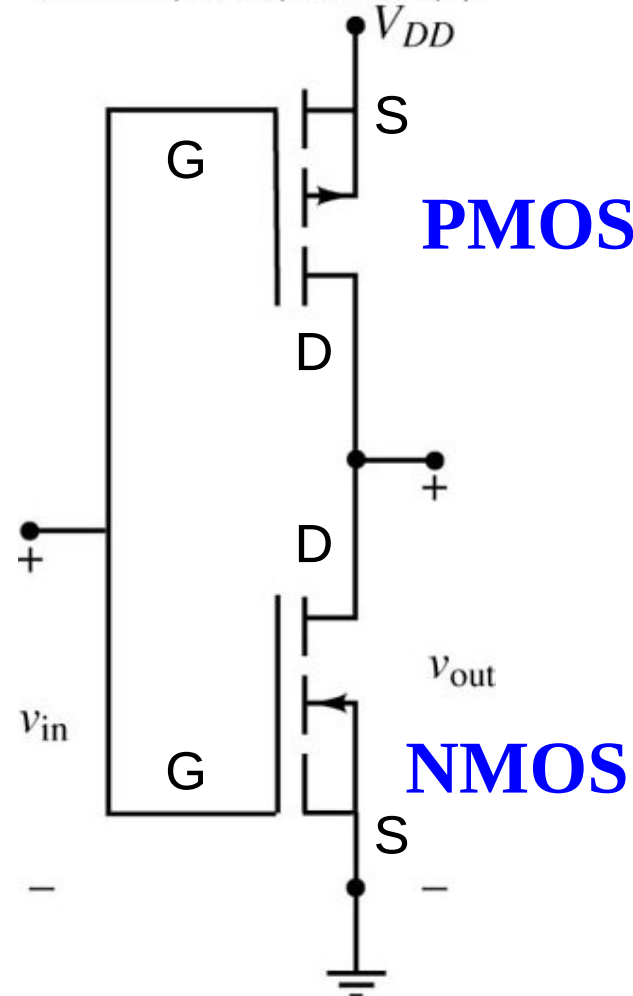


CMOS Gates

- Most MOSFET switches make use of CMOS (Complementary MOS) technology
- Makes use of the complementary characteristics of PMOS and NMOS
- Complementary: If the PMOS part is ON, then the NMOS part must be OFF
- Easy to fabricate and require a single supply voltage

CMOS Inverter (1)

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PMOS

**PMOS source
connected to V_{DD}**

**NMOS source
connected to 0V**

NMOS

CMOS Inverter (2)

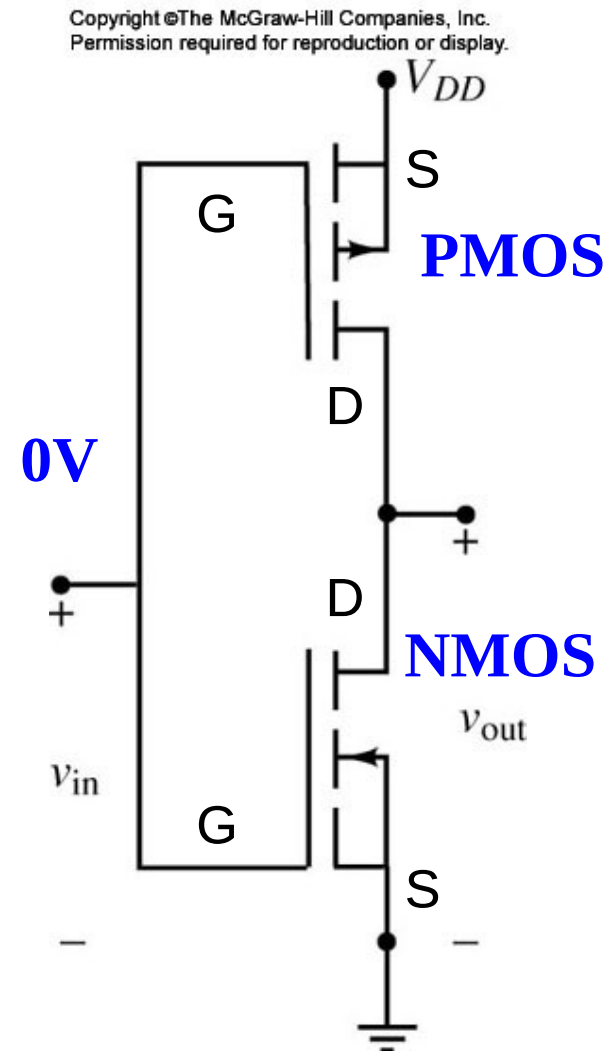
When $v_{in} = 0V$ (Logic 0)

NMOS $V_{GS} = 0V$ (OFF)

Open Circuit

PMOS $V_{GS} = -5V$ (ON)

Closed Circuit



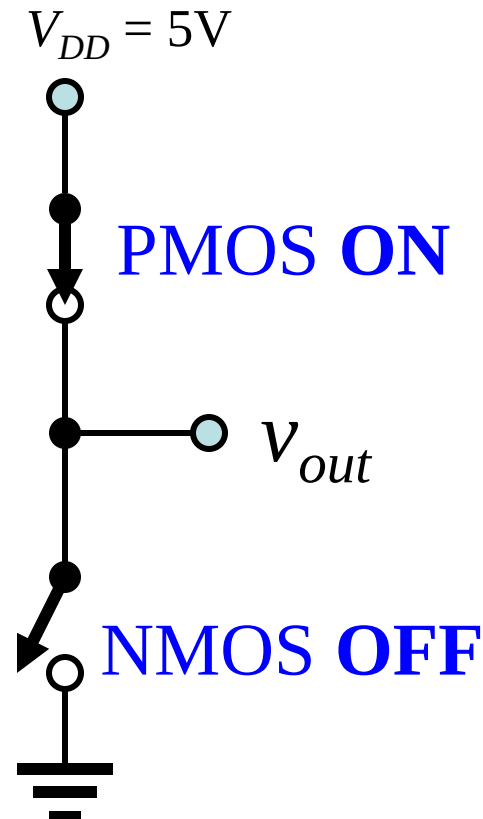
CMOS Inverter (3)

When $v_{in} = 0V$ (Logic 0)

NMOS OFF

PMOS ON

$v_{out} = 5V$ (Logic 1)



CMOS Inverter (4)

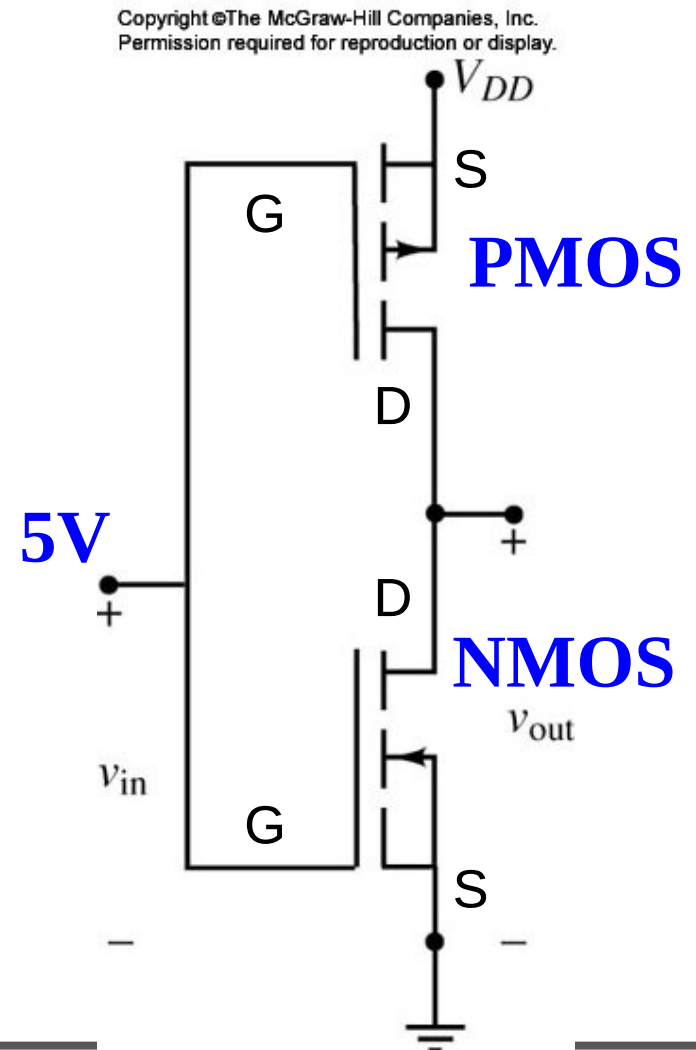
When $v_{in} = 5V$ (Logic 1)

NMOS $V_{GS} = 5V$ (ON)

Short Circuit

PMOS $V_{GS} = 0V$ (OFF)

Open Circuit



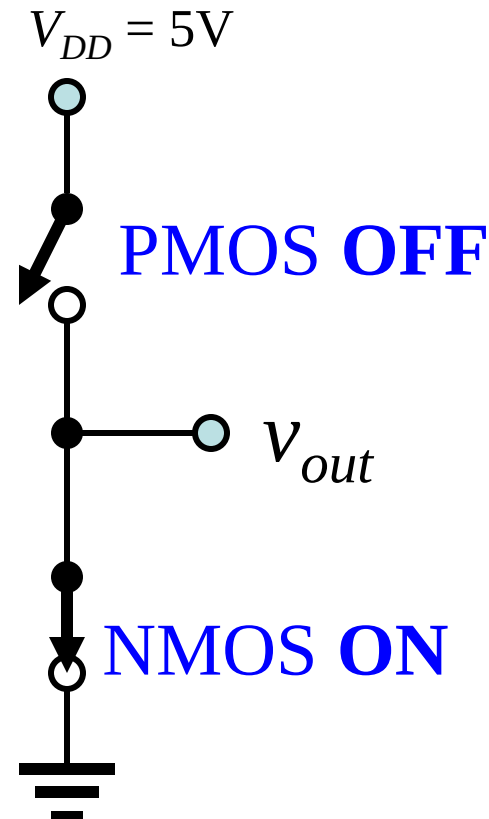
CMOS Inverter (5)

When $v_{in} = 5V$ (Logic 1)

NMOS ON

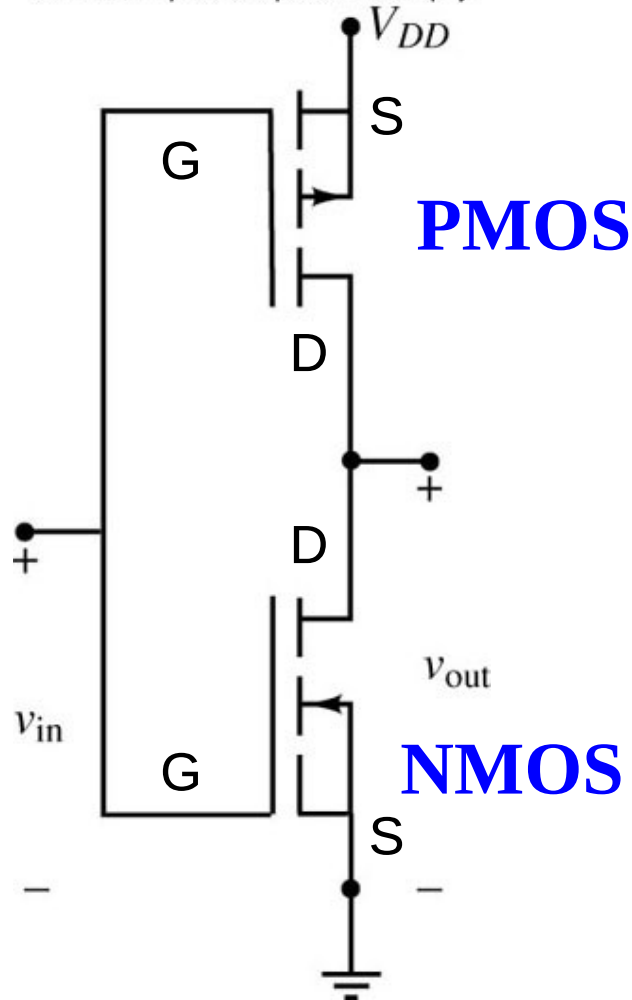
PMOS OFF

$v_{out} = 0V$ (Logic 0)



CMOS Inverter (6)

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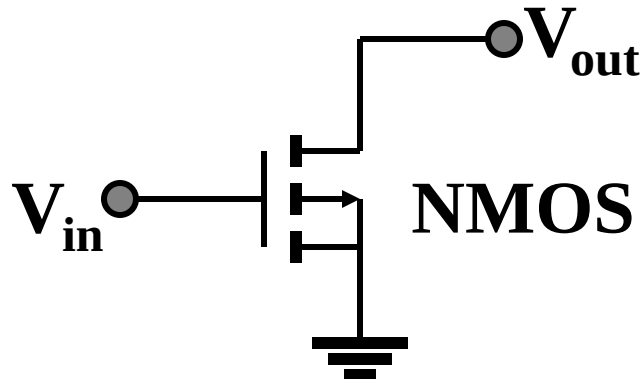


v_{in}	v_{out}
0	1
1	0

Input is inverted
at the output

Effect on Output

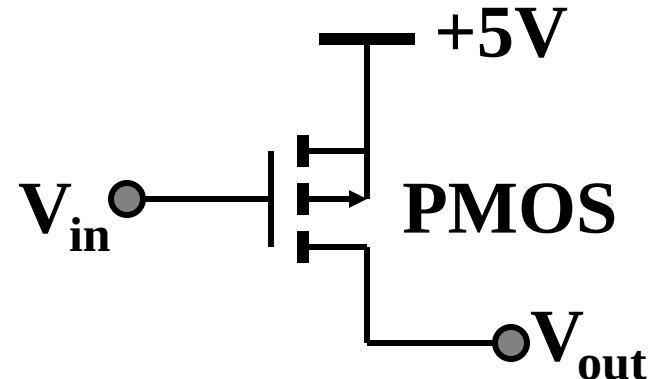
Pull Down



$V_{in} = 1$: NMOS is ON

Switch Closes: $V_{out} = 0$

Pull Up

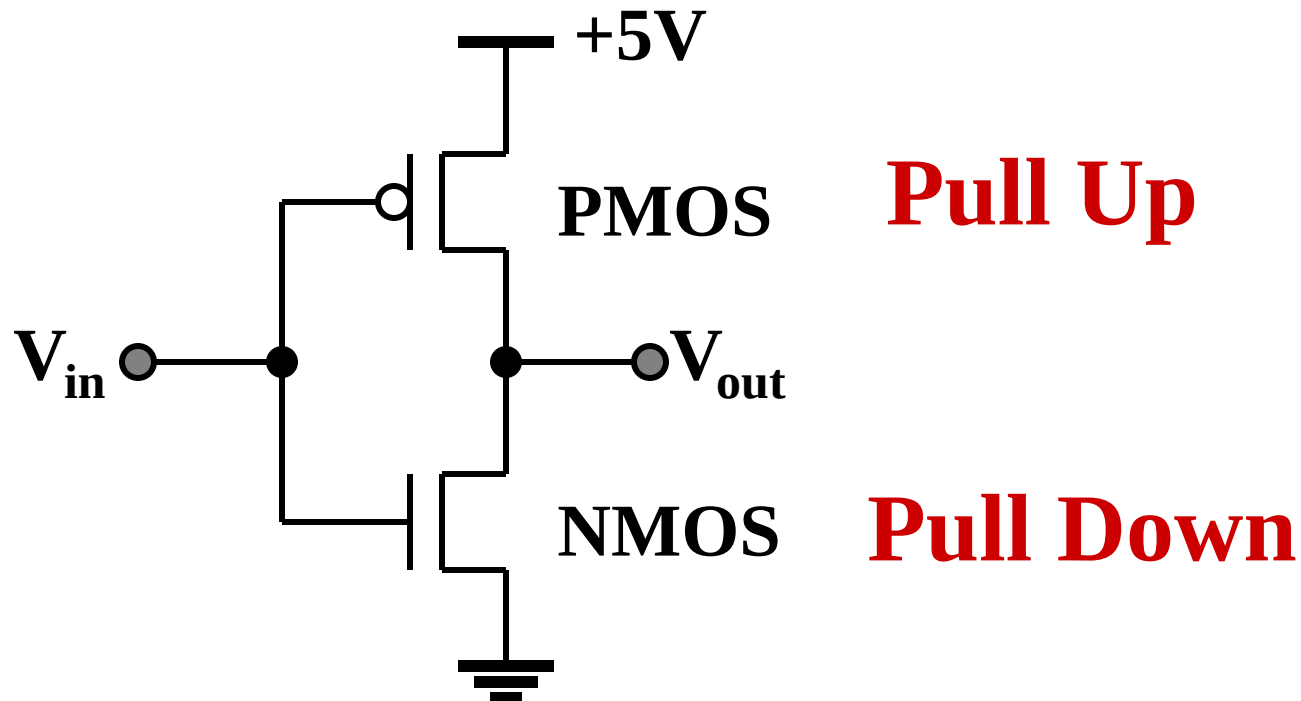
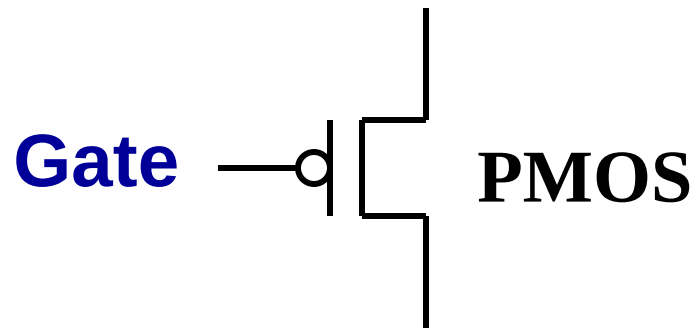
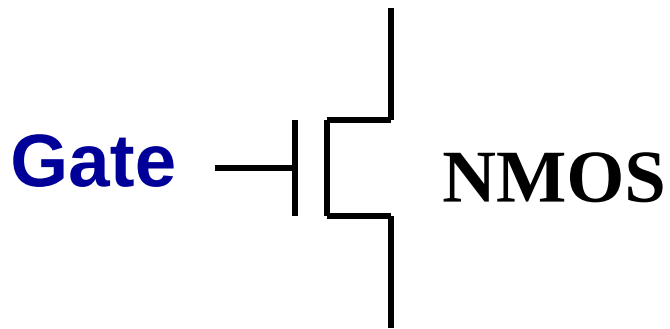


$V_{in} = 0$: PMOS is ON

Switch Closes: $V_{out} = 1$

Source is always connected to a fixed voltage: NMOS(0V), PMOS(5V)

Simplified symbol for MOS

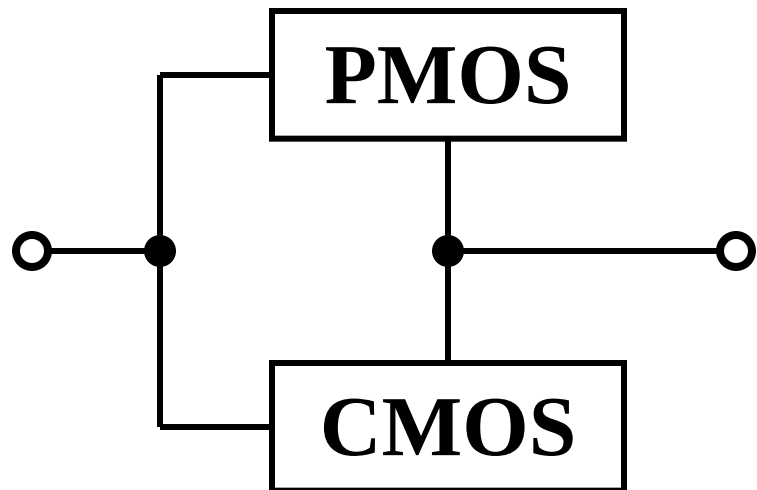


CMOS Logic

CMOS logic gate
comprises 2 parts:

PMOS: Pull-Up

NMOS: Pull-Down

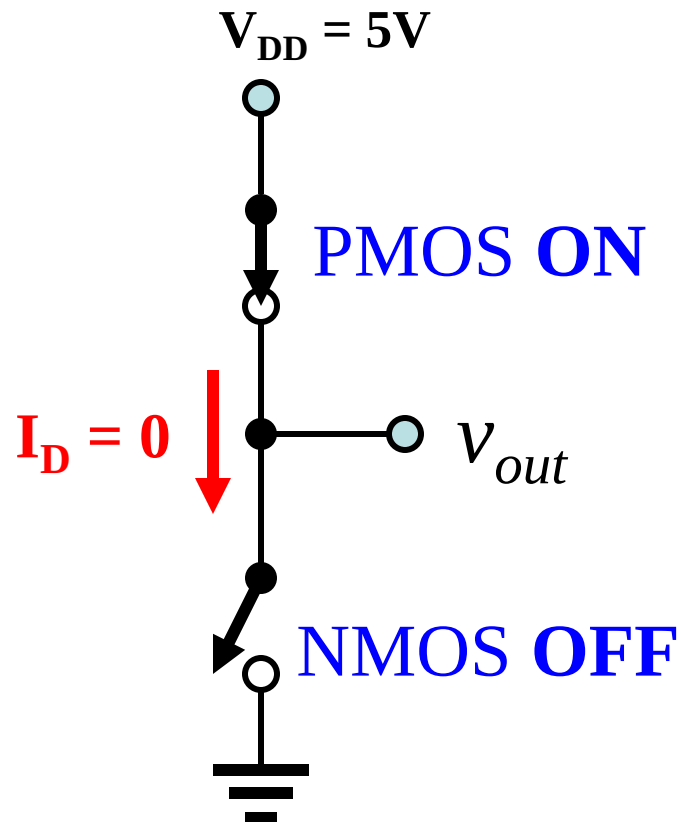
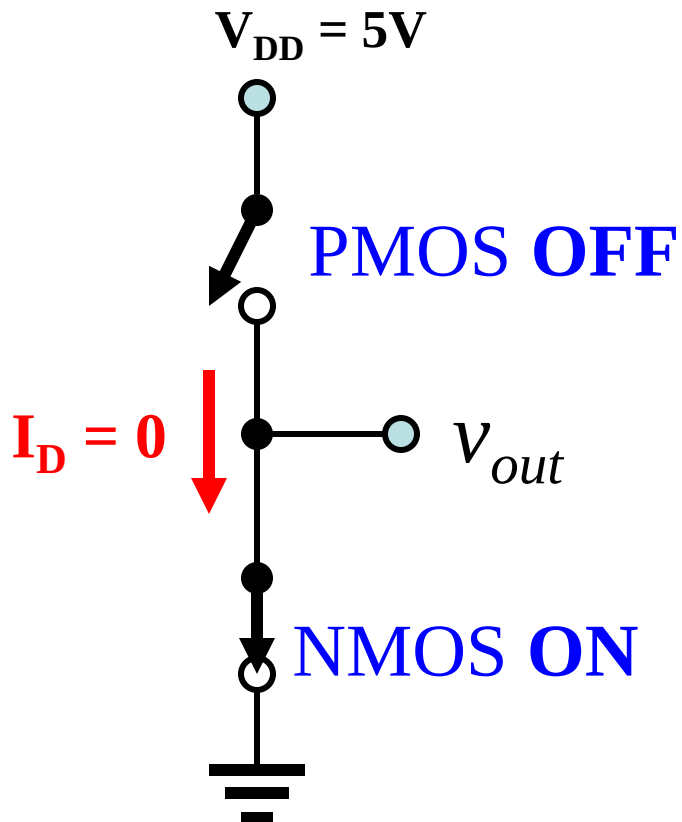


Important: When one part is on, the other must be off

Therefore no current flows in either low or high states

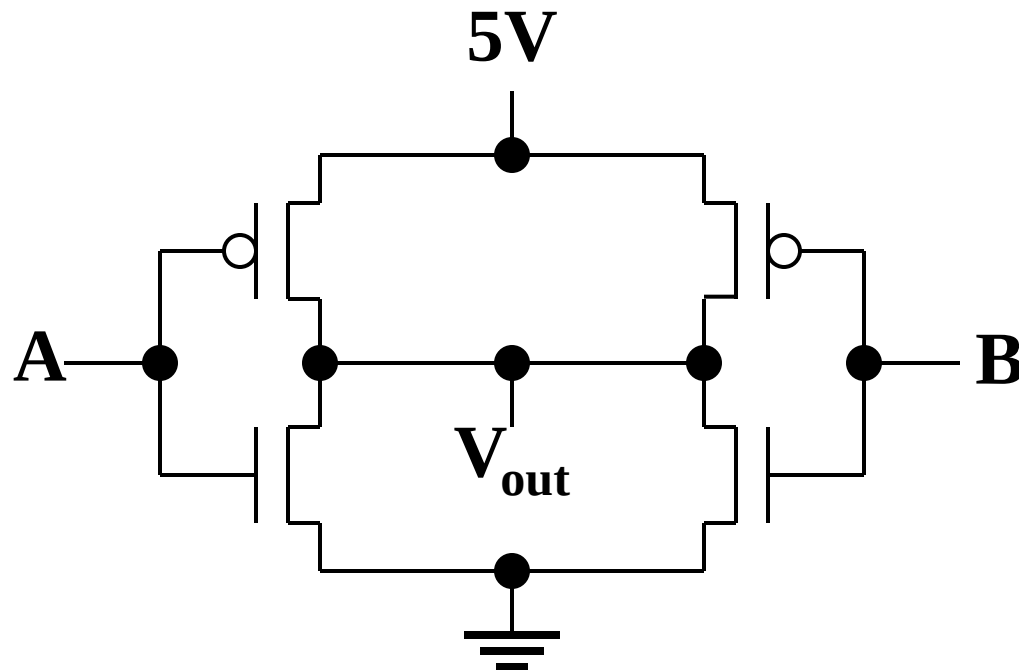
Power dissipated only during the state transition

Complementary function



Example of a bad CMOS circuit

Is the complementary function satisfied?

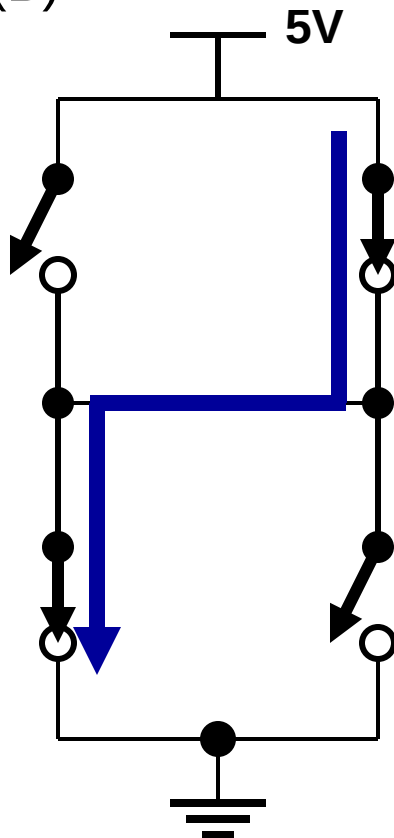


Can you identify the problem state?

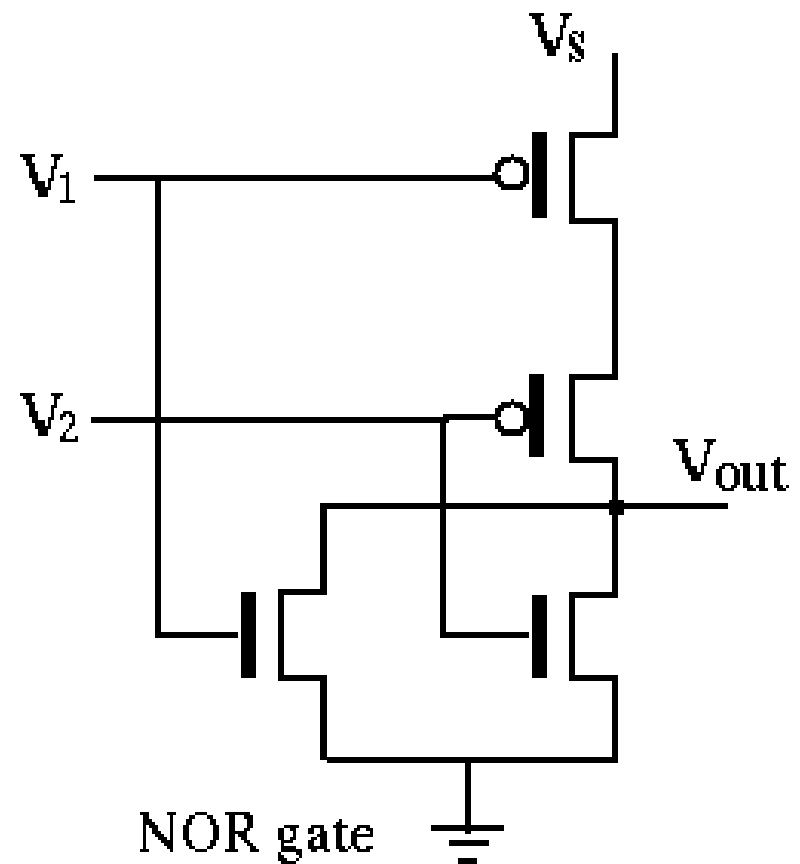
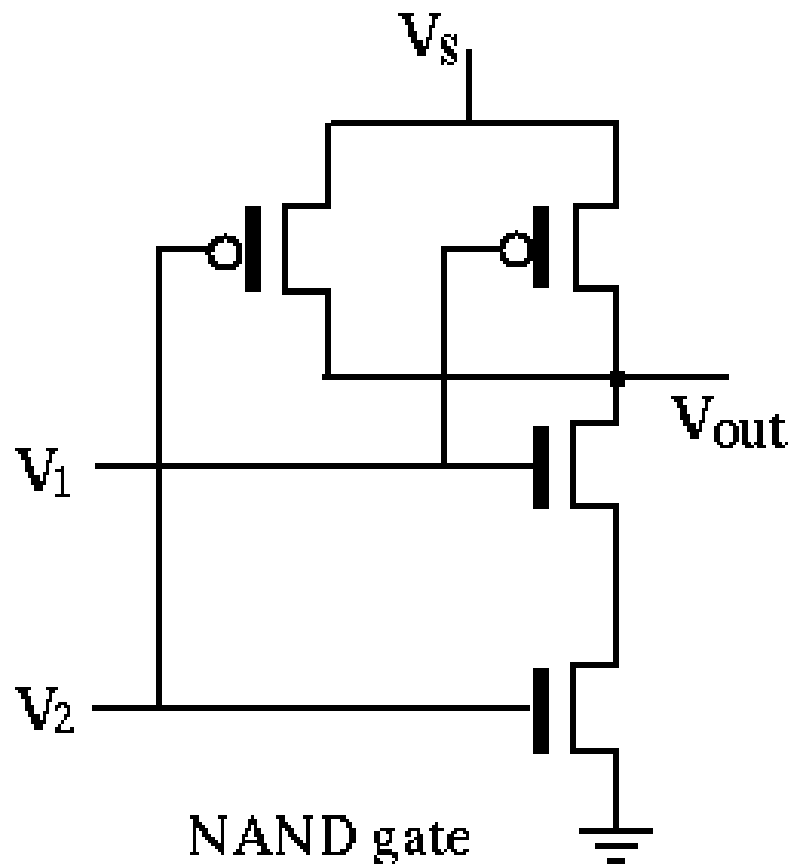
Example of a bad CMOS circuit

Problem combination: A and B are complementary:
ie $\text{NOT}(A) + B$ or $A + \text{NOT}(B)$

**Current shoots through
MOSFETs burn out**



CMOS NAND and NOR gates



MOS Concept Checklist 1

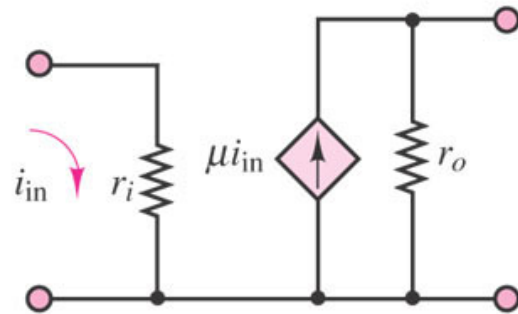
- Draw the symbol of a MOSFET and label the 3 terminals.
- What are the 3 terminals of a MOSFET?
- What is meant by the Threshold Voltage?
- For an NMOS, what is the condition required to turn on the device?

MOS Concept Checklist 2

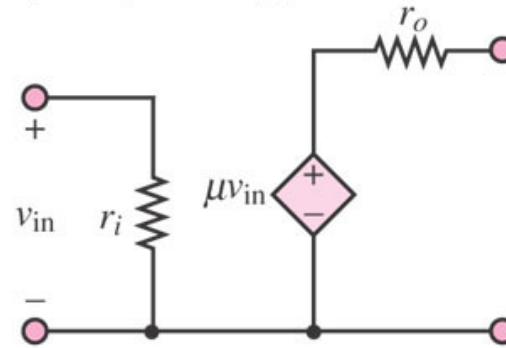
- What is meant by Saturation mode? Condition?
- What is meant by Linear/Triode/Ohmic mode?
- Which mode is used for amplifiers?
- Which modes are used for switches?

MOSFETs for Amplifiers

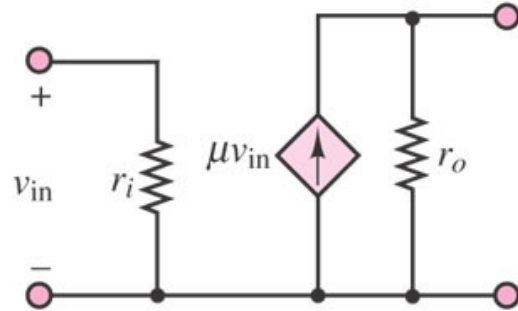
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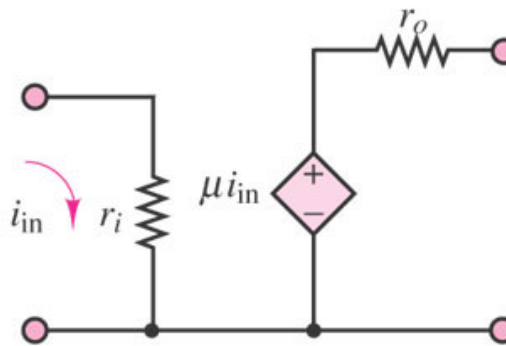
(a) Current-controlled current source



(b) Voltage-controlled voltage source



(c) Voltage-controlled current source



(d) Current-controlled voltage source

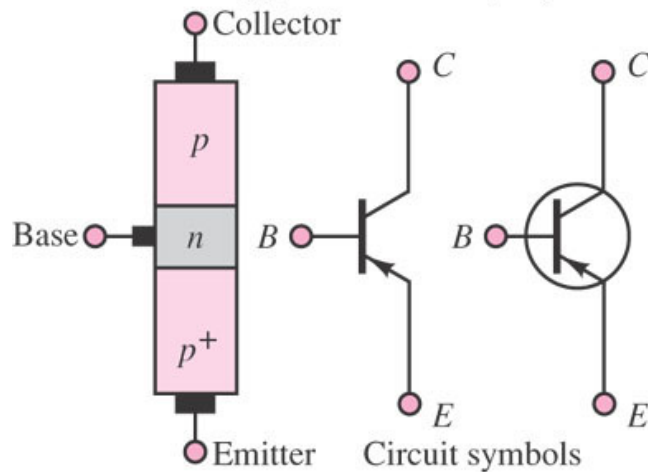
MOSFET

MODE:

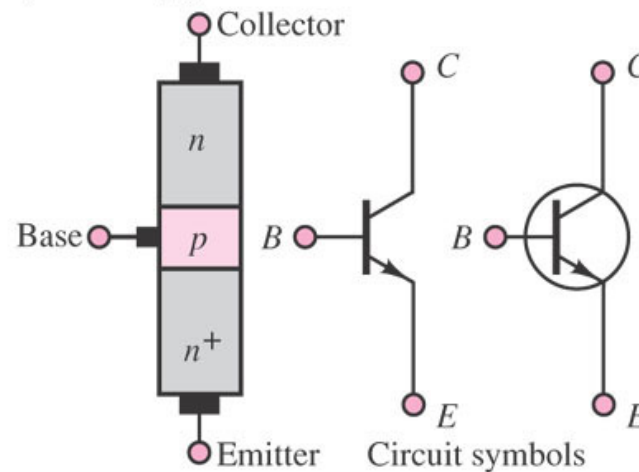
Structure of BJT

- 3 sections alternately doped semiconductor NPN or PNP
- Middle section always very thin: called the base (B)
- Comprises three terminals (one for each section): emitter (E), base (B) and collector (C)
- Majority carriers move from E to C

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pnp transistor



npn transistor

Transistor: NPN vs PNP

NPN

PNP

Large Signal Model

The BJT is also characterized by 3 operating regions. Note that each region takes on a different means from that of the MOSFET.

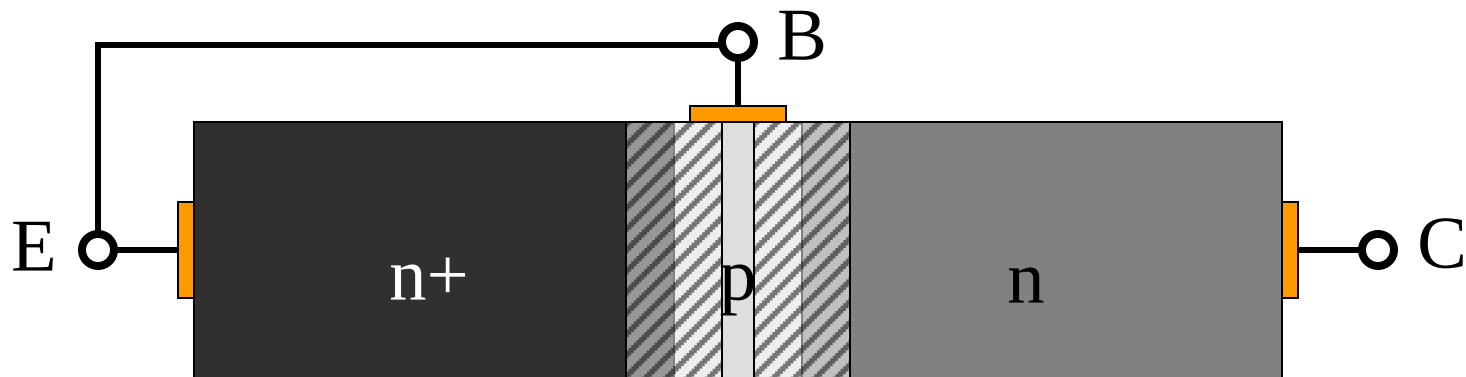
For a BJT, we can think that the emitter current (I_E) is controlled by the base current (I_B) and the voltage across the collector and emitter (V_{CE})

- **Cut-off region**
 - > BE junction is reverse-biased
- **Linear active region**
 - > BE junction is forward-biased ($V_{BE} = V_\gamma$ typically around 0.7V)
 - > BC junction is reverse-biased
- **Saturation region**
 - > BOTH BE and BC junctions are forward-biased ($V_{BE} = V_\gamma$)

Cutoff mode

In the cutoff mode, the pn junctions at both the emitter-base and collector-base interfaces are reverse biased. This is similar to having two back to back reverse biased diodes, where it can be seen that no current can flow between the emitter and collector terminals. As such, the transistor is simply off. There is also no current flowing into the base in this mode.

To turn the transistor on, we must forward bias the base-emitter junction



Linear active mode

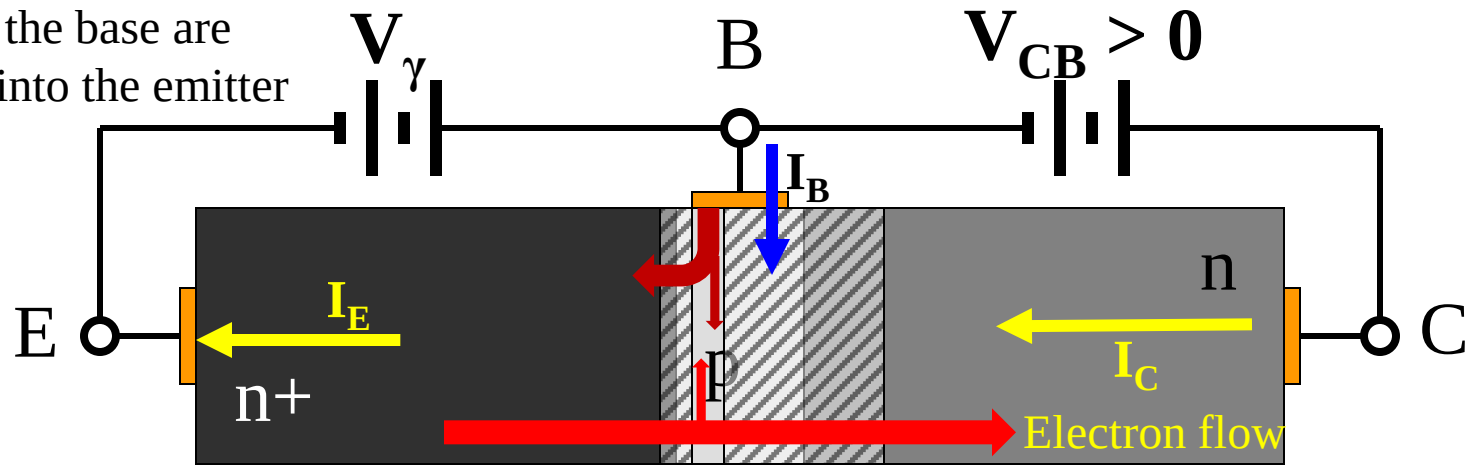
The active region is characterized by a small base current greatly amplified to give a much larger collector current, such that $I_B \ll I_C$

⇒ It is common to express their relationship by a parameter symbolized by β :

$I_C = \beta I_B$, where β is typically large in the active region (from 50 to above 400)

⇒ As a result of this large current gain, we find that $I_C \sim I_E$

Holes in the base are
injected into the emitter



Electrons in the emitter
are injected into the base

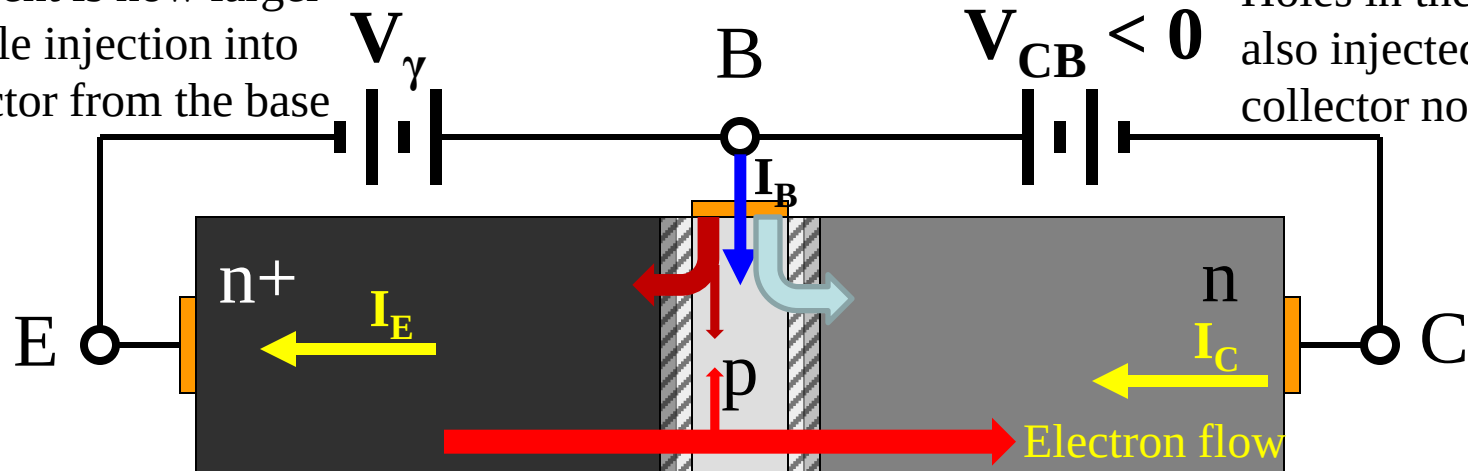
Some of the emitter electrons recombine
in the base but most it is swept into the
collector

Large electric field across the junction sweeps electrons in the base into the collector with minimal recombination occurring in the thin base layer.

Saturation mode

The saturation region is characterized by low current gain between the base and collector.

Base current is now larger due to hole injection into the collector from the base



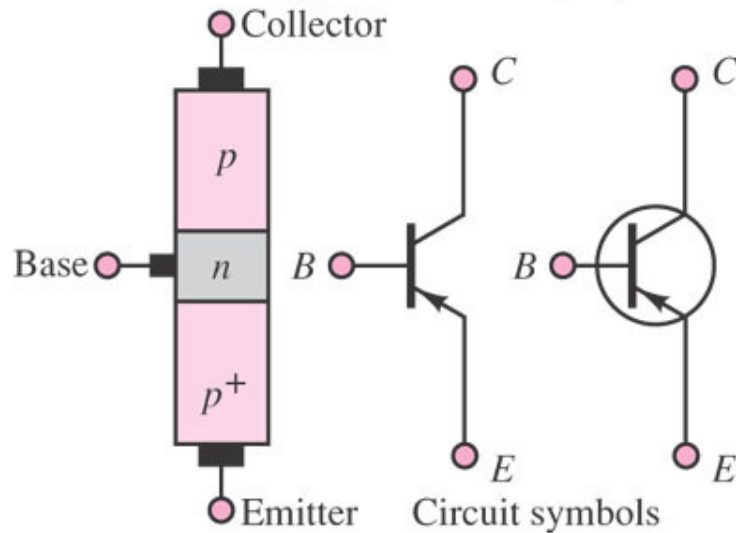
Holes in the base are also injected into the collector now

Potential gradient between collector and emitter is greatly reduced since $V_{CE} < V_\gamma$ (but still positive), having an effect on the collector current

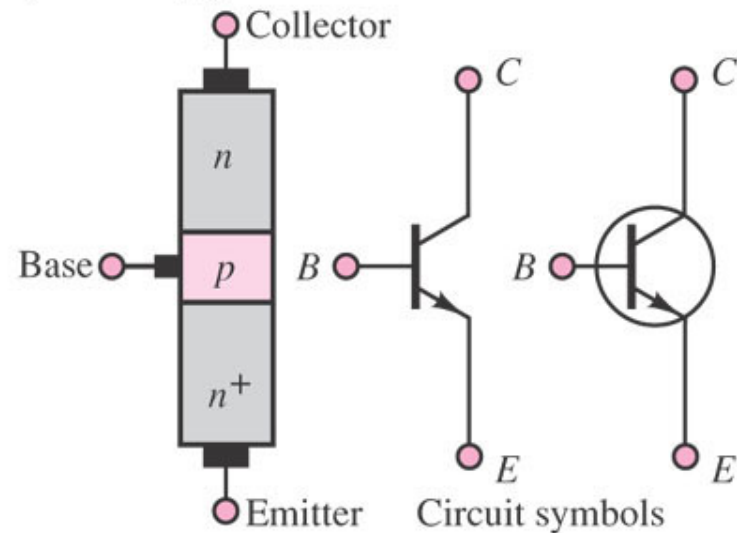
Accelerating electric field across the junction is now switched off. Electrons diffuse into collector.

Power Dissipation

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pnp transistor



npn transistor

$$\text{Power} = I_{CE} V_{CE}$$

This sets a limit on the operating conditions

Too much power and the transistor burns out

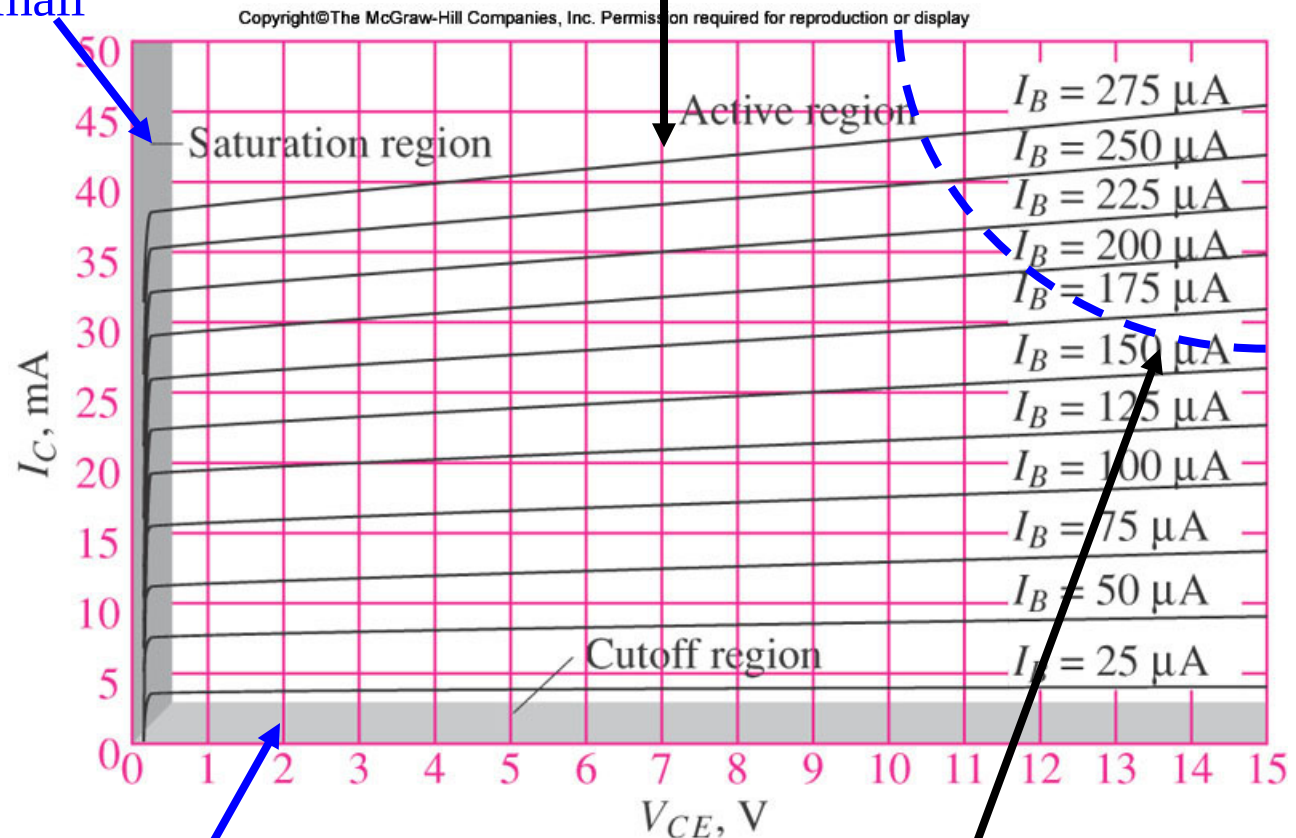
Quick summary on BJT

- BJT: Bipolar junction transistor; also commonly referred to as just bipolar transistor
- Current between C and E (I_C , I_E) controlled by the base current (I_B)
- Bipolar: flow of both holes and electrons (for MOS, either only holes OR electrons flow – unipolar device)

BJT I-V Characteristic

Both junctions are forward-biased; V_{CE} is small

BE forward-biased, CB reverse-biased
(amplifier operation)

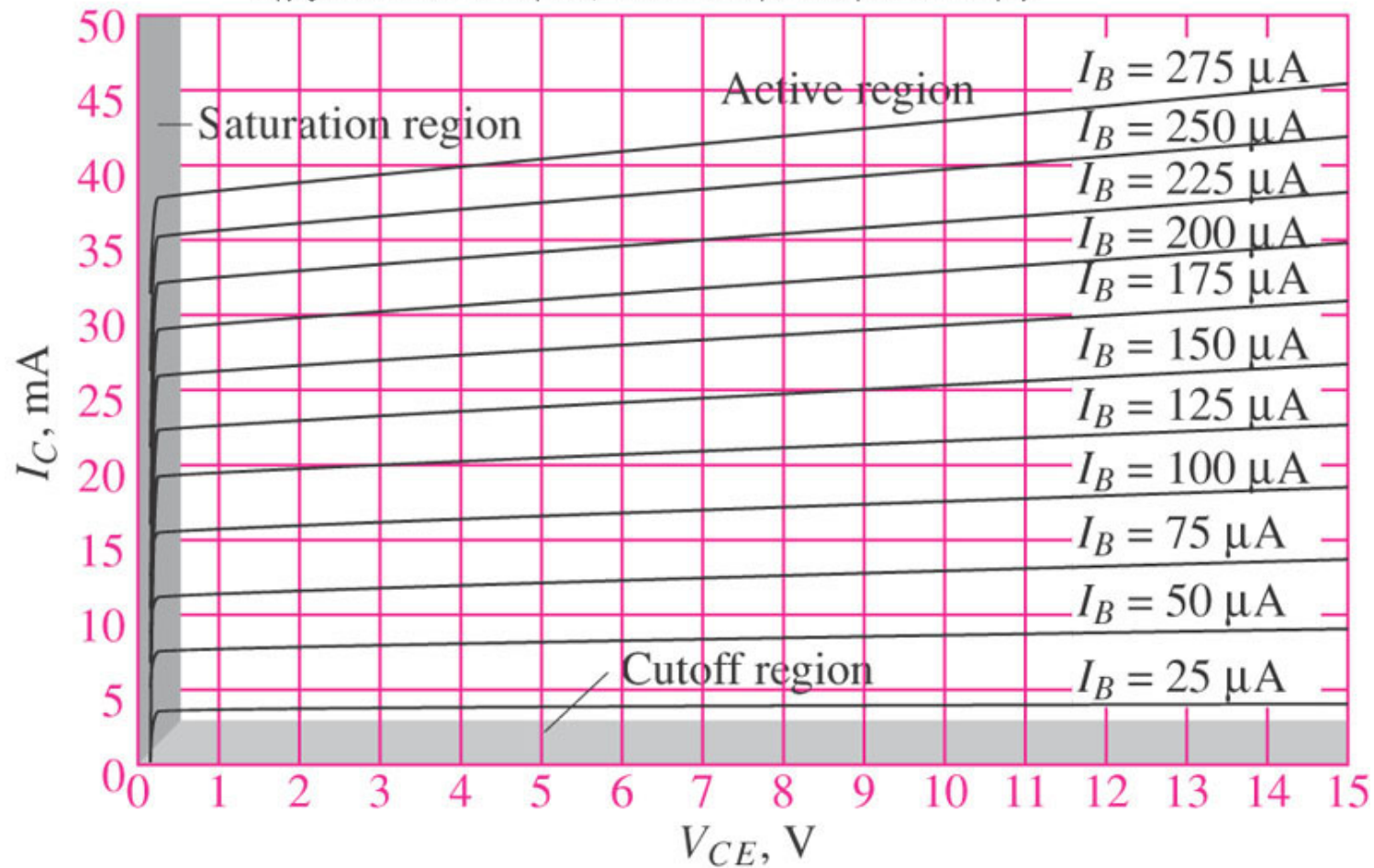


Both junctions are reverse-biased

Breakdown region: Physical limit of operation of the device

Applications of each mode

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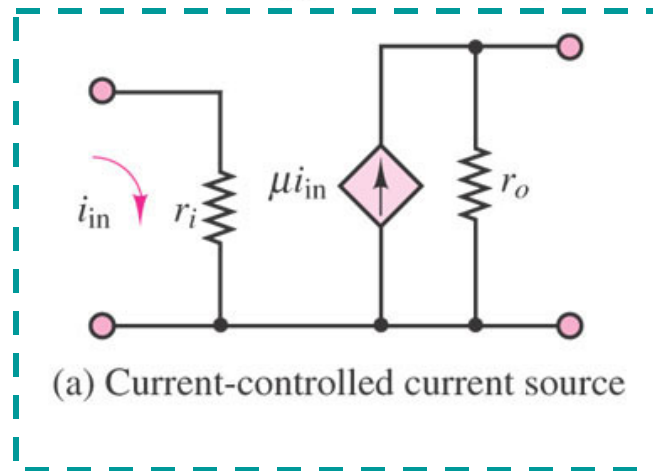


(b)

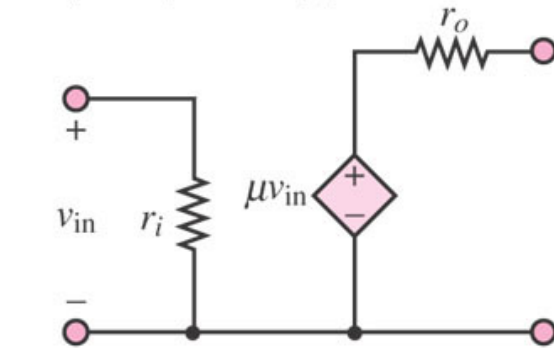
Transistors for Amplifiers

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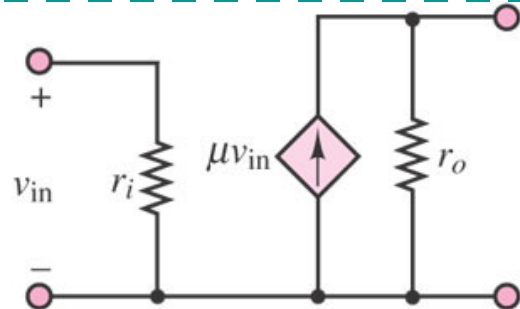
BJT



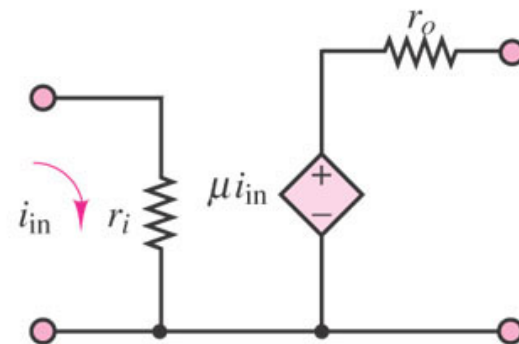
(a) Current-controlled current source



(b) Voltage-controlled voltage source



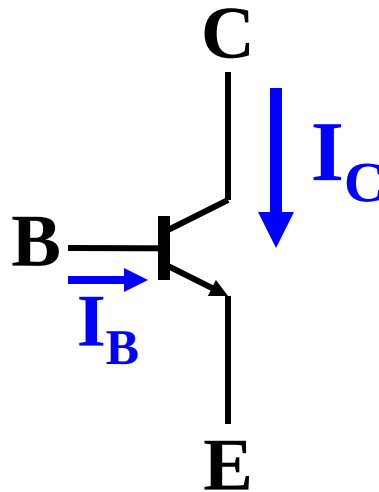
(c) Voltage-controlled current source



(d) Current-controlled voltage source

MODE:

Transistors as Switches



In Cut-Off:

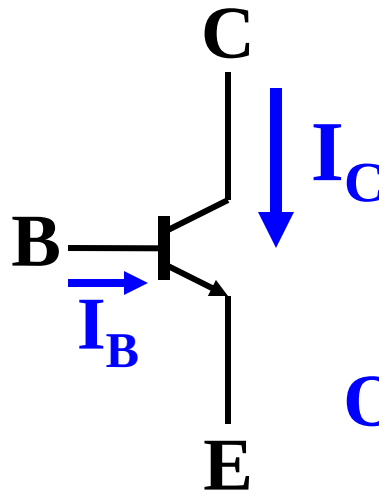
Input: $V_{BE} < 0.7V$, $I_B \approx 0$

Output: $I_C \approx 0$

No current thru' terminals (C & E)

Equivalent to an **OPENED** Switch (**OFF**)

Transistors as Switches



In Saturation:

Input: $V_{BE} = 0.7V$, $I_B > 0$

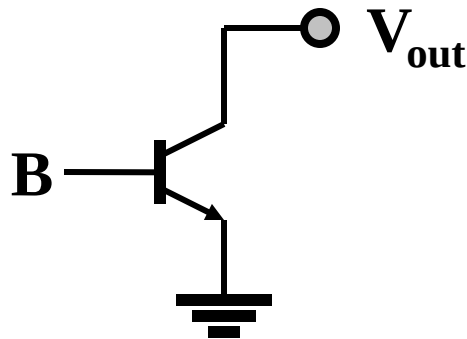
Output: $I_C > 0$ (Large), $V_{CE} = 0.2 V$ (Sat)

Large current thru' terminals (C & E)

Equivalent to a **CLOSED** Switch (**ON**)

Effect on Output

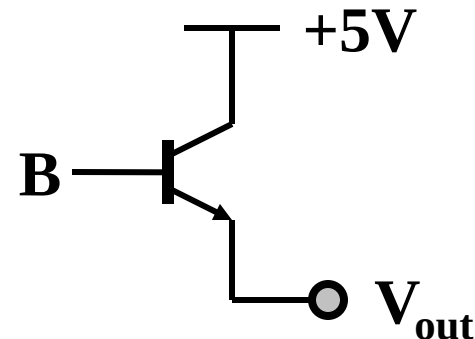
Pull Down



ON: Switch closed

ON: $V_{out} = 0$

Pull Up

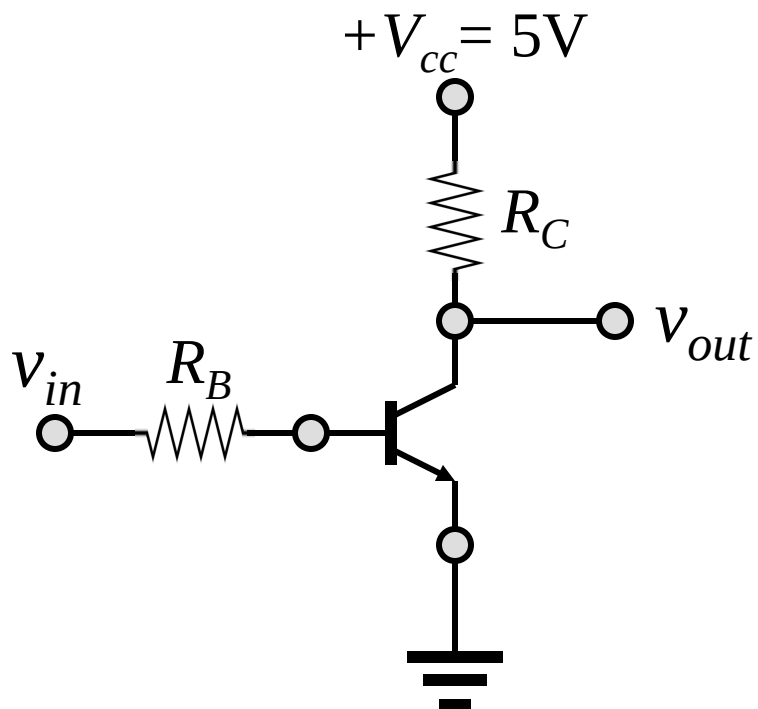


ON: Switch closed

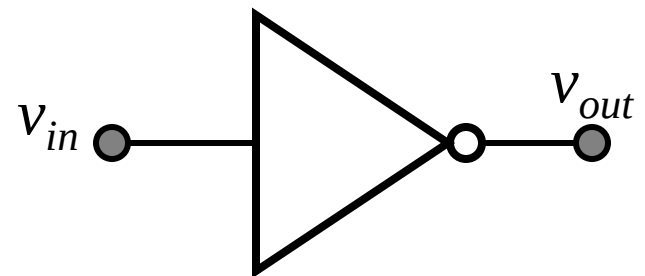
ON: $V_{out} = 1$

RTL Gate

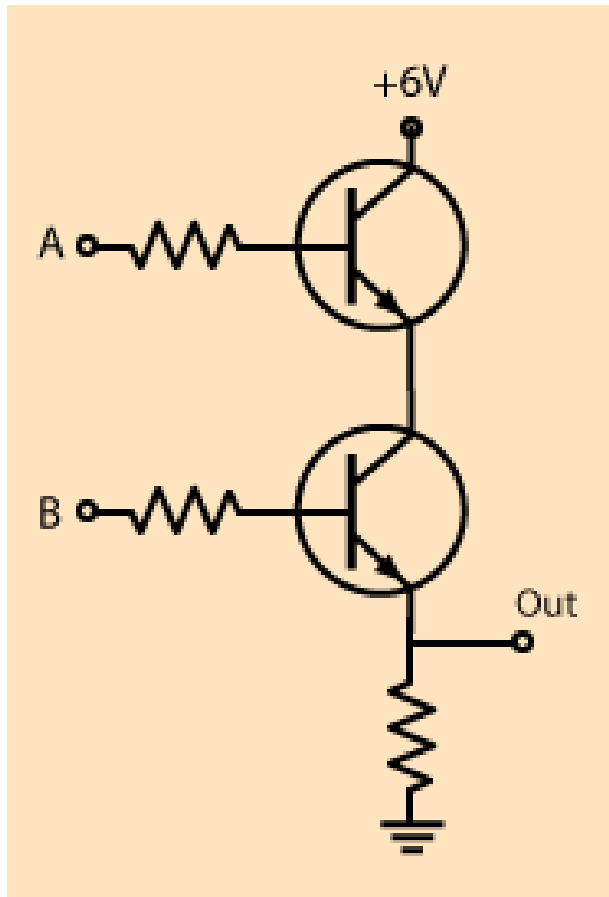
RTL: Resistor-Transistor Logic



Inverter



RTL Gates



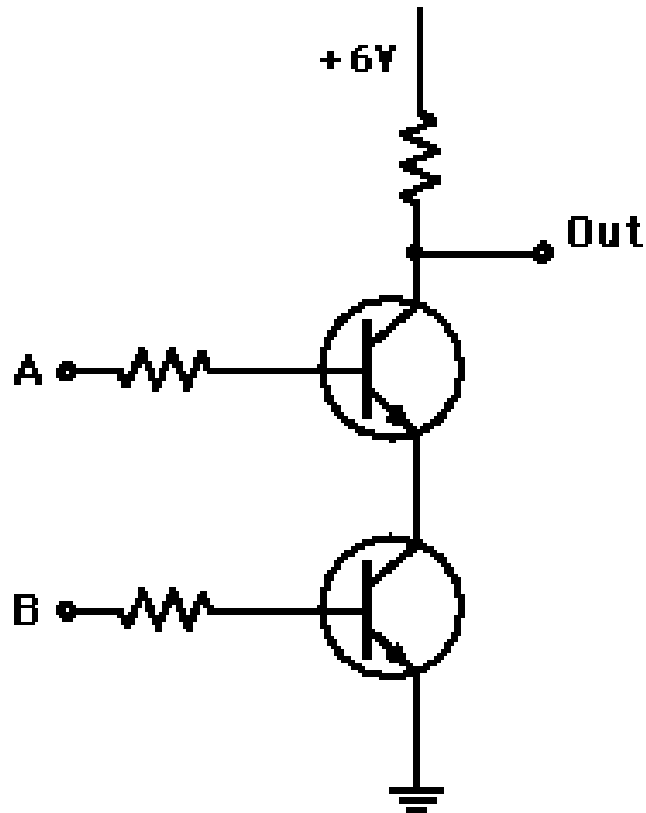
Both transistors must be ON for Out to be 1

Both A & B must be 1 in order for Out to be 1

All other combinations of A & B will give Out = 0

AND gate

RTL Gates



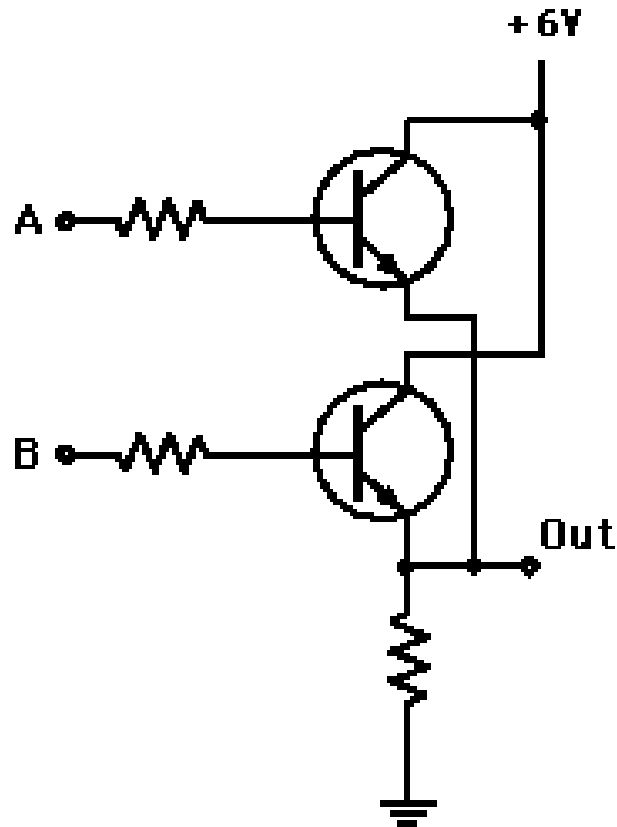
Both transistors must be ON for Out to be 0

Both A & B must be 1 in order for Out to be 0

All other combinations of A & B will give Out = 1

NAND gate

RTL Gates

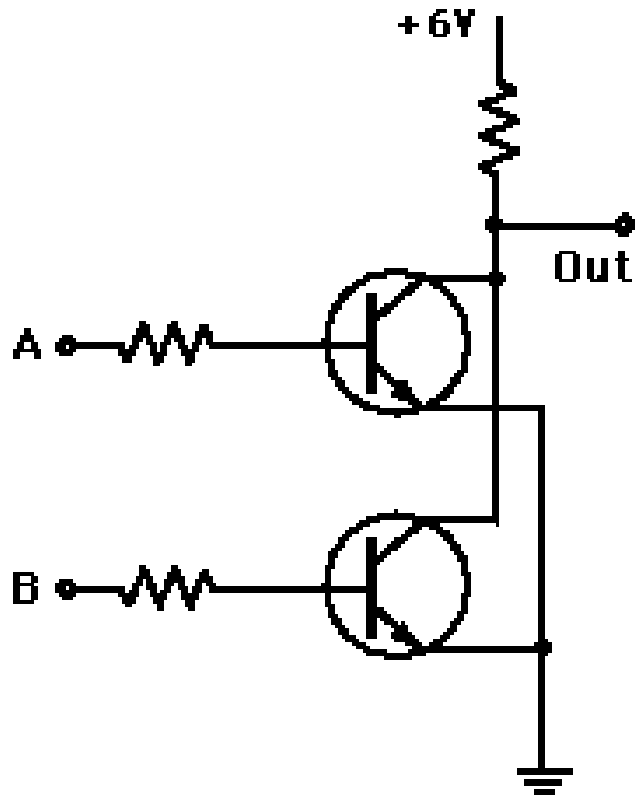


Out = 1 as long as
either transistor is ON

Out = 1 as long as
either A or B = 1

OR gate

RTL Gates



Out = 0 as long as
either transistor is ON

Out = 1 as long as
either A or B = 1

NOR gate