

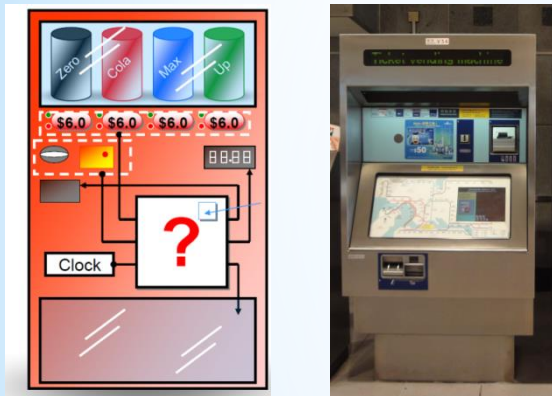
Outline

- 5.1 Latch
 - Active High
 - Active Low
- 5.2 Flip-Flop (FF)
 - - SR-, D-, JK-, T- FFs
- 5.3 Master-Slave FF
- 5.4 Edge-Triggered FF
- 5.5 Synchronous and Asynchronous Operation
- 5.6 Flip-Flop timing

Two classes of logic circuits

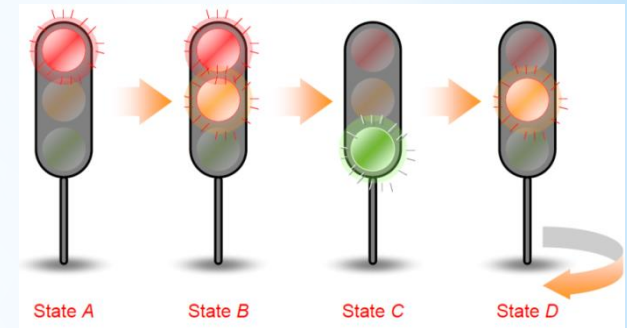
- Combinational logic circuit
 - Previous lectures have been discussed
 - (Generally without a synchronizing clock signal)
- Sequential logic circuit
 - Output depends on present input + past history
 - Memory circuit (previous STATE information) is required
- 2 types of sequential logic circuits
 - Synchronous sequential logic circuit operates with a synchronizing clock signal
 - Asynchronous sequential logic circuit operates without a synchronizing clock

Sequential logic circuit

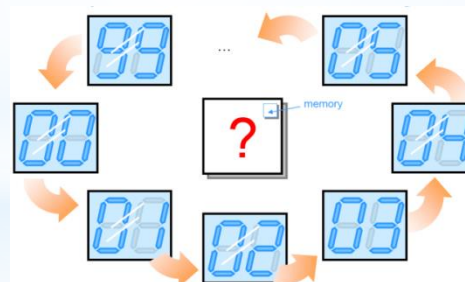


Vending Machine
Food/ drink / MTR tickets

Examples



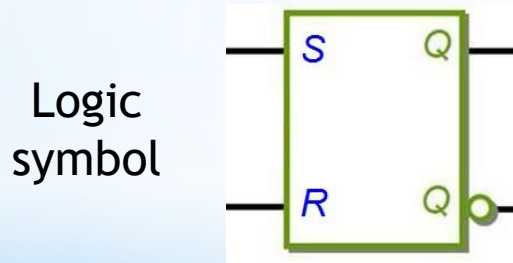
Traffic light controller



Digital counter / clock

5.1 Latch

- The output state of a *latch* is controlled by its excitation input signals
- *Latch* and *flip-flop* are memory devices and implemented using *bistable* circuit - its output will remain in either 0 or 1 state



S stands for set input

R stands for reset input

Q and Q' define the state of the latch

- Q stores the **state** of the latch, or view as
- Storing the data (0 or 1) in Q

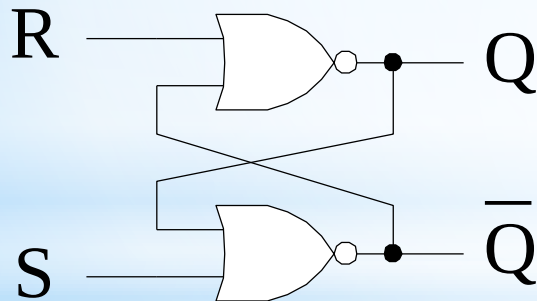
Latch

SR (Set-Reset) latch circuit

When S (set) is set to 1, the output Q will be set to 1.

Likewise, when R (reset) is set to 1, the output Q will be set to 0. It is invalid to set both S and R to 1

Active High Latch



NOR gate implementation

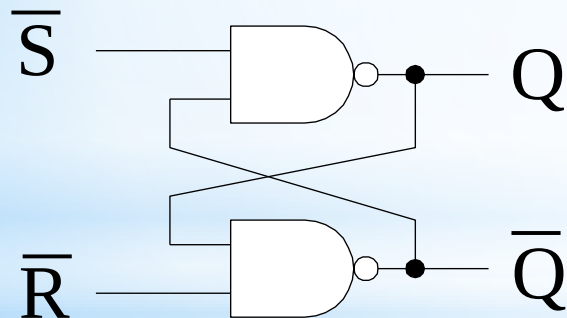
		Next State		
S	R	Q_{t+1}	Q'_{t+1}	State
0	0	Q_t	Q'_t	Hold state
0	1	0	1	Reset state
1	0	1	0	Set state
1	1	0	0	Undefined state

Latch

S'R' latch circuit

When S' (set) is set to 1, the output Q will be set to 0. Likewise, when R' (reset) is set to 1, the output Q will be set to 1. It is invalid to set both S' and R' to 1

Active Low Latch

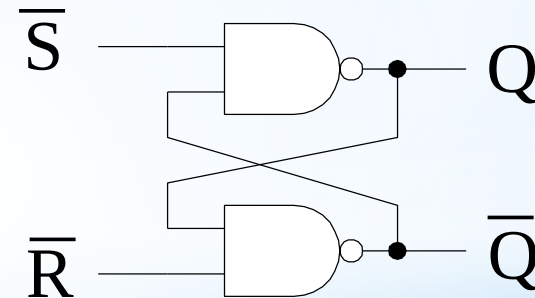
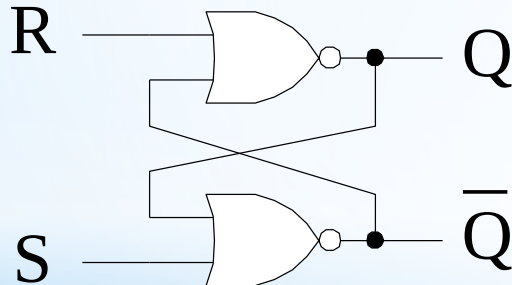


NAND gate implementation

		Next State		
S'	R'	Q_{t+1}	Q'_{t+1}	State
1	1	Q_t	Q'_t	Hold state
1	0	0	1	Reset state
0	1	1	0	Set state
0	0	1	1	Undefined state

Latch

- Note that the input is active high for NOR gate implementation, whereas the input is active low for NAND gate implementation

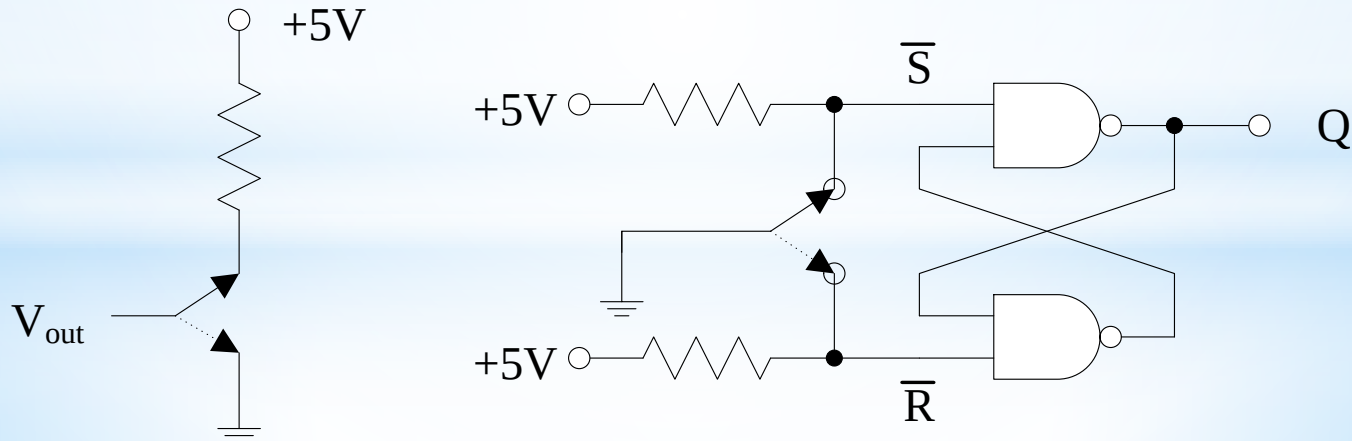


Require a 1 signal to change its state Require a 0 signal to change its state

Application of SR latch

Key de-bouncing circuit:

When pressing a key (or switch), its internal spring may cause the contact point to vibrate for a short period of time to cause a series of “ON” and “OF” condition before settling down.



Drawbacks

- If inputs S , R are unstable (due to noisy interference), output may exhibit unwanted short pulse
- Solution:
 - Prevention of input noise
 - Using “Clocked Flip-Flop (or Gated Latch)”

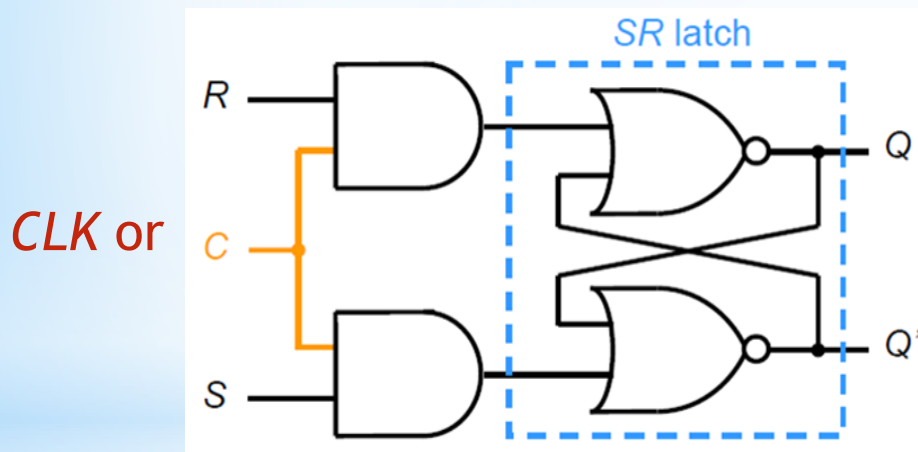
NEVER make $S = R = 1$, you don't want to set and reset the output at the same time - does not make sense !!!!

5.2 Clocked Flip-Flop (FF)

- A latch with a clock input is called clocked FF
- The clock signal is used to synchronize the action of a sequential system, i.e., all actions occur at the same instant
- The output of flip-flop changes according to the inputs and the state of clock signal
- Clocked FF (or level triggered* FF) , master-slave FF and edge-triggered FF
- Four basic types of FF
 - SR FF
 - D-type FF
 - JK FF
 - T FF(* triggered : cause the device to function)

Clocked RS FF

C is a clock signal. Through a AND gate, an enable control is established to pass the **external SR** input to the **internal SR** latch.

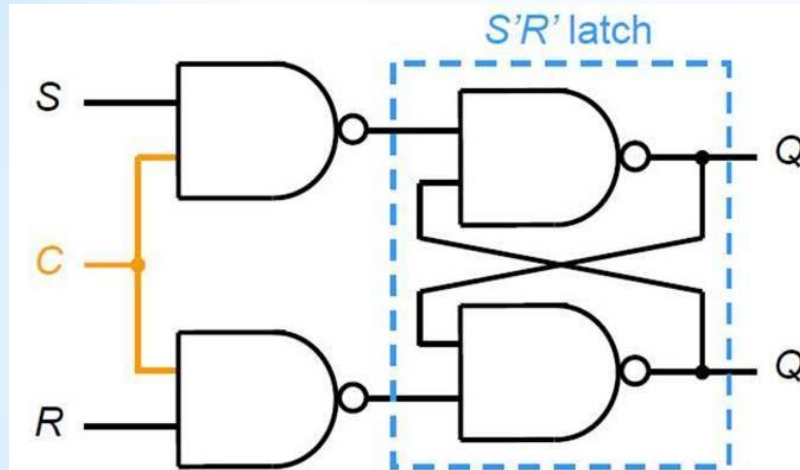


C	S	R	State
0	x	x	Disable
1	0	0	Hold state
1	0	1	Reset state
1	1	0	Set state
1	1	1	Undefined state

When $C = 0$, the two inputs to the SR latch are (0, 0), output Q will be unchanged (state change disabled)

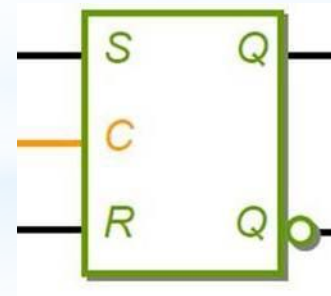
When $C = 1$, the two inputs to the SR latch are (S , R), output Q will follow that of the SR latch (state change enabled)

NAND gate implementation



C	S'	R'	State
0	x	x	Disable (Hold)
1	1	1	Hold state
1	1	0	Reset state
1	0	1	Set state
1	0	0	Undefined state

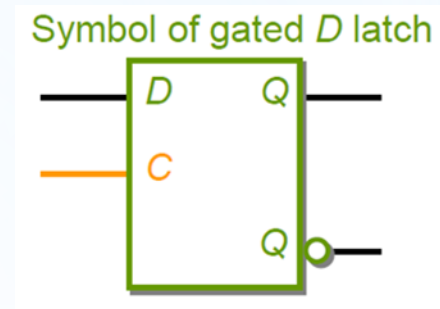
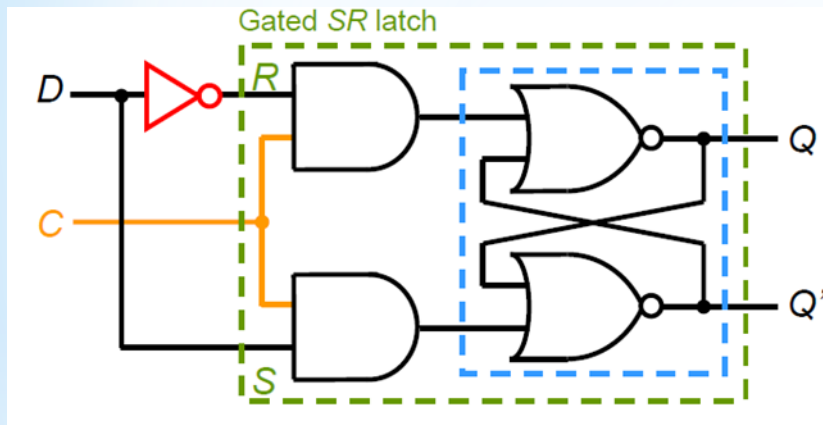
The input is controlled through an “enable input gate”
 When the clock signal **C** is replaced by any control signal and this device is then called gated latch



Logic symbol
of gated
SR latch

Clocked D-type FF

By inverting one of the inputs to the SR FF, a D-type FF is formed. Essentially, the output state follows the input state - may also considered as a single bit buffer, may be called “data FF”



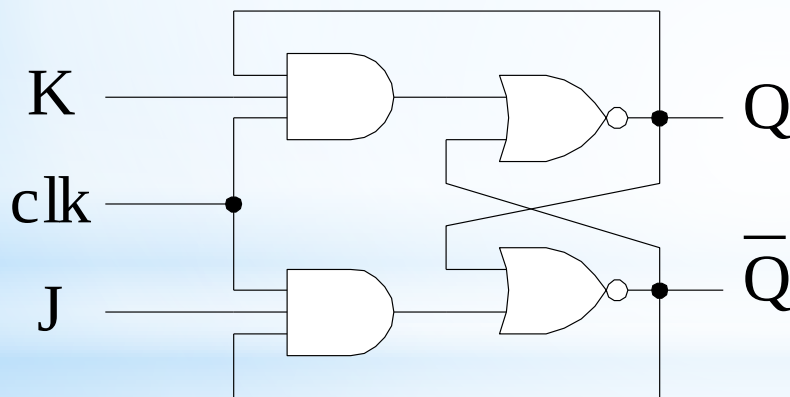
- $S = D, R = D'$
- When $D = 0$,
 - $S = 0, R = 1$ (reset state)
- When $D = 1$,
 - $S = 1, R = 0$ (reset state)
- No undefined state!

C	D	Q	Next state of Q
0	x	Q	Hold state
1	0	0 (= D)	Reset state
1	1	1 (= D)	Set state

Remember in this way:
Output Q follows input D

Clocked JK FF

- The *JK* FF is a refinement of the *SR* FF in that the undetermined state of the *SR* type is defined in the *JK* type. Inputs *J* and *K* behave like inputs *S* and *R* to set and reset (clear) the FF, respectively. The input marked *J* is for *set* and the input marked *K* is *reset*.

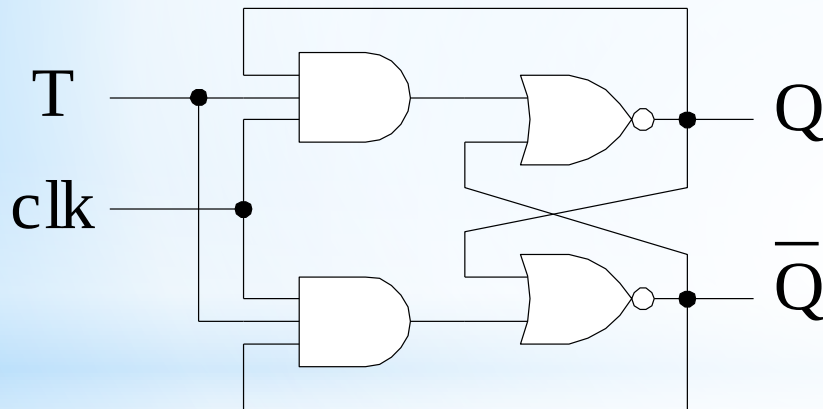


		clk = 0	clk = 1
J	K	Q_{n+1}	Q_{n+1}
0	0	Q_n	Q_n
0	1	Q_n	0
1	0	Q_n	1
1	1	Q_n	$\overline{Q_n}$

Problem: when $\text{clk} = 1$, Q_n will continue to complement its output if $JK = 11$!!!

Clocked T-type FF

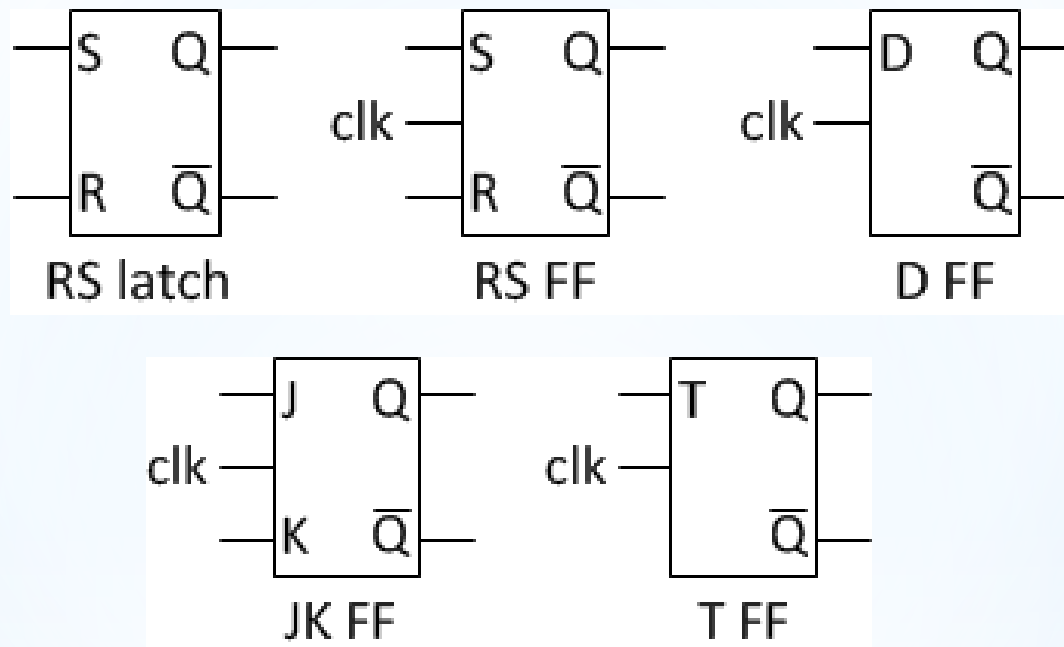
- The toggle (T) FF has a clock input which causes the output state changed for each clock pulse if T is in its active state. It is useful in counter design.



clk	T	Q_{n+1}
0	X	Q_n
1	0	Q_n
1	1	$\overline{Q_n}$

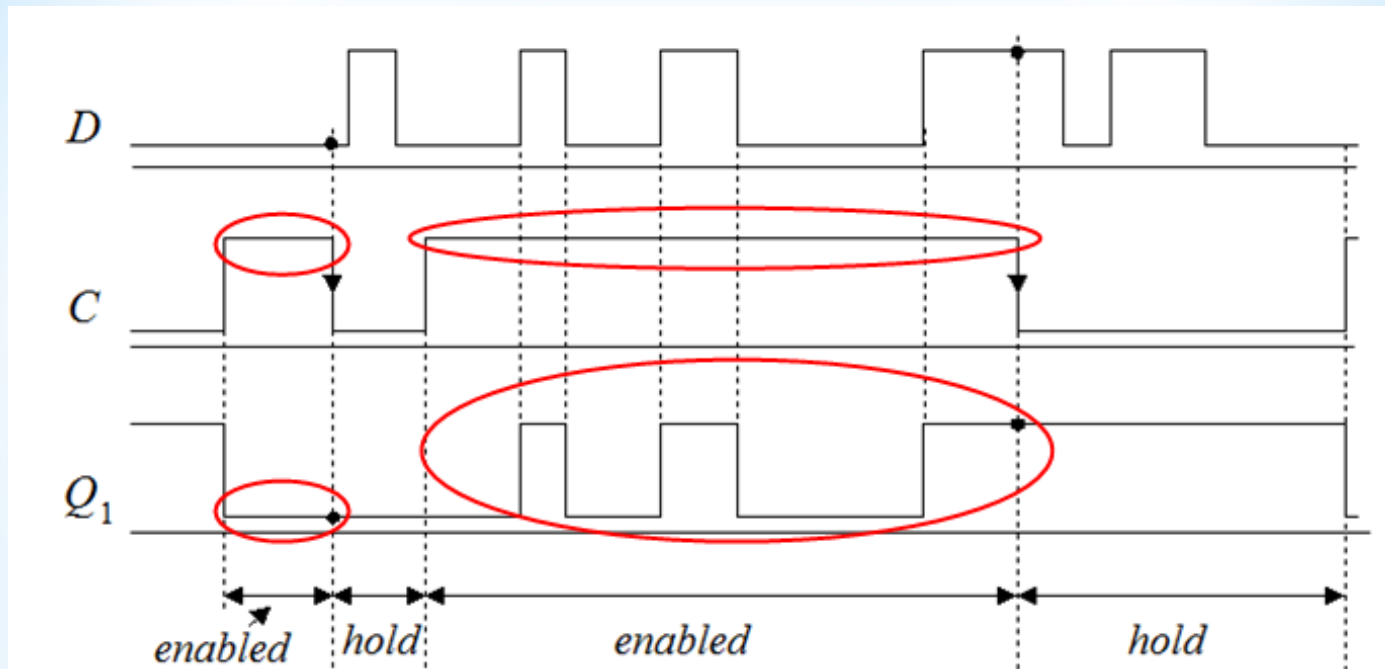
Problem: when $\text{clk} = 1$, Q_n will continue to complement its output if $T = 1$!!!

Logic symbols of various latch and flip-flops



Problem:

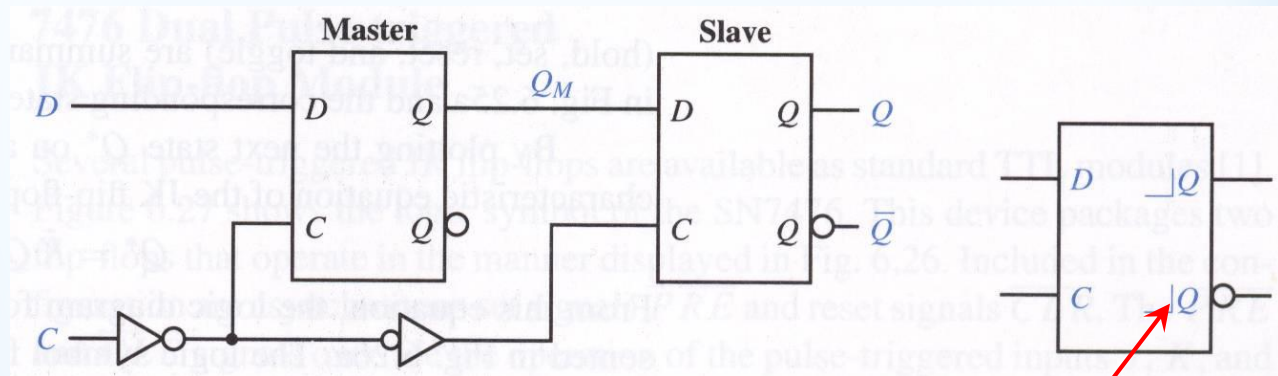
Output is unstable during clock active period, not suitable for synchronized sequential system. We only want a single change for each clock period, otherwise, it is difficult to track the behavior of the system.



The out of the clocked D-FF essentially follows the input when clock is “High”. It then maintains its output state soon as the clock changes to “low”.

5.3 Master-Slave Flip-Flop

- Master-Slave D Flip-Flop

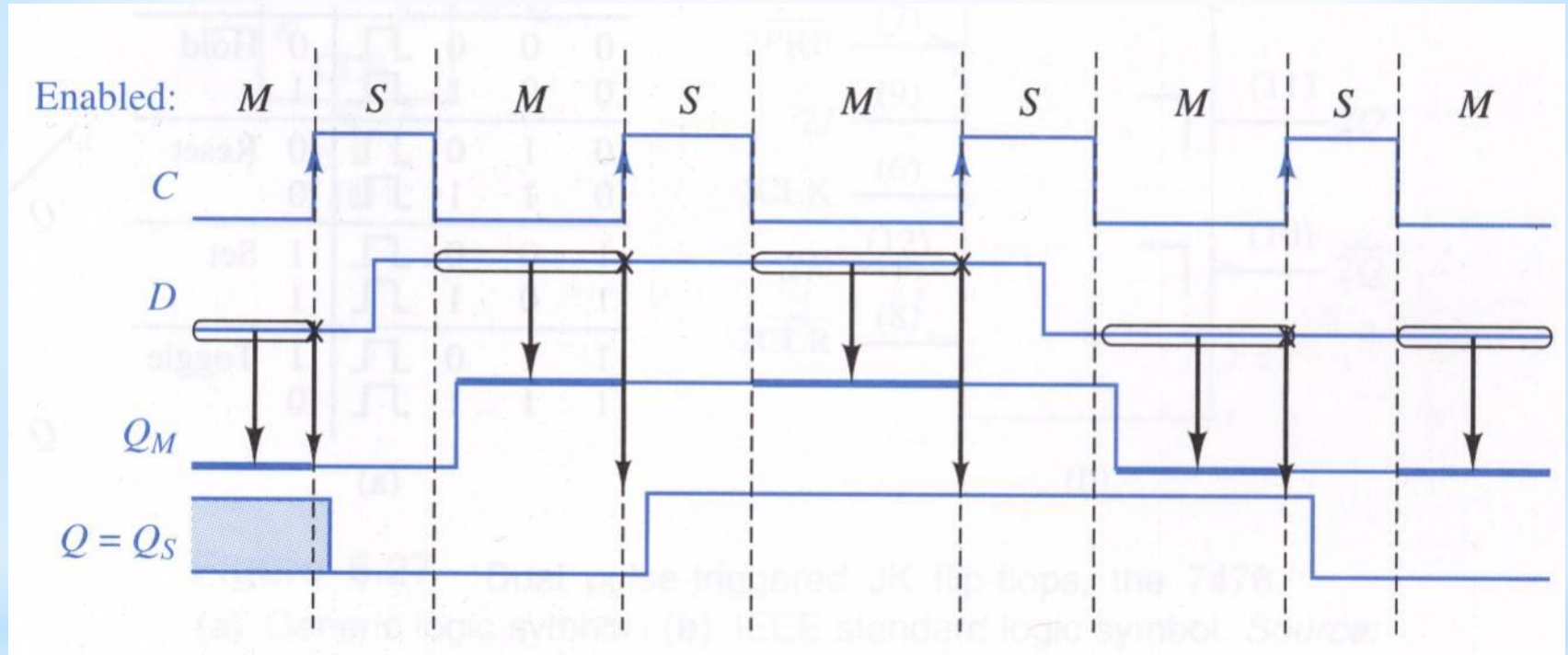


D	Q	C	Q^*
0	0		0
0	1		0
1	0		1
1	1		1

Symbol signifies rising pulse edge triggered

Timing diagram:

Needs both the 0-1 and 1-0 transitions on C in order to operate properly



The output of the slave changes once only for each clock period.

Replacing the D FF with SR, JK or T FF, it becomes a MS SR, MS JK or MS T FF.

Problems with clocked or MS FF

Clocked FF:

The FF's output state change as input change

MS FF:

The master FF's output state change as input change

NOT good for synchronized system operation !!

Solution: Edge-triggered flip-flops

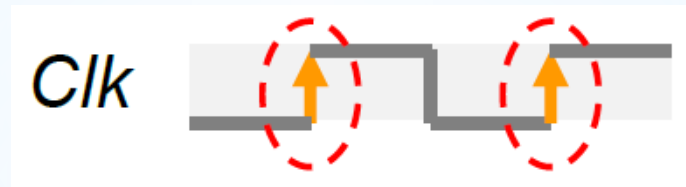
5.4 Edge-Triggered Flip-Flop

- The device only “**reads**” the input and changes its output during either the rising or falling clock edge
 - **edge triggered**
- The flip-flops remains unresponsive to the change at the input until the next triggering edge appears

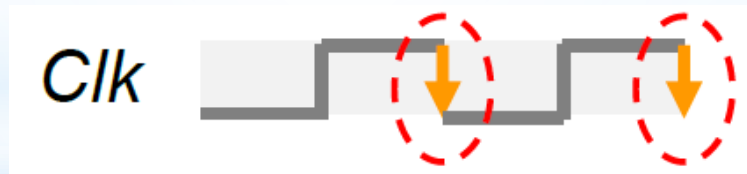
Triggering Edge

The device responds to one edge only!!!

- Positive (rising, leading) edge-triggering: 0-to-1 transition

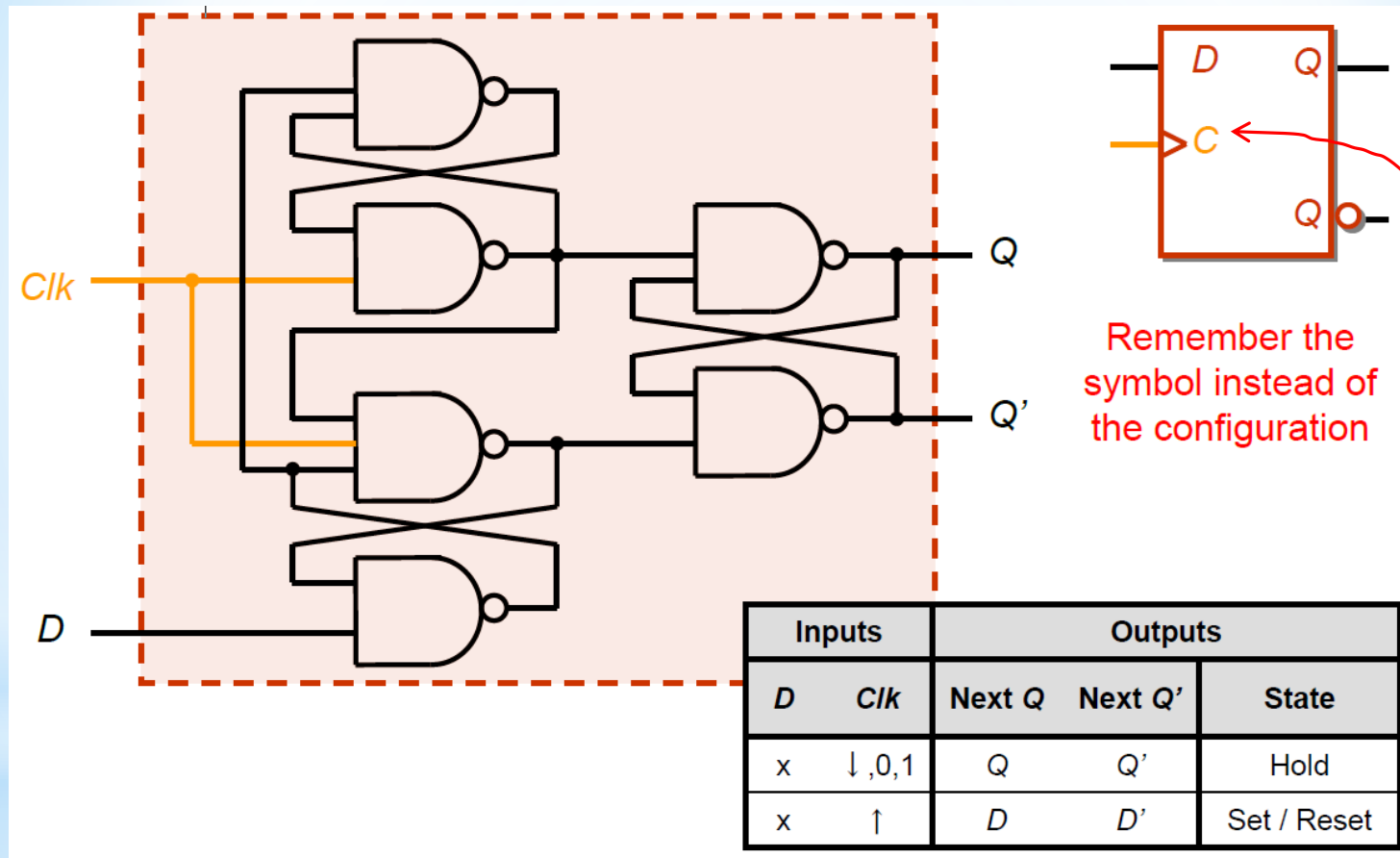


- Negative (falling, trailing) edge-triggering: 1-to-0 transition



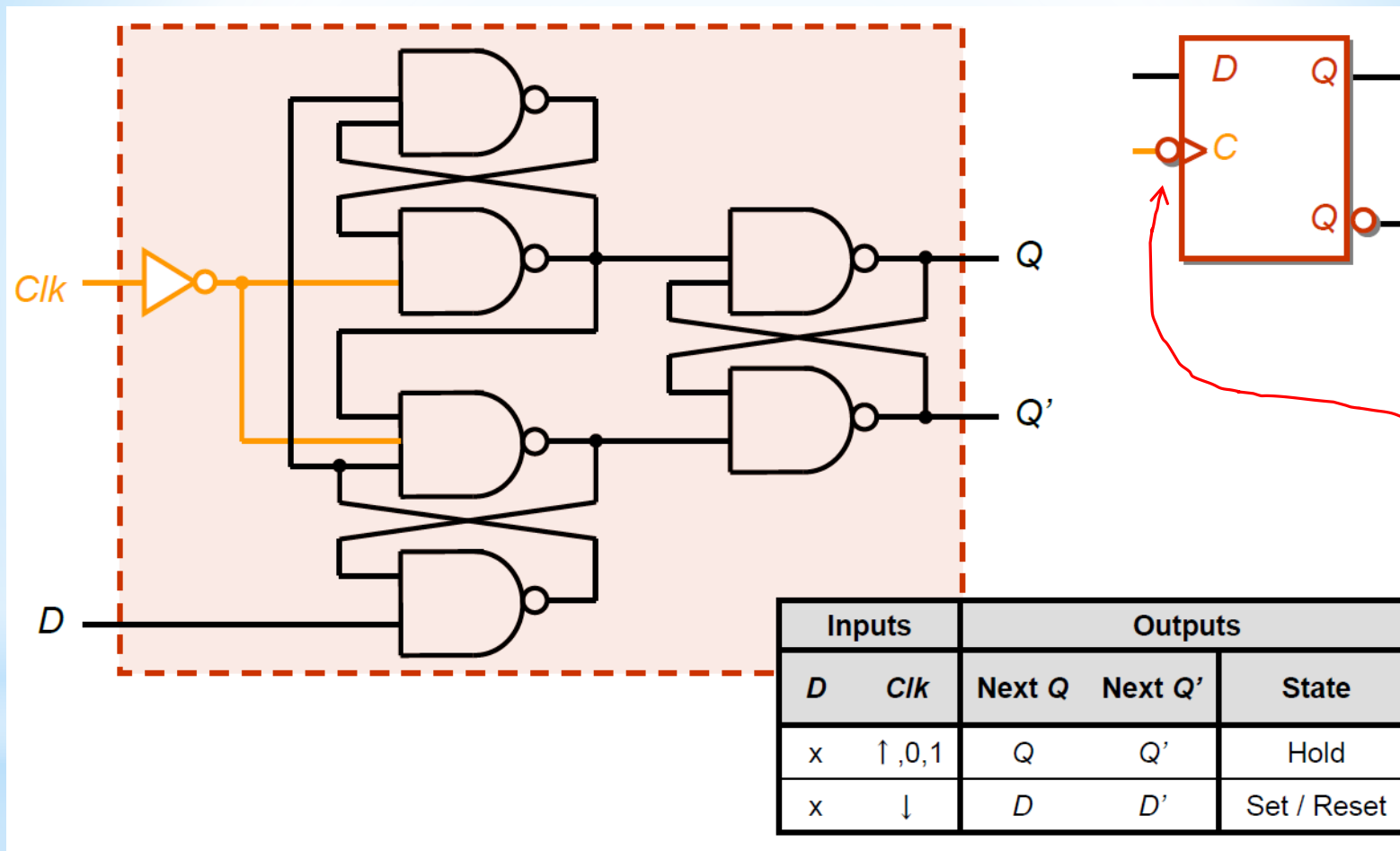
- Additional circuit is used to ensure it will only response to the input at the corresponding clock edge

Positive-Edge-Triggered D FF



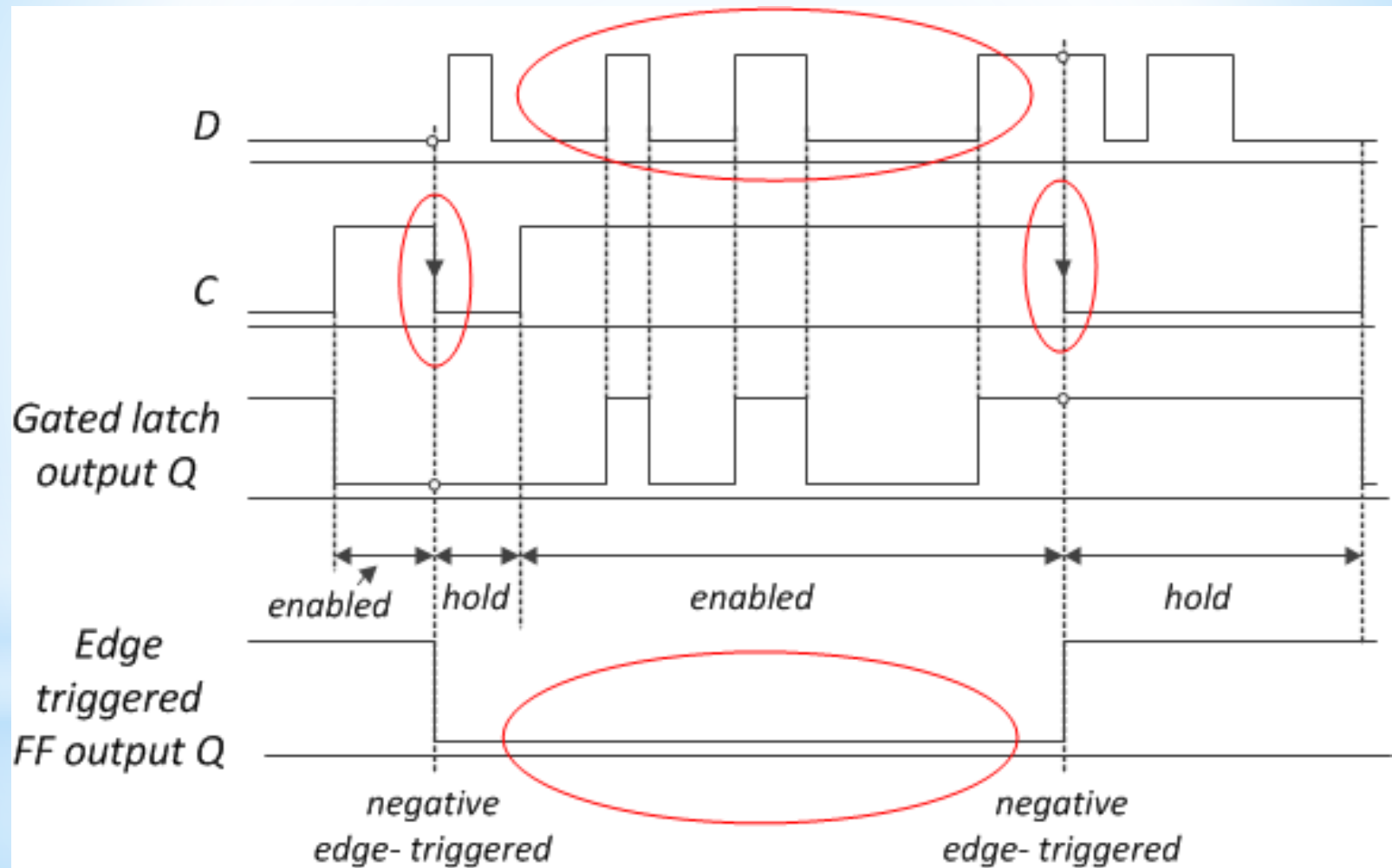
The triangle at the clock input indicates that this is an edge trigger device.

Negative-Edge-Triggered D FF

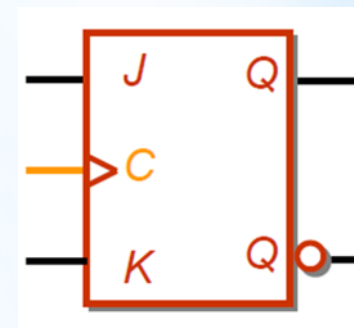
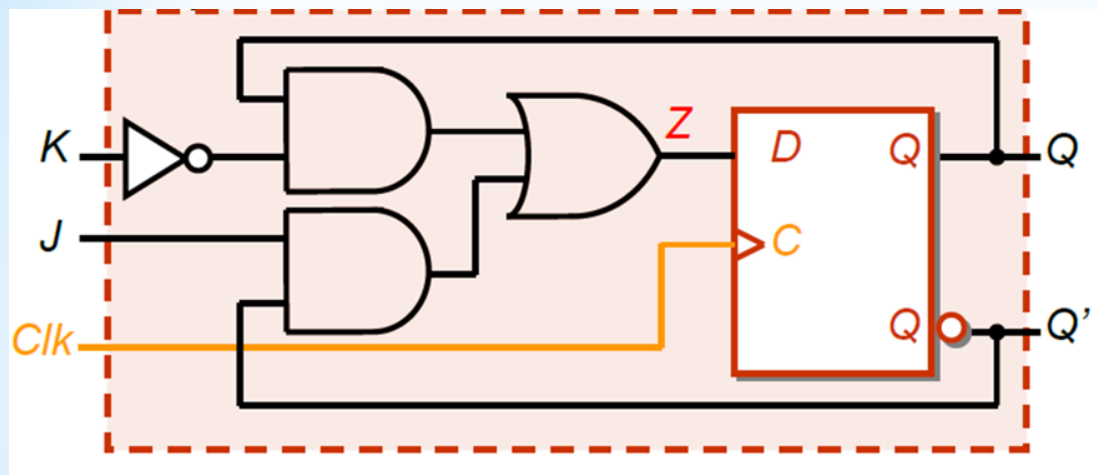


The bubble at the clock input indicates that this is a **negative edge trigger device**.

Effect of edge triggering



Edge-Triggered *JK* Flip-Flop



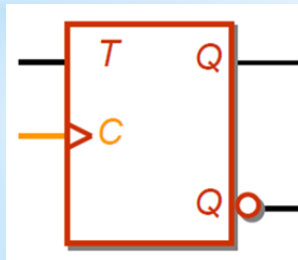
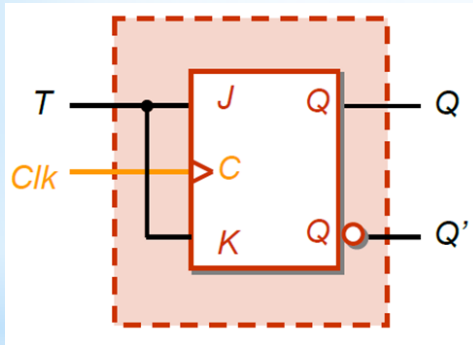
Inputs			Outputs		
<i>J</i>	<i>K</i>	<i>clk</i>	Next <i>Q</i>	Next <i>Q'</i>	meaning
X	X	↓,0,1	<i>Q</i>	<i>Q'</i>	Hold
0	0	↑	<i>Q</i>	<i>Q'</i>	Hold
0	1	↑	0	1	Reset
1	0	↑	1	0	Set
1	1	↑	<i>Q'</i>	<i>Q</i>	Toggle

Edge-Triggered T Flip- Flop

Assign $J = K = T$

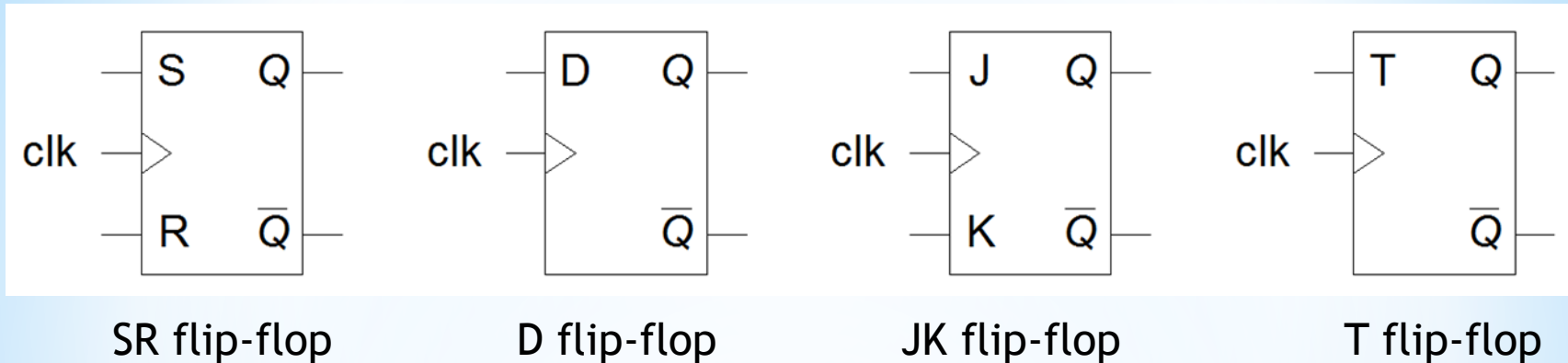
- When $T = 0$ ($J = 0$ and $K = 0$), hold state
- When $T = 1$ ($J = 1$ and $K = 1$), toggle state

Remove the reset and set state

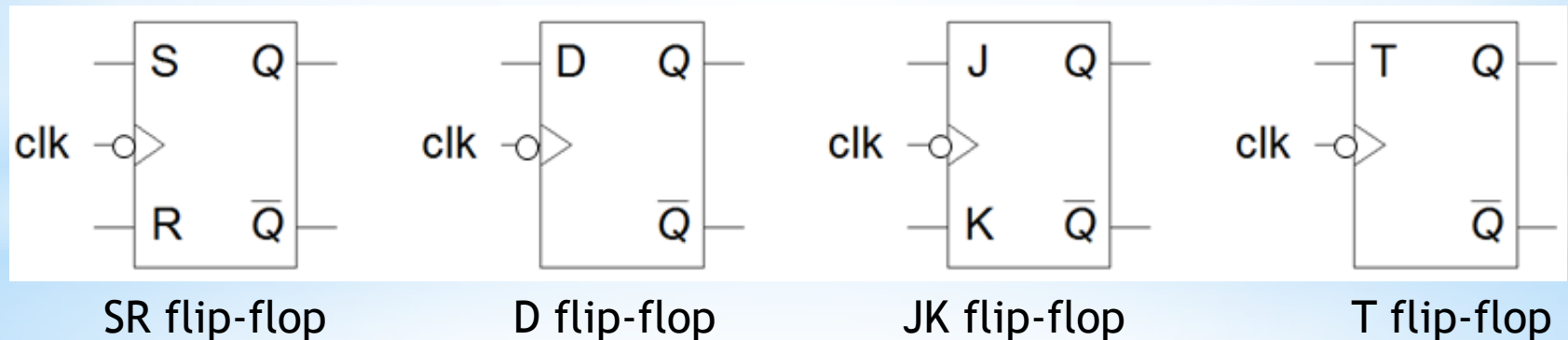


Inputs		Outputs		
T	clk	Next Q	Next Q'	meaning
X	$\downarrow, 0, 1$	Q	Q'	Hold
0	$\uparrow$	Q	Q'	Hold
1	$\uparrow$	Q'	Q	Toggle

Positive-edge triggered FFs



Negative-edge triggered FFs



The details in the symbol tell us how does it work !!!

Memorize the operations!!!

Do NOT memorize the truth table!!!

Memorize the **definition** with positive logic operation:

SR FF :

S=1, R=0, set Q to 1 (set output operation)

S=0, R=1, reset Q to 0 (reset output operation)

S=R=0, not setting anything, Q → unchanged

S=R=1, invalid input (cannot set and reset Q at the same time)

D FF (consider it as a data FF):

Q follows input (Q=0 for D=0,
Q=1 for D=1)

JK FF:

Consider it a special kind of SR FF

J=S, K=R

Q toggle when J=K=1.

T FF:

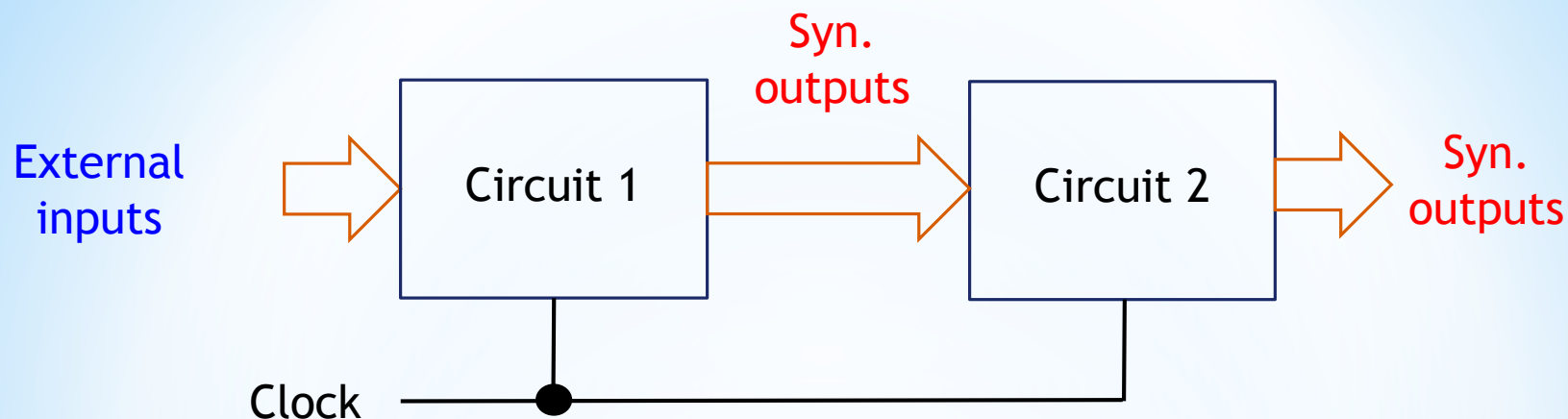
Q toggle when T=1

5.5 Synchronous and Asynchronous operation

- For edge triggered devices, the output changes when the corresponding clock edge appears, i.e. **synchronous operation**
- If the FF's output change when input change, this operation becomes **asynchronous operation**
- Normally, the SR, D, JK and T inputs are all synchronous input for edge triggered device
- All sequentially systems use synchronous device

Asynchronous Preset and Clear

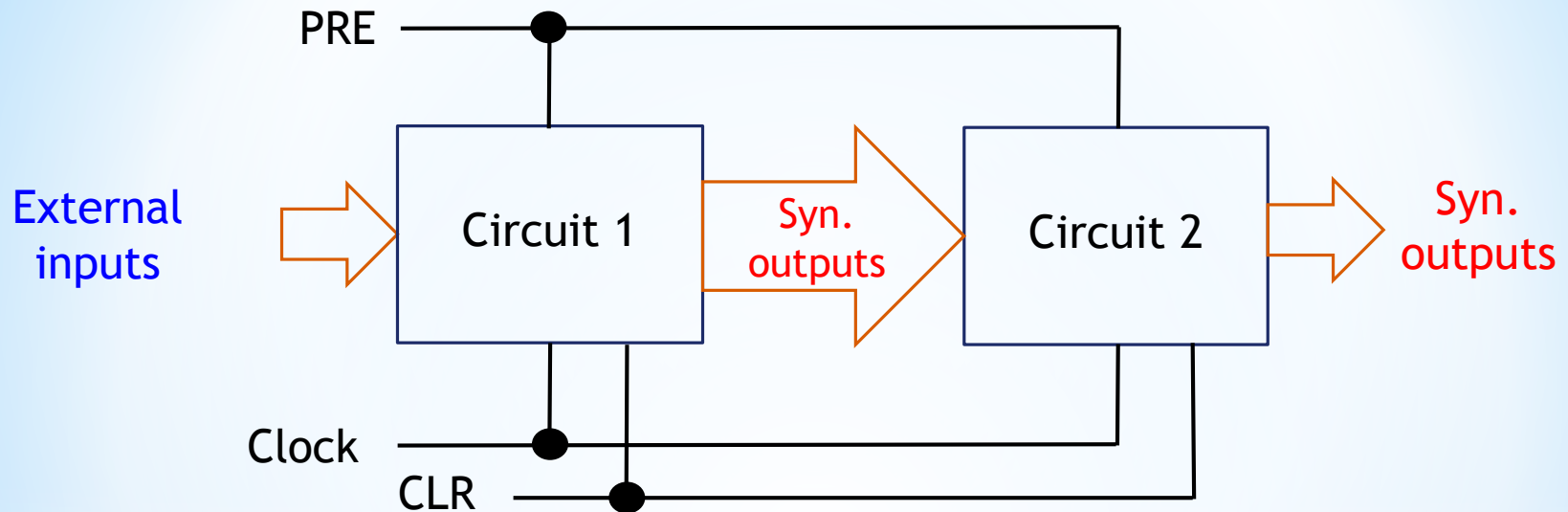
- FF may have two asynchronous inputs (level triggered)
 - Preset (PRE) and clear (CLR)
- The output responds to the inputs normally only when all async. inputs are inactive
- When any of these two PRE or CLR is active, output Q will respond instantaneously
 - PRE active $\rightarrow Q=1$
 - CLR active $\rightarrow Q=0$
- **Never make both PRE and CLR active at the same time**
- Asynchronous inputs are used to set the initial state of the FF prior to normal circuit operation
- They are also used to bring the system back to initial state during normal circuit operation when required



External Inputs: they may change any time, no timing relationship with clock (asynchronous inputs)

Syn. Outputs: they only change when corresponding clock edge appears

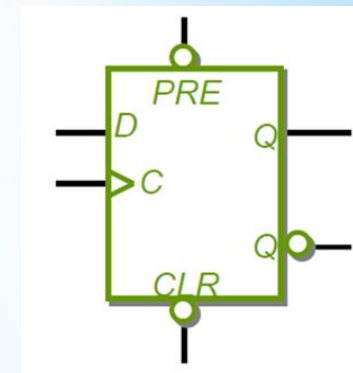
The syn. outputs from circuit 1 becomes syn. Inputs to circuit 2 (common clock for both circuits)



When either PRE *or* CLR is active, the outputs will change instantaneously regardless the clock state or inputs.

Example

Inputs				Outputs		
PRE'	CLR'	clk	D	Next Q	Next Q'	meaning
0	1	X	X	1	0	Preset
1	0	X	X	0	1	Clear
0	0	X	X	1*	1*	Undefined
1	1	$\uparrow$	X	D	D'	Set/Reset
1	1	$\downarrow, 0, 1$	X	Q	Q'	Hold



The same behaviors as D FF

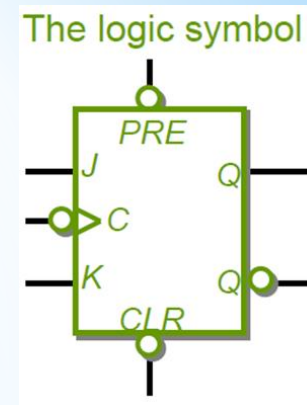
Normal operation

Unpredictable behavior will result if both PRE' and CLR' set to 1 simultaneously

The bubble at the PRE and CLR inputs means that logic “0” will set Q to “1” or reset Q to “0”

Example

The function table of an negative-edge-triggered *JK* FF with asynchronous preset and clear inputs



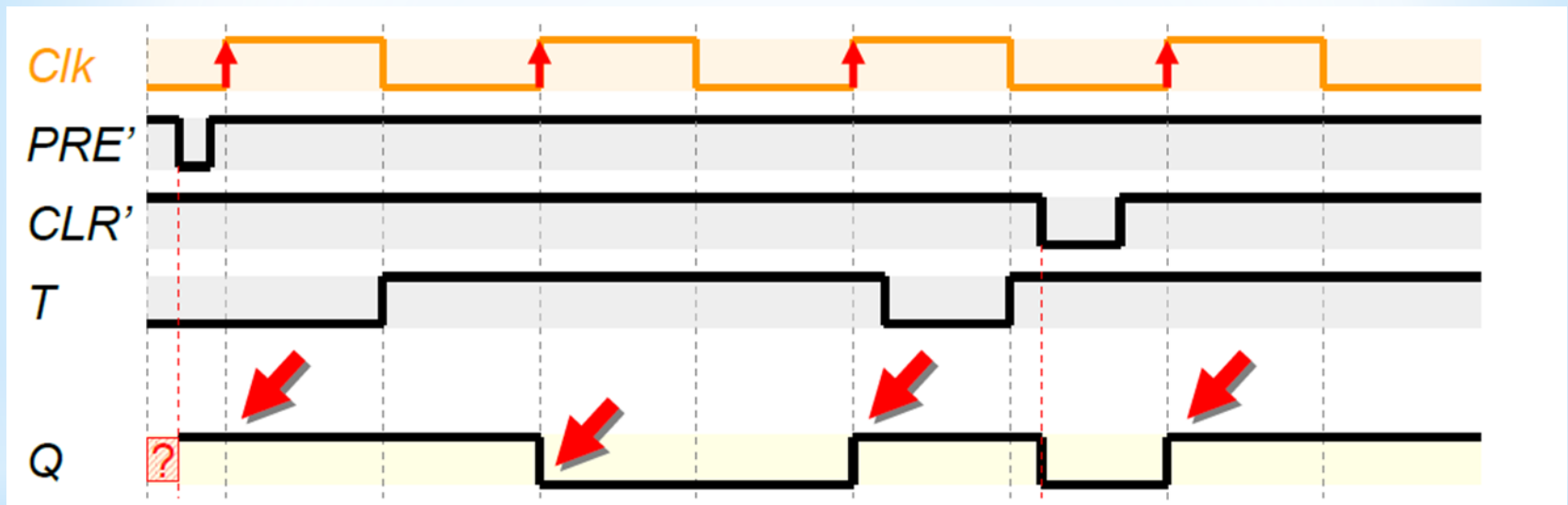
Inputs					Outputs		
PRE'	CLR'	clk	J	K	Next Q	Next Q'	meaning
L	H	X	X	X	H	L	Preset
H	L	X	X	X	L	H	Clear
L	L	X	X	X	H*	H*	Undefined
H	H	↓	L	L	Q	Q'	Hold
H	H	↓	H	L	H	L	Set
H	H	↓	L	H	L	H	Reset
H	H	↓	H	H	Q'	Q	Toggle
H	H	↑,0,1	X	X	Q	Q'	Hold

The same behaviors as *JK* FF

Normal operation

Timing Diagram

Timing Diagram of T FF with asynchronous preset and clear inputs (if no delay)



Response to
asynchronous input PRE'

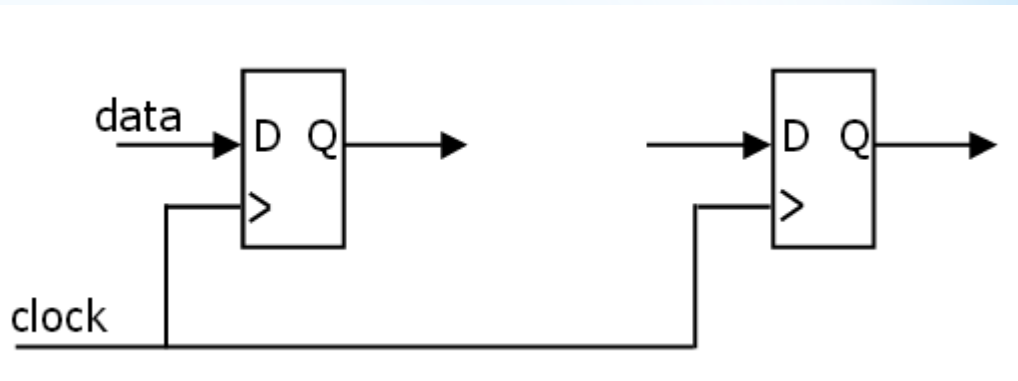
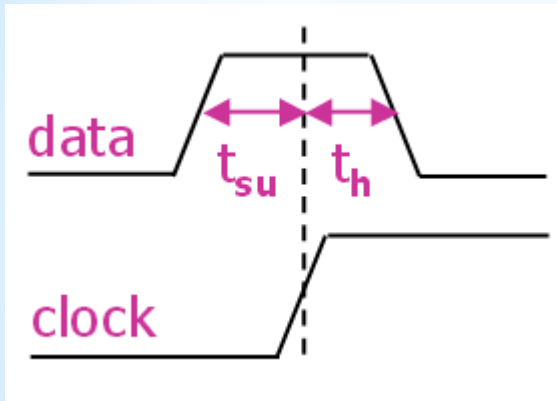
Response to
asynchronous input CLR'

5.6 Flip-Flop timing

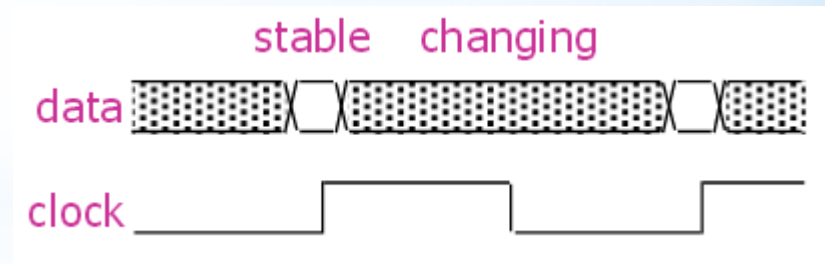
- Logic IC device is made of semi-conductor
- When device is soldered on PCB, its input and output circuits exhibit charging and discharging characteristics when signal changes
- For input, we consider “Setup time” and “Hold time”
- For output, we consider “Propagation delay time”
- Transition time and minimum clock pulse width

Setup time t_{su} : Amount of time the input must be stable before the clock edge

Hold time t_h : Amount of time the input must be stable after the clock edge



There is a timing "window" around the clock edge during which the input must remain stable



If data is not stable for t_{su} before the clock edge and stable for t_h after the clock edge, the D input **MAY NOT** be "read" by the FF.

Propagation delay: The amount of time for the FF output to change its state caused by a trigger signal.

It is defined from the 50% point of the trigger signal to the 50% point of the output signal.

t_{PHL} - propagation time from HIGH to LOW

t_{PLH} - propagation time from LOW to HIGH.

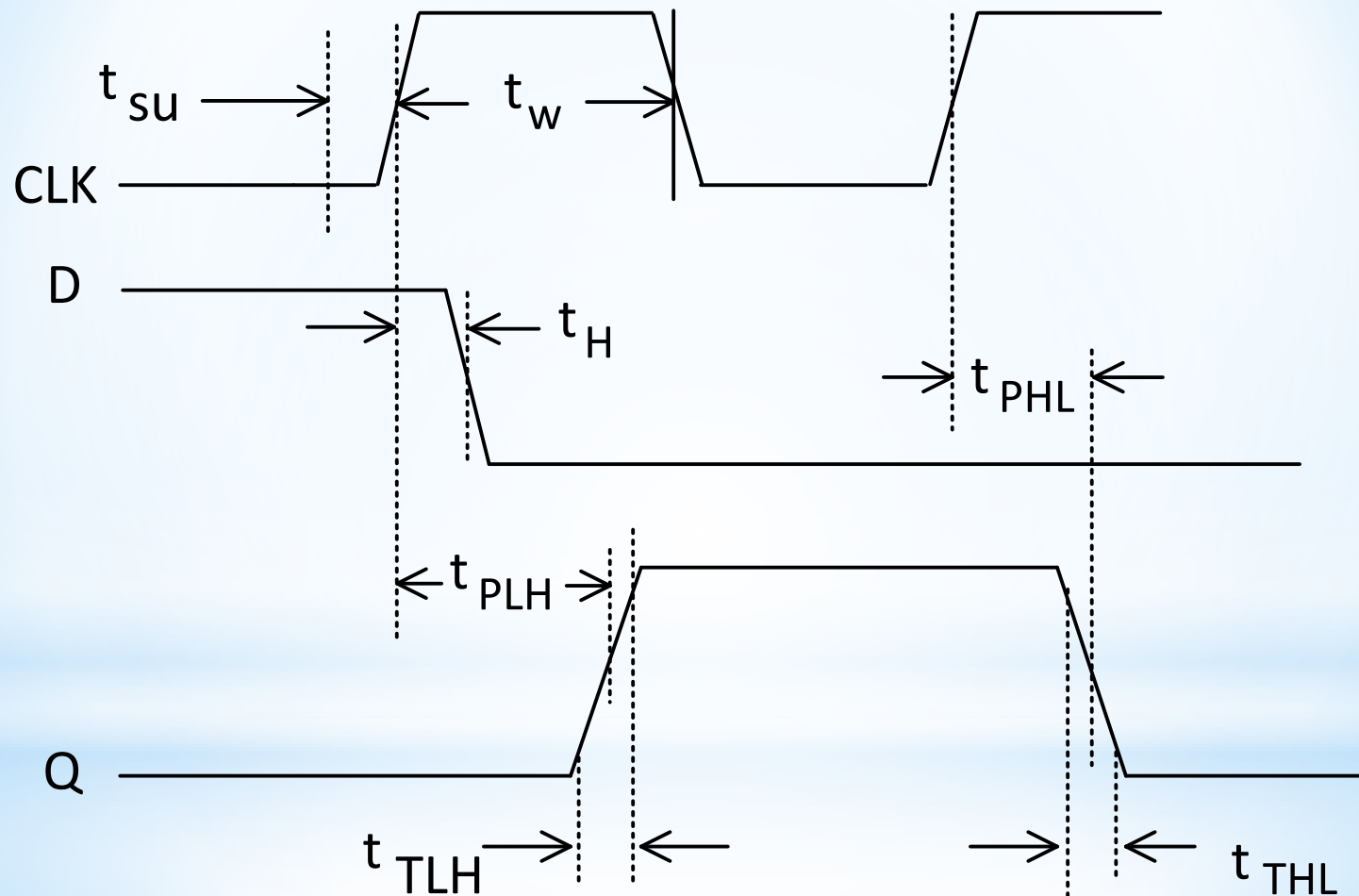
Transition time: The transition time is defined as the rise time or fall time of the signal.

t_{TLH} is the 10% to 90% time to change from LOW to HIGH

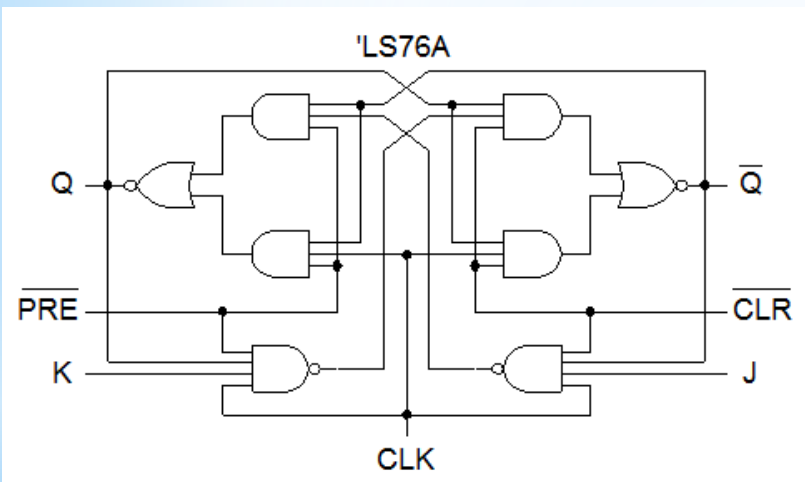
t_{THL} is the 90% to 10% time to change from HIGH to LOW

Minimum pulse width: The minimum pulse width is required to guarantee a correct state change for the flip-flop operation. It is usually denoted by t_w . This parameter indicates the maximum operating clock frequency.

Example: D-type FF Timing illustration



Example: JK edge-triggered FF (54/74LS76A)



INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q_0}$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q_0}$

* This configuration is nonstable, i.e., it will not persist when either preset or clear returns to its active (high) level.

Example: JK edge-triggered FF (54/74LS76A)

Recommended operating conditions:

			SN54LS76A			SN74LS76A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.75	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				-0.4			-0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		30	MHz
t_w	Pulse duration	CLK high	20			20			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time before CLK $\downarrow$	data high or low	20			20			ns
		$\overline{CLR}$ inactive	20			20			
		$\overline{PRE}$ inactive	25			25			
t_h	Hold time-data after CLK $\downarrow$		0			0			ns
T_A	Operating free-air temperature		-55		125	0		70	°C

Example: JK edge-triggered FF (54/74LS76A)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS76A			SN74LS76A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}		$V_{CC} = \text{MIN}, I_{OH} = -0.4 \text{ mA}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	2.5	3.4		2.7	3.4		V
V_{OL}		$V_{CC} = \text{MIN}, I_{OL} = 4 \text{ mA}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}$		0.25	0.4		0.25	0.4	V
		$V_{CC} = \text{MIN}, I_{OL} = 8 \text{ mA}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}$					0.35	0.5	
I_I	J or K	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$				0.3			0.3	
	CLK				0.4			0.4	
I_{IH}	J or K	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$				60			60	
	CLK				80			80	
I_{IL}	J or K	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
	All other				-0.8			-0.8	
$I_{OS}§$		$V_{CC} = \text{MAX}, \text{See Note 4}$	-20		-100	-20		-100	mA
$I_{CC} \text{ (Total)}$		$V_{CC} = \text{MAX}, \text{See Note 2}$		4	6		4	6	mA

Example: JK edge-triggered FF (54/74LS76A)

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	30	45		MHz	$V_{CC} = 5.0\text{ V}$ $C_L = 15\text{ pF}$
t_{PLH}	Clock, Clear, Set to Output		15	20	ns	
t_{PHL}			15	20	ns	

Summary

- Flip-flops as memory elements
 - To store the value in Q
 - One FF can store 1-bit data
- Different types of FFs
 - SR -type, D -type, JK -type, T -type
 - By controlling the inputs (S , R , D , J , K , T) to change, set, reset or hold the value of Q
- Different Triggering Methods
 - level-triggered
 - Edge-triggered
- FF Timing
 - - Setup and hold time
 - - propagation time
 - - transition time
 - - minimum clock pulse width