

EE3220: Assignment 2

Question 1

The memory system requirement for a S3C44B0X based board with *different data bus width* for different memory banks is shown as follows:

ROM: 24M bytes using 4M x 8-bit chips for Bank0 with 16-bit data bus system

RAM: 32M bytes using 4M x 16-bit chips for Bank6 with 32-bit data bus system

- (i) Find the chip count for all the memory components.
- (ii) Design the address table for the memory system.
- (iii) Determine the Boolean expressions of **ALL** the chip select signals.
- (iv) Use standard decoder chips to design the *decoder circuit* (e.g. 2-to-4, 3-to-8, etc..)for the ROM and RAM and draw the circuits (see example in page 10 of Chapter 9).
- (v) Draw the connection diagram of RAM chip to the CPU control signals (see examples in pages 26 & 27 of Chapter 9).

Question 2

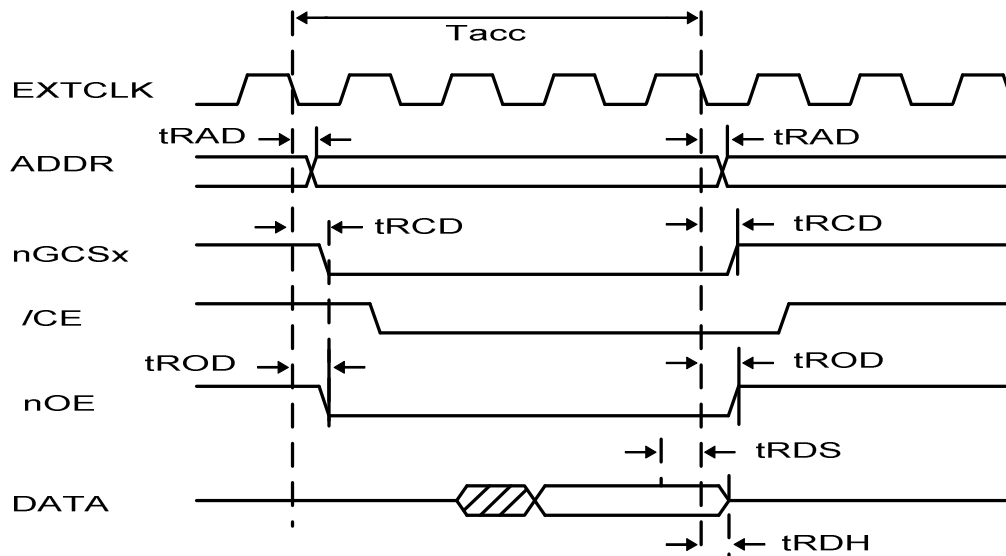
Determine for the number of T_{acc} (with T_{acs} , T_{cos} , T_{och} and $T_{cah} = 0$) cycles required for S3C44B0X to carry out valid read/write operations when operated at 50 MHz with SRAM V62C3801024 (70 ns). Complete the timing diagrams for both read and write cycles for submission, see pages 18 and 24 for details. **Assuming that the address decoder circuit consists of one single chip 74LV138 with delay of 12 ns.**

Question 3

Determine the relevant register setting for interfacing SDRAM PD45128163-I (speed grade – A10) to S3C44B0X with 2 M x 16 x 4 banks configuration. Draw the circuit diagram as well. S3C44B0X is operated at 66 MHz.

Find the memory chip data sheets from internet

S3C44B0X READ CYCLE:



S3C44B0X WRITE CYCLE:

