

EE4218 Computer Architecture
Sem A 2019-20
Tutorial I Solution

Q1.

a.

$$CPI_A = 2.217$$

$$MIPS_A = 564$$

$$T_A = 0.082 \text{ sec}$$

$$CPI_B = 4.225$$

$$MIPS_B = 710$$

$$T_B = 0.056 \text{ sec}$$

b.

Based on effective CPI, machine A has higher performance. Based on MIPS rate and total execution time, machine B has higher performance. The discrepancy is due to smaller instruction count and higher clock rate of machine B.

2.

Memory (contents in hex): 300: 3005; 301: 5940; 302: 7006

Step 1: 3005 → IR; **Step 2:** 3 → AC

Step 3: 5940 → IR; **Step 4:** 3 + 2 = 5 → AC

Step 5: 7006 → IR; **Step 6:** AC → Device 6

3.

PUSH A	LOAD E	MOV R0, E	MUL R0, E, F
PUSH B	MUL F	MUL R0, F	SUB R0, D, R0
PUSH C	STORE T	MOV R1, D	MUL R1, B, C
MUL	LOAD D	SUB R1, R0	ADD R1, A, R1
ADD	SUB T	MOV R0, B	DIV X, R0, R1
PUSH D	STORE T	MOV R0, C	
PUSH E	LOAD B	ADD R0, A	
PUSH F	MUL C	DIV R0, R1	
MUL	ADD A	MOV X, R0	
SUB	DIV T		
DIV	STO X		
POP X			

4.

Let X be the number of one-address instructions. The feasibility of having K two address, X one-address, and L zero-address instructions, all in a 16-bit instruction word, requires that:

$$(K \times 2^6 \times 2^6) + (X \times 2^6) + L = 2^{16}$$

Solving for X:

$$X = (2^{16} - (K \times 2^6 \times 2^6) - L) / 2^6$$

To verify this result, consider the case of no zero-address and no two-address instructions; that is, $L = K = 0$. In this case, we have

$$X = 2^{16} / 2^6 = 2^{10}$$

This is what it should be when 10 bits are used for opcodes and 6 bits for addresses.

5.

The opcode field can take on one of $2^5 = 32$ different values. Each value can be interpreted to ways, depending on whether the Operand 2 field is all zeros, for a total of 64 different opcodes.