

Name: _____.

SID: _____.

EE3220 Worksheet - Answer 1

1. State the various phases of action for the CPU to execution an instruction.

For non-pipelined processor

Fetch, decode, operand fetch(optional), execution, write back (optional)

For pipelined processor

Fetch, decode, execution

2. State the essential information embedded in an instruction.

Op-code, operand, operand location

3. Describe the instruction execution timing characteristic differences between non-pipeline and pipeline processors and state the reasons for these differences.

Non-pipeline processor: instruction may contain operands in associated with external memory, hence the number clock cycles required is different for different addressing modes.

Pipeline processor: fetch, decode and execution units can work concurrently, hence the time for execute an instruction is the same if external memory access is NOT involved.

4. State the reason for a large number of registers for pipeline processor design.

More registers for operands storage, a large chunk of program does not need to access external memory, hence pipeline operation will be broken too frequently.

5. Draw the memory map to illustrate the following data area, if the starting address is 0x0C000000. Determine the address labels: AA, BB and CC.

```
.data
.byte 4, 0x78
AA:
.hword 0x760a, 0b010101111001, 0x17e5
BB:
.skip 6
.align
CC:
.word 0xaa7169bc, 0x72ae76f
```

Address	+0	+1	+2	+3
0x0C000000	04	78	0a	76
0x0C000004	79	05	e5	17
0x0C000008				
0x0C00000C			00	00
0x0C000010	bc	69	71	aa
0x0C000018	6f	e7	2a	07

AA: 0x0C000002

BB: 0x0C000008

CC: 0x0C000010