

EE2000 2018/19 Assignment 4 (Due: Dec 2, Sunday, 2018 12:00 midnight)

Question 1: (VHDL Statement)

Given the concurrent VHDL statements.

B <= A and C after 3 ns;

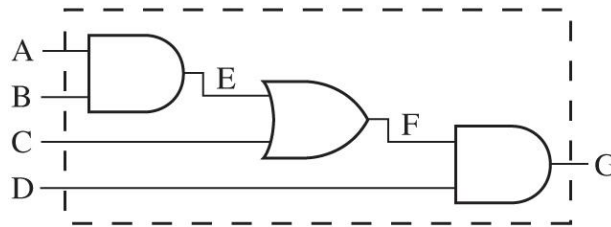
C <= not B after 2ns;

- 1) Draw the circuit the statements represent.
- 2) Draw a timing diagram if initially A = B = '0' and C = '1', and A changes to '1' at time 5 ns. Draw the timing diagram until 22 ns.

Question 2: (Basic VHDL Statement)

Write VHDL code for the following circuit. Assume that the gate delays are negligible (no delay).

- 1) Using concurrent statements.
- 2) Using a process with sequential statements.



Question 3: (Block Diagram)

Consider the following VHDL Code:

```
5 entity Q3 is
6     port(
7         A, B, C, F, Clk: in bit;
8         E: out bit
9     );
10 end Q3;
11
12 architecture Behavioral of Q3 is
13     signal D, G: bit;
14     begin
15         process(Clk)
16         begin
17             if (clk'event) and (clk = '1') then
18                 D <= A and B and C;
19                 G <= not A and not B;
20                 E <= D or G or F;
21             end if;
22         end process;
23     end Behavioral;
```

- 1) Draw a block diagram for the circuit (no gates – only at the block level)
- 2) Draw the circuit generated by the above code (at the gate level)

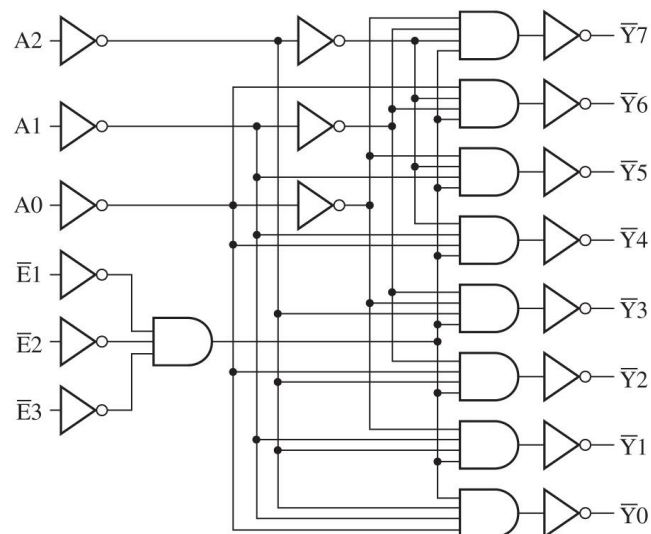
Question 4: (DFF with Synchronous Clear)

In the lecture, we have covered how to design a D-type Flip-Flop with Asynchronous Clear, as shown below. Now, 1) modify the design to turn it into a DFF with Synchronous Clear, 2) provide a testbench for this design, 3) simulated waveform to demonstrate the design is working properly.

```
34 entity DFF_AC is
35   -- Port ( );
36   port (
37       CLK, D, ClrN: in std_logic;
38       Q: out std_logic
39   );
40 end DFF_AC;
41
42 architecture Behavioral of DFF_AC is
43 begin
44     process (CLK, ClrN)
45     begin
46         if CLRn = '0' then Q <= '0';
47         else if CLK'event and CLK = '1'
48             then Q <= D;
49         end if;
50     end if;
51 end process;
52 end Behavioral;
```

Question 5: (Decoder)

The 74HC138 is a 3-to-8 decoder with a logic diagram as shown below. Please write a dataflow VHDL model for this circuit using the corresponding logical equations.



Please submit your answer into a single file in PDF format, together with your waveform simulation in this assignment. A submission box on Canvas is created for you.

End