

CITY UNIVERSITY OF HONG KONG

Course code & title : EE 6427 Modern Power Electronics
Session : Semester B 2005/2006
Time allowed : Three hours

This paper has SEVEN pages (including this page).

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1. This paper consists of 5 questions.
 2. Choose **ANY FOUR** questions. (25 marks per question)
 3. The full mark of this paper is 100.
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Materials, aids & instruments permitted to be used during examination:

1. Approved calculator
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Answer any FOUR questions:

Q.1

(a) Sketch a typical safe operating area (SOA) of a power mosfet. (4 marks)

(b) Explain the limitations of the SOA of a power mosfet. (4 marks)

(c) Briefly explain why power mosfets are more suitable for parallel operation than power BJTs. (5 marks)

(d) Several power mosfet switches are connected in parallel in order to increase the total current capability. They are mounted on the same heatsink. The case of the mosfet is coated with an insulation material. The junction-to-case thermal resistance is $0.5^{\circ}\text{C}/\text{W}$. All of the switches are switched at 20kHz together. The energy loss per power switch is 1 mJ per switching cycle. The heatsink has a thermal resistance of $0.5^{\circ}\text{C}/\text{W}$. The ambient temperature is 40°C . The junction temperature must not exceed 125°C .

(i) Calculate the maximum number of parallel switches. (8 marks)

(ii) Calculate the heatsink temperature. (4 marks)

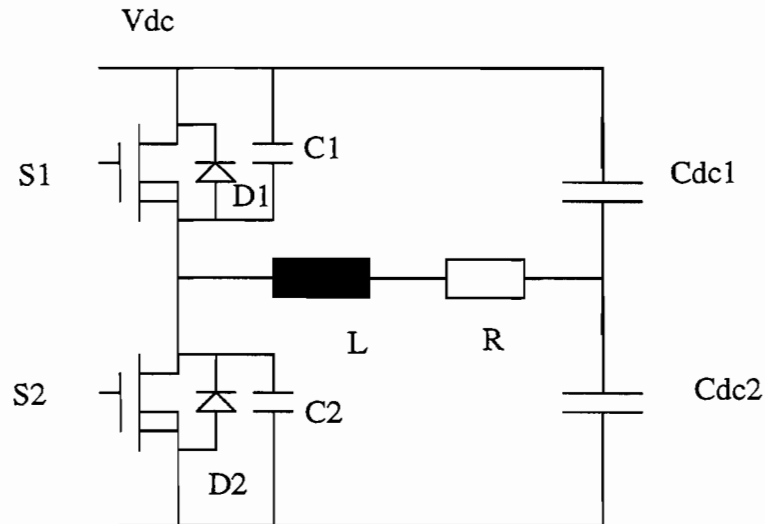
Q2

(a) Fig.Q2 shows a half-bridge power inverter feeding an inductive load. Explain the functions of C1, C2 and Cdc1 and Cdc2.

(4 marks)

(b)

Fig.Q2



(i) Sketch typical switching waveforms of the gating signals of power switches S1 and S2.

(4 marks)

(ii) With the aid of equivalent circuits and the switching waveforms in (b-i), explain the six operating modes of this inverter in order that both S1 and S2 be zero-voltage-switched.

(12 marks)

(c) If the load current is very small, explain why it is likely that zero-voltage switching may not be achieved. Suggest one solution (e.g. modification of this circuit) to ensure that zero-voltage switching can always be achieved.

(5 marks)

Q3

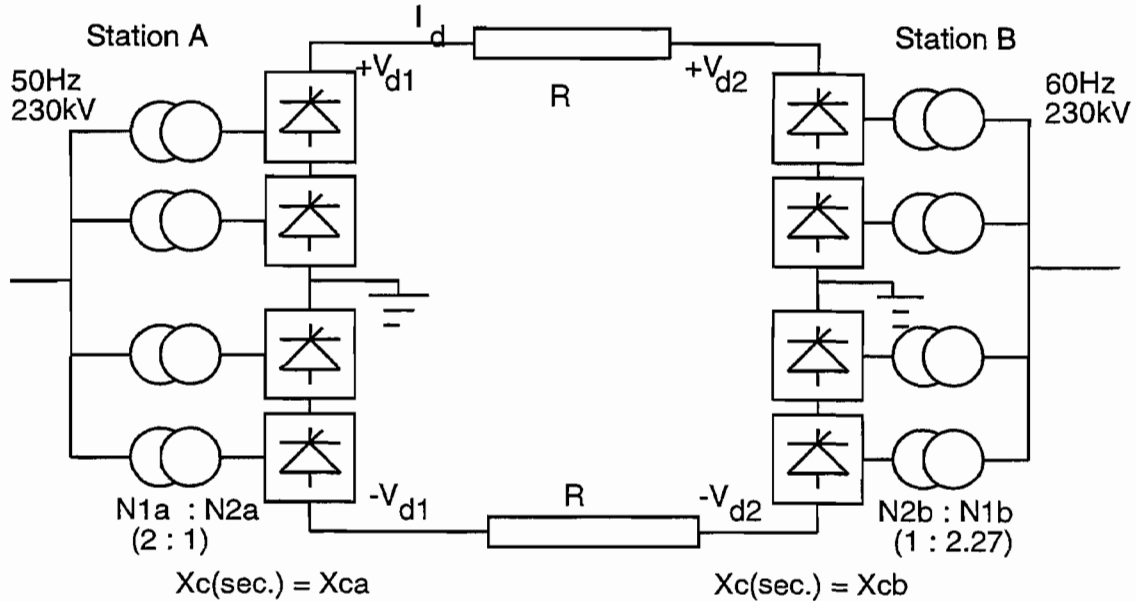


Fig.Q3

A HVDC transmission system is 3000 km long and interconnects two 230kV AC systems. Terminal A is the energy sending station and is connected to an AC system of **50 Hz**, whilst terminal B is the receiving end connected to AC system of **60 Hz**. Each terminal station consists of four 6-pulse converter bridges (two converters per pole) with each pole rated at nominal DC ratings of $\pm 250\text{kV}$.

The source leakage inductance (referred to the secondary winding) for converter transformers A and B are $L_{ca} = 45\text{mH}$ and $L_{cb} = 40\text{mH}$ respectively. The steady-state dc current is set at 1000A. The turns ratios of the converter transformers for converter stations A and B are $N1a/N2a = 2.00$ and $N1b/N2b = 2.27$ respectively.

Suppose that the minimum inverter extinction angle is 17° , the DC line winding resistance $12\text{m}\Omega$ per kilometre, and that the general equation for the mean dc converter output voltage V_d is:

$$V_d = \frac{3\sqrt{2}}{\pi} V_{LL} \cos \alpha - \frac{3X_c}{\pi} I_d, \text{ where } \alpha \text{ is the delay angle, } V_{LL} \text{ is the line to line voltage,}$$

I_d is the mean converter dc current and X_c the secondary transformer reactance. Determine:

- the dc winding resistance (R) per pole; (3 marks)
- the secondary transformer reactances (X_{ca} and X_{cb}) for stations A and B respectively; (6 marks)
- the dc link voltages at both ends of the HVDC line; (8 marks)
- the delay angle of the converter in station A. (5 marks)
- Give 3 advantages of DC transmission over AC transmission system for long distance power transmission (say at least 1000 km). (3 marks)

Q4

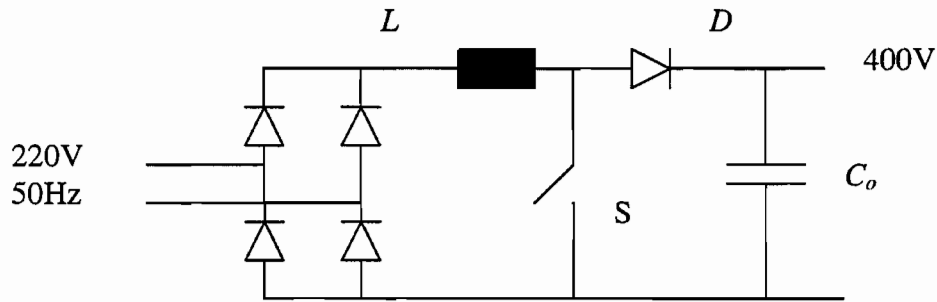


Fig.Q4

- (a) State the two conditions for achieving unity power factor. (2 marks)
- (b) Explain, with the aid of circuit diagrams and typical waveforms, how a boost-type DC-DC converter (as shown in Fig.Q4) can be used to provide input power factor correction for AC-DC power conversion with the rectifier bridge. (6 marks)
- (c) The circuit in Fig.Q4 is fed with a load with an average output DC voltage of 400V and a constant DC current of 4A. Assuming that the input power factor is unity and an overall energy efficiency is 95%, calculate:
 - (i) the required root-mean-square (rms) input current from the 220V, 50 Hz AC supply; (4 marks)
 - (ii) the minimum capacitance value for the output capacitor C_o of the boost converter in order that the voltage ripple across C_o be less than 30V. (7 marks)
- (d) This boost circuit may suffer a serious EMI emission problem because of non-ideal power diode. Give the reason for this problem and modify the circuit in order to suppress EMI. (6 marks)

Q5

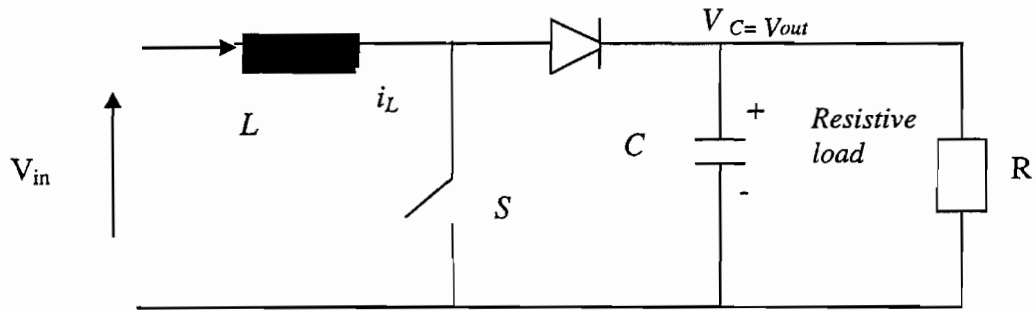


Fig.Q5

Fig.Q5 shows the schematic of a boost (step-up) converter.

The general form of its state-space equation in time domain is

$$\frac{dX}{dt} = AX + BU$$

$$Y = CX$$

where X is the variable matrix, U is the forcing function and Y is the output; A, B and C are matrixes describing the characteristics of the system.

- (a) Assuming that the inductor current is continuous, sketch the equivalent circuits for the conducting paths and derive the state-space equations (using i_L and v_C as state variables) in the time domain for the circuit shown in Fig.Q5 (including the effect of the load) when the

- (i) power switch S is turned on;
- (ii) power switch S is turned off.

(14 marks)

- (b) Using the results in (a) and for a nominal switching duty cycle of d , derive the “averaged” state-space equation in the time domain for the converter.

(6 marks)

- (c) Comment on the requirements on the input EMI filter for (i) constant frequency and (ii) variable frequency operations.

(5 marks)

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