

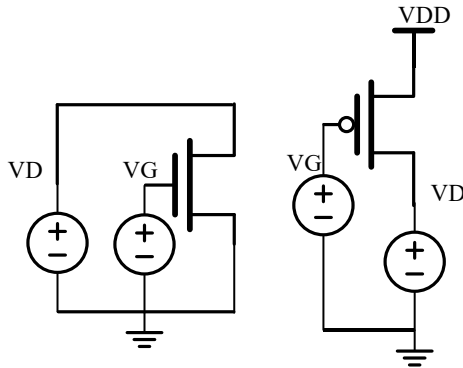
EE4803: Analog IC Design

Laboratory Manual

For each lab exercise, please call TA to show your result. Please take screenshot or save the result of your exercise for the final lab report.

Lab 1: Understanding MOS and VIRTUOSO Environment

1. Simulate NMOS and PMOS I_d vs V_{gs} for various W/L (at fixed V_{ds}) – understanding DC voltage sweep



- What is effect of increasing W/L on I_d vs V_{gs} ? – understand parametric sweep
- Can you fit curves to get K_n' and K_p' ?

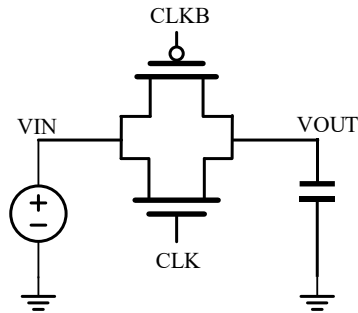
2. Simulate NMOS and PMOS I_d vs V_{ds} for various W/L (at fixed V_{gs}) -- understanding DC voltage sweep

- What is effect of increasing L with fixed W/L on I_d vs V_{ds} ? – understand parametric sweep
- Can you fit curves to get dependence of λ on L ?

From now on, use these equations to perform hand design of your circuit before you start simulation.

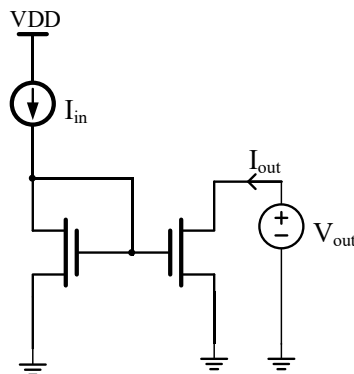
3. Design a switch to charge a load capacitor of 10 pF (*try 2 initial conditions of voltage on capacitor: (a) 0 V & (b) Vdd*) in a fixed time period of 10 ns to within 1% of a desired voltage of $V_{dd}/2$. First, create a hand design to meet specifications using the earlier derived transistor parameters. (*Need to create an inverter and create symbol for it; Need to understand how to create pulse voltage source; Need to know how to set initial condition*)

- NMOS only
- PMOS only
- Transmission gate



Lab 2: Current Mirror and Common Source

4. Simulate a simple current mirror given a bias current of 1 μA .



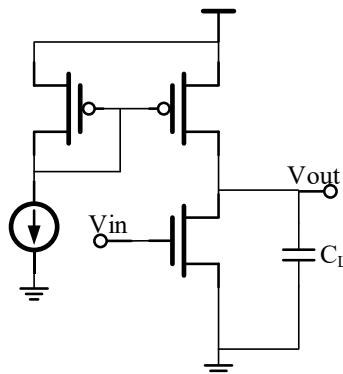
a. Design the (W/L) of the transistors in the circuit for output resistance > 20 Mohm.

b. How can you increase output resistance to > 1 Gohm?

(Hint: use cascode)

- Find $V_{\min}$ for both.
- Match the simulated resistances with a theoretical calculation based on the earlier derived transistor parameters.

5. Simulate a Common Source amplifier with current source load given the bias current of 1 μA and load capacitor $C_L = 1$ pF.



The (W/L) of the common source NMOS is (5/0.5) and the current mirror transistors are (5/1).

(a) Perform DC sweep of input voltage

(b) Perform AC frequency sweep and plot transfer function

(c) Apply input sinusoid signal and perform transient simulation to check time domain waveform and correspondence with frequency response in part (b).

- Understand how to provide AC input and what should be DC operating point
- Understand how to perform AC transfer function simulation
- Now, redesign the amplifier and try to increase (a) gain (G), (b) bandwidth (BW) and (c) gain bandwidth (GBW) product by at least a factor of 2 while minimizing power dissipation. (these are 3 separate experiments)

HINT: For each case, find out the theoretical equations.

$$G = -g_{mn} (r_{on} \parallel r_{op})$$

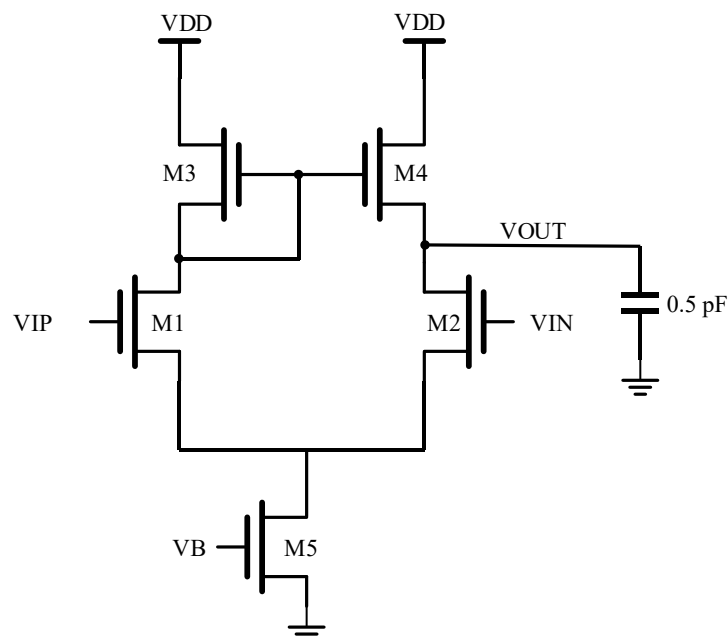
$$BW = 1 / ((r_{on} \parallel r_{op})C_L)$$

$$GBW = g_m / C_L$$

From these equations, try to decide how to change bias current or transistor sizes to increase each of these parameters.

Lab 3: Differential Amplifier Design

6. Design a 5T differential amplifier with the following specifications:



- AC gain > 50 V/V
- GBW > 10 MHz
- ICMR better than (0.8 – 1.3) V.
- Load Capacitance = 0.5 pF

Try to design the amplifier while minimizing power dissipation. Please do a hand design first using the earlier derived transistor parameters.

You need to understand the simulation setup to measure each specification.

7. Design a 9T/11T/13T differential amplifier to match the below specifications with and comment on differences between the two.

- AC gain > 30dB
- GBW > 5MHz
- ICMR better than (0.3 – 0.8) V.
- Load Capacitance = 0.5 pF

